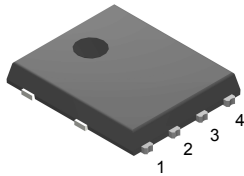
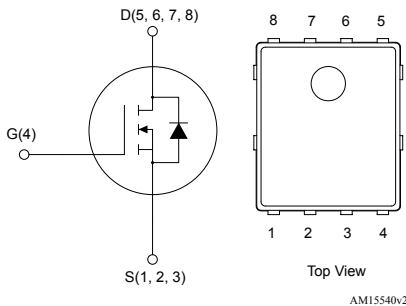



## Automotive-grade N-channel 30 V, 4 mΩ typ., 80 A STripFET™ H6 Power MOSFET in a PowerFLAT™ 5x6 package


**PowerFLAT™ 5x6**


### Features

Order code	V <sub>DS</sub>	R <sub>DS(on)</sub> max.	I <sub>D</sub>
STL86N3LLH6AG	30 V	5.2 mΩ	80 A

- AEC-Q101 qualified 
- Very low on-resistance
- Very low gate charge
- High avalanche ruggedness
- Low gate drive power loss
- Logic level
- Wettable flank package

### Applications

- Switching applications

### Description

This device is an N-channel Power MOSFET developed using the STripFET™ H6 technology with a new trench gate structure. The resulting Power MOSFET exhibits very low R<sub>DS(on)</sub> in all packages.

#### Product status link

[STL86N3LLH6AG](#)

#### Product summary

<b>Order code</b>	STL86N3LLH6AG
<b>Marking</b>	86N3LLH6
<b>Package</b>	PowerFLAT™ 5x6
<b>Packing</b>	Tape and reel

# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage	30	V
$V_{GS}$	Gate-source voltage	$\pm 20$	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	80	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 70\text{ }^\circ\text{C}$	60	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	51	A
$I_{DM}^{(2)(1)}$	Drain current (pulsed)	320	A
$I_D^{(3)}$	Drain current (continuous) at $T_{pcb} = 25\text{ }^\circ\text{C}$	21	A
$I_D^{(3)}$	Drain current (continuous) at $T_{pcb} = 70\text{ }^\circ\text{C}$	15.7	A
$I_D^{(3)}$	Drain current (continuous) at $T_{pcb} = 100\text{ }^\circ\text{C}$	13.1	A
$I_{DM}^{(2)(3)}$	Drain current (pulsed)	84	A
$P_{TOT}^{(1)}$	Total power dissipation at $T_C = 25\text{ }^\circ\text{C}$	60	W
$P_{TOT}^{(3)}$	Total power dissipation at $T_{pcb} = 25\text{ }^\circ\text{C}$	4	
$T_{stg}$	Storage temperature range	- 55 to 150	$^\circ\text{C}$
$T_j$	Operating junction temperature range		

1. The value is rated according to  $R_{thj-c}$ .
2. Pulse width limited by safe operating area.
3. The value is rated according to  $R_{thj-pcb}$ .

**Table 2. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	2.08	$^\circ\text{C/W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	31.3	

1. When mounted on FR-4 board of 1 inch<sup>2</sup>, 2oz Cu,  $t < 10\text{ s}$

## 2 Electrical characteristics

( $T_C = 25\text{ °C}$  unless otherwise specified).

**Table 3. On/off-states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$ , $I_D = 1\text{ mA}$	30			V
$I_{DSS}$	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$ , $V_{DS} = 30\text{ V}$			1	$\mu\text{A}$
		$V_{GS} = 0\text{ V}$ , $V_{DS} = 30\text{ V}$ , $T_C = 125\text{ °C}^{(1)}$			10	
$I_{GSS}$	Gate-body leakage current	$V_{DS} = 0\text{ V}$ , $V_{GS} = \pm 20\text{ V}$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	1	1.7	2.5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$ , $I_D = 10.5\text{ A}$		4	5.2	$\text{m}\Omega$
		$V_{GS} = 4.5\text{ V}$ , $I_D = 10.5\text{ A}$		6.7	7.6	$\text{m}\Omega$

1. Defined by design, not subject to production test.

**Table 4. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 25\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0\text{ V}$	1350	1690	2030	pF
$C_{oss}$	Output capacitance		230	290	350	pF
$C_{rSS}$	Reverse transfer capacitance		140	176	210	pF
$Q_g$	Total gate charge	$V_{DD} = 15\text{ V}$ , $I_D = 21\text{ A}$ ,	-	17	-	nC
$Q_{gs}$	Gate-source charge	$V_{GS} = 0\text{ to }4.5\text{ V}$	-	8	-	nC
$Q_{gd}$	Gate-drain charge	(see Figure 12. Test circuit for resistive load switching times)	-	6	-	nC
$R_G$	Gate input resistance	$f = 1\text{ MHz}$ , $I_D = 0\text{ A}$	1.25	1.7	1.2	$\Omega$

**Table 5. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 15\text{ V}$ , $I_D = 10.5\text{ A}$ , $R_G = 4.7\text{ }\Omega$ , $V_{GS} = 10\text{ V}$	-	9.5	-	ns
$t_r$	Rise time		-	30	-	ns
$t_{d(off)}$	Turn-off delay time	See Figure 12. Test circuit for resistive load switching times and Figure 17. Switching time waveform	-	37	-	ns
$t_f$	Fall time		-	12	-	ns

**Table 6. Source-drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		21	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		84	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 21\text{ A}$ , $V_{GS} = 0\text{ V}$	-		1.1	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 10.5\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$	-	24		ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 25\text{ V}$	-	16.8		nC
$I_{RRM}$	Reverse recovery current	See Figure 14. Test circuit for inductive load switching and diode recovery times	-	1.4		A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%.

## 2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

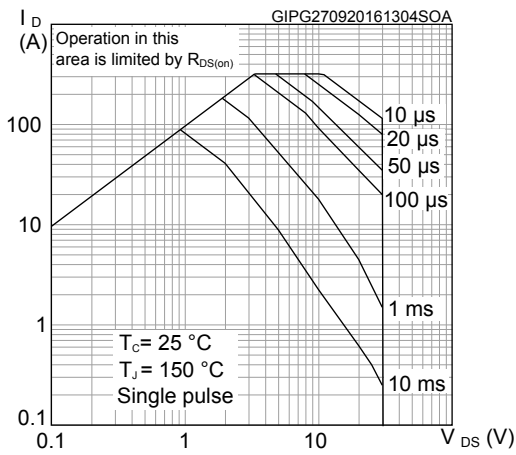


Figure 2. Thermal impedance

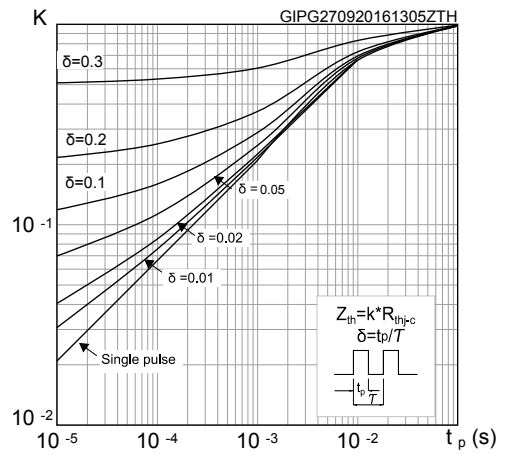


Figure 3. Output characteristics

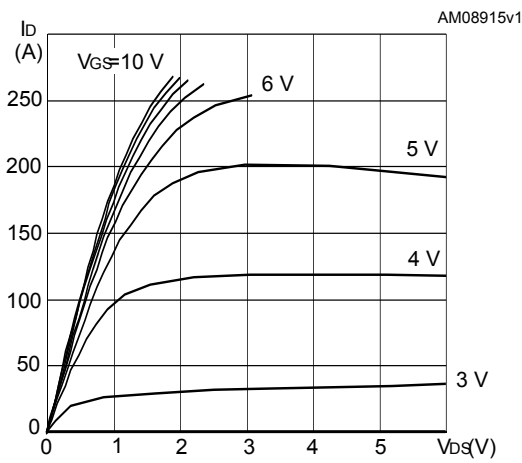


Figure 4. Transfer characteristics

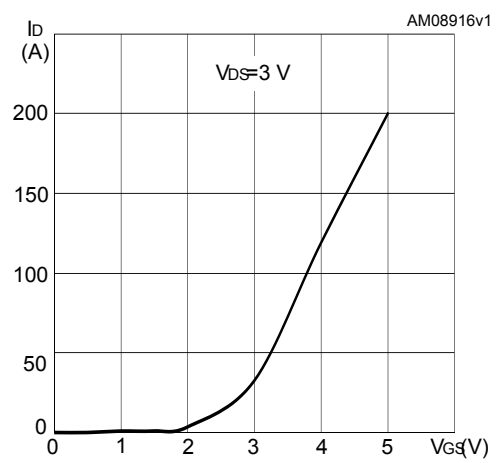


Figure 5. Normalized  $V_{(BR)DSS}$  vs temperature

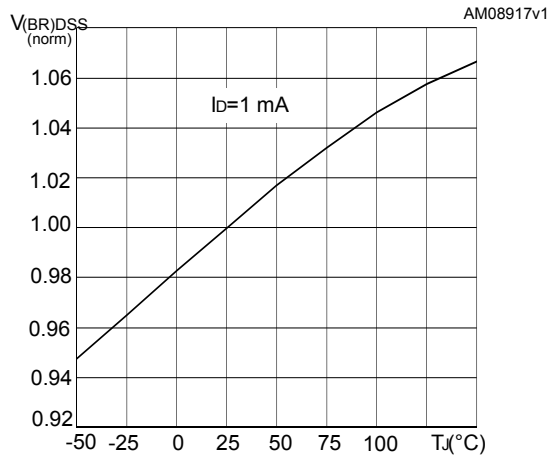


Figure 6. Static drain-source on-resistance

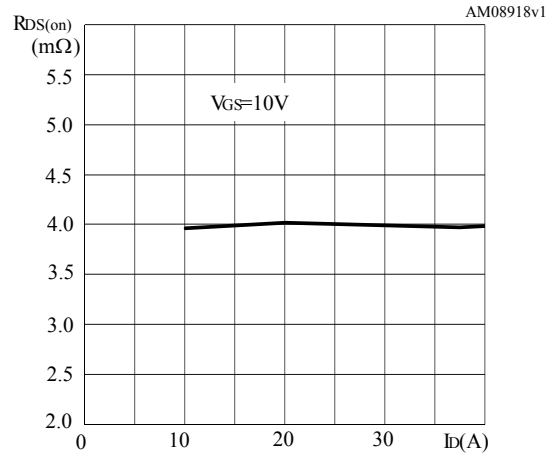


Figure 7. Gate charge vs gate-source voltage

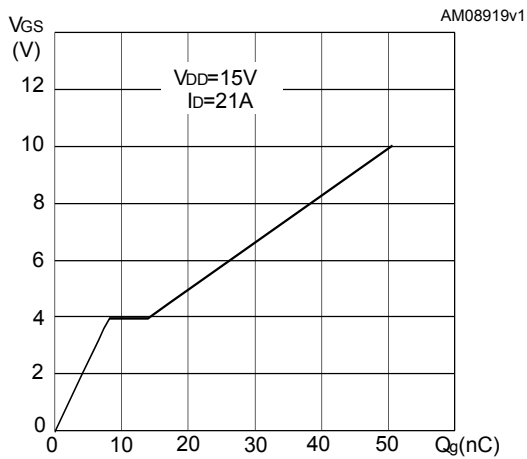


Figure 8. Capacitance variations

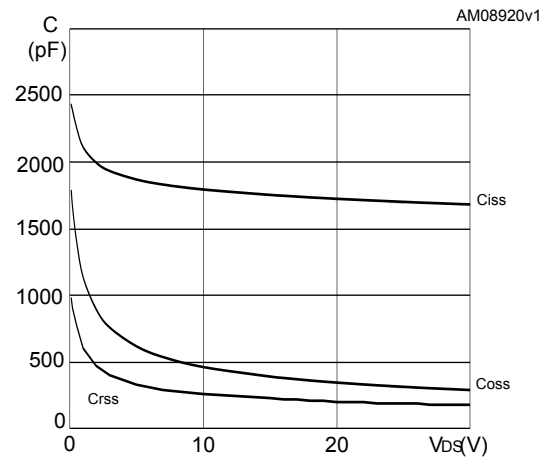


Figure 9. Normalized gate threshold voltage vs temperature

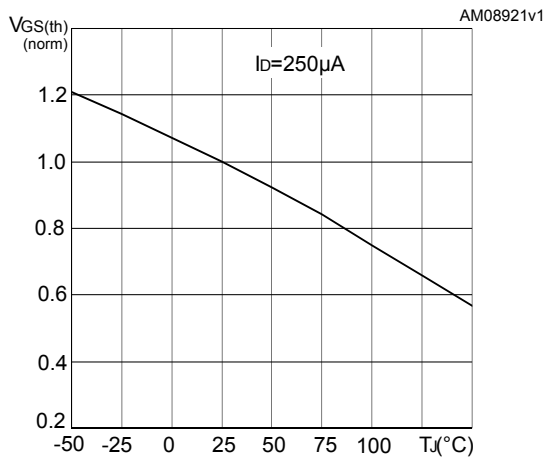
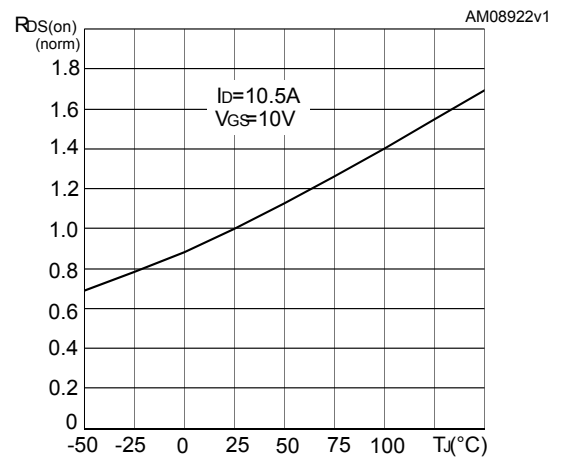
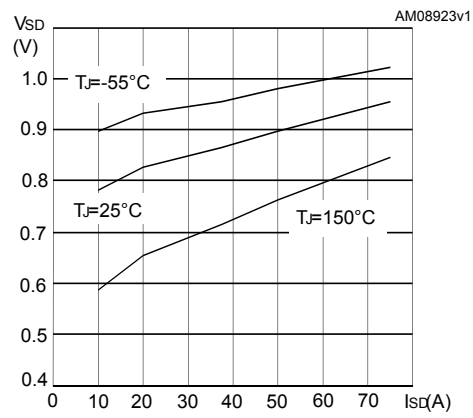


Figure 10. Normalized on resistance vs temperature



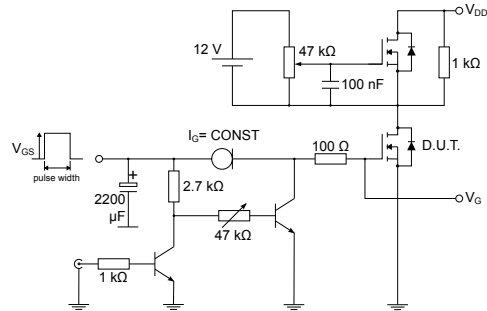
**Figure 11. Source-drain diode forward characteristics**



### 3 Test circuit

**Figure 12. Test circuit for resistive load switching times**

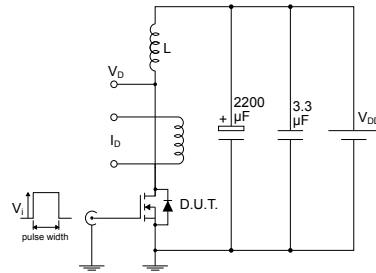

AM01468v1

**Figure 13. Test circuit for gate charge behavior**


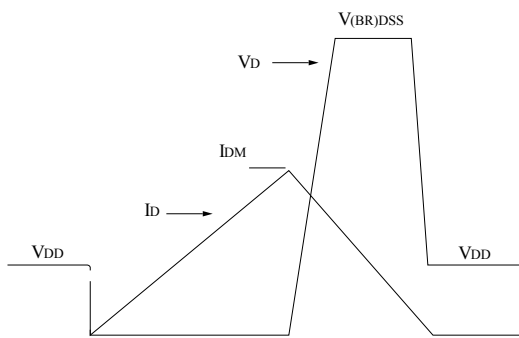
AM01469v1

**Figure 14. Test circuit for inductive load switching and diode recovery times**


AM01470v1

**Figure 15. Unclamped inductive load test circuit**


AM01471v1

**Figure 16. Unclamped inductive waveform**


AM01472v1

**Figure 17. Switching time waveform**


AM01473v1

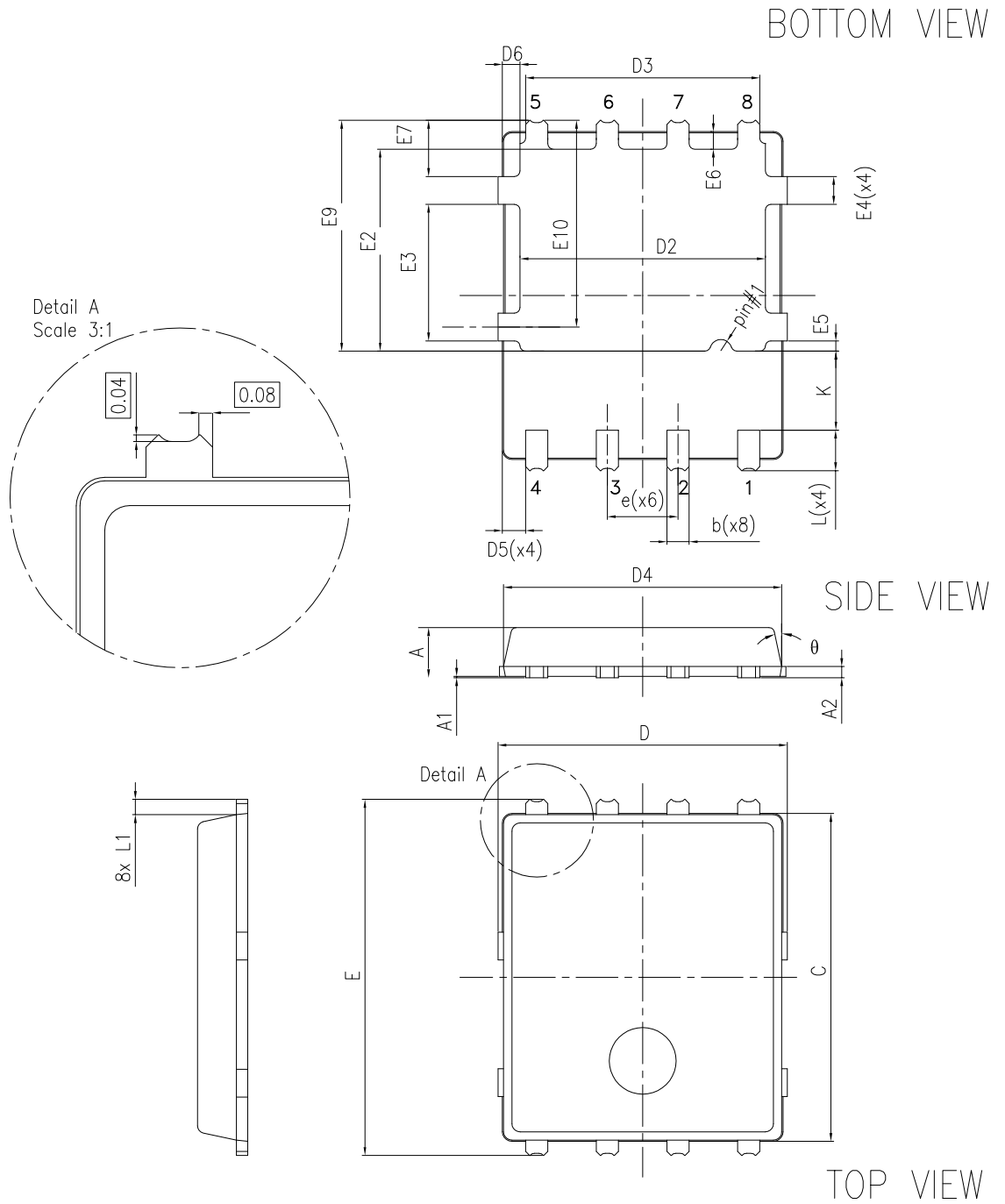


## 4 Package information

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In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK®** packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

### 4.1 PowerFLAT™ 5x6 WF type R package information

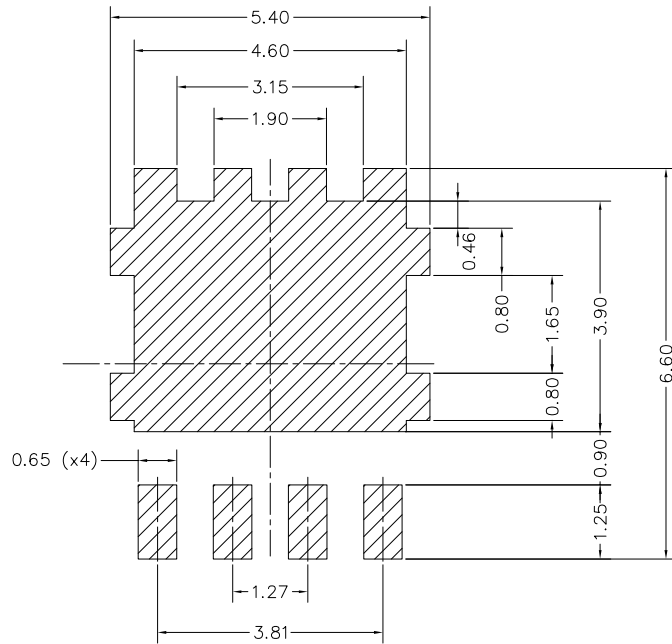
**Figure 18. PowerFLAT™ 5x6 WF type R package outline**


8231817\_R\_WF\_Rev\_18

**Table 7. PowerFLAT™ 5x6 WF type R mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
C	5.80	6.00	6.10
D	5.00	5.20	5.40
D2	4.15		4.45
D3	4.05	4.20	4.35
D4	4.80	5.00	5.10
D5	0.25	0.4	0.55
D6	0.15	0.3	0.45
e		1.27	
E	6.20	6.40	6.60
E2	3.50		3.70
E3	2.35		2.55
E4	0.40		0.60
E5	0.08		0.28
E6	0.20	0.325	0.45
E7	0.85	1.00	1.15
E9	4.00	4.20	4.40
E10	3.55	3.70	3.85
K	1.275		1.575
L	0.725	0.825	0.925
L1	0.175	0.275	0.375
θ	0°		12°

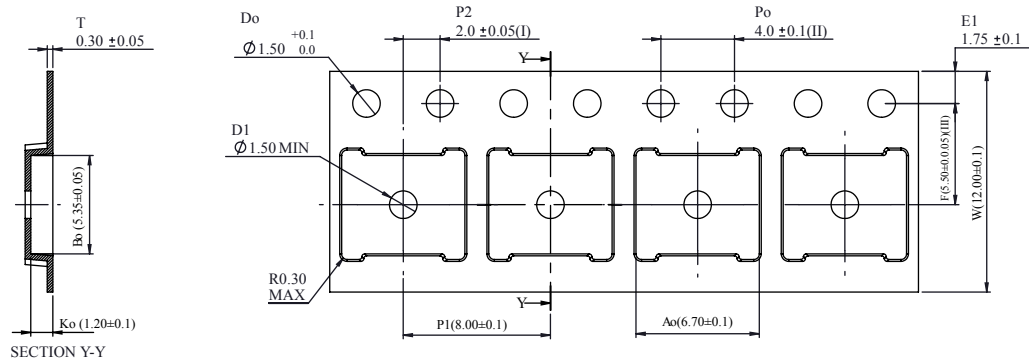
Figure 19. PowerFLAT™ 5x6 recommended footprint (dimensions are in mm)



8231817\_FOOTPRINT\_rev18

## 4.2 PowerFLAT™ 5x6 WF packing information

**Figure 20. PowerFLAT™ 5x6 WF tape (dimensions are in mm)**



- (I) Measured from centreline of sprocket hole to centreline of pocket.
- (II) Cumulative tolerance of 10 sprocket holes is  $\pm 0.20$ .
- (III) Measured from centreline of sprocket hole to centreline of pocket.

Base and bulk quantity 3000 pcs

8234350\_TapeWF\_rev\_C

**Figure 21. PowerFLAT™ 5x6 package orientation in carrier tape**

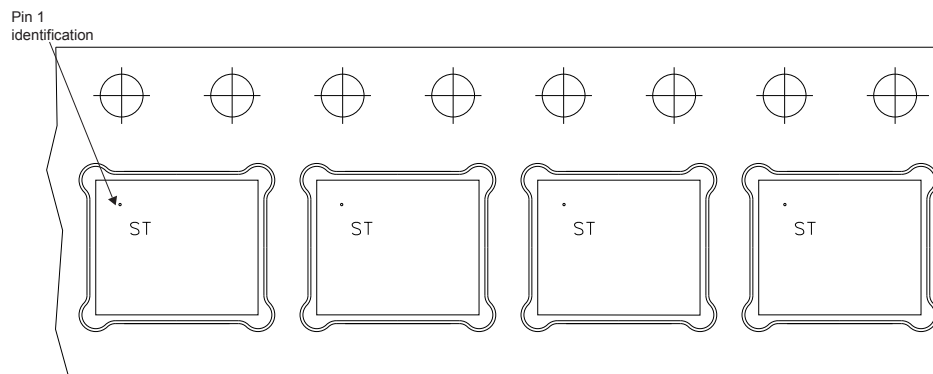
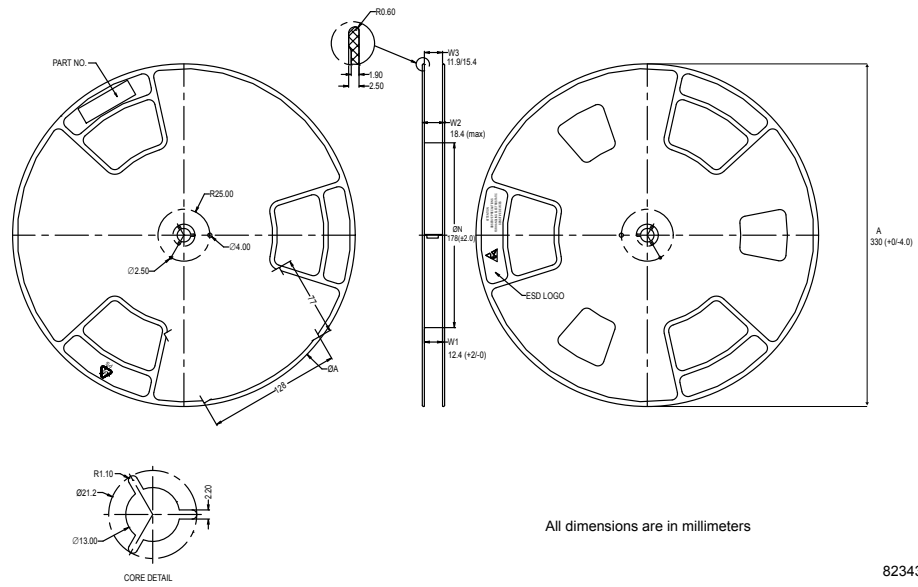


Figure 22. PowerFLAT™ 5x6 reel (dimensions are in mm)



8234350\_Reel\_rev\_C

## Revision history

**Table 8. Document revision history**

Date	Revision	Changes
26-Sep-2014	1	First release.
21-Jan-2015	2	Document status promoted from preliminary to production data. Updated <i>Section 4: Package mechanical data</i> .
03-Feb-2015	3	Updated title and features in cover page.
03-Oct-2016	4	Updated title and features in cover page. Updated <i>Table 1. Absolute maximum ratings</i> and <i>Table 3. On/off-states</i> . Changed <i>Figure 1. Safe operating area</i> and <i>Figure 2. Thermal impedance</i> .
11-Feb-2019	5	Updated <a href="#">Section 4 Package information</a> Minor text changes.

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