

P-channel 20 V, 0.0195 Ω typ., 8 A STripFET™ VII DeepGATE™ Power MOSFET in a PowerFLAT™ 2x2 package

Datasheet - production data

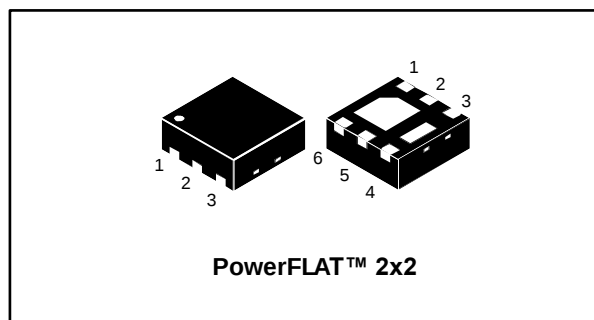
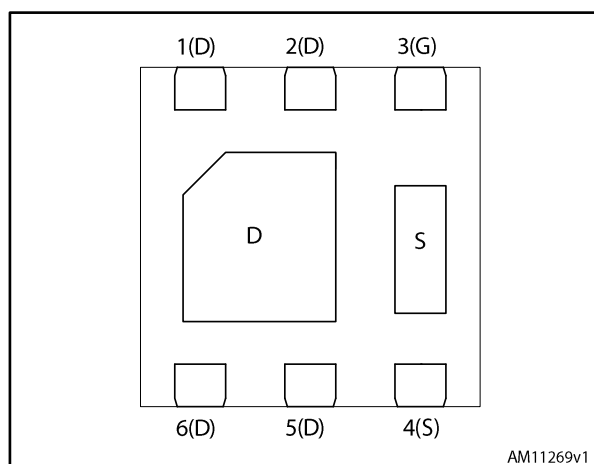


Figure 1: Internal schematic diagram



Features

Order code	V_{DS}	$R_{DS(on)max}$	I_D
STL8P2UH7	20 V	0.0225 Ω @ 4.5 V	8 A

- Extremely low on-resistance $R_{DS(on)}$
- Ultra logic level

Applications

- Switching applications

Description

This device exhibits low on-state resistance and capacitance for improved conduction and switching performance.

Table 1: Device summary

Order code	Marking	Package	Packaging
STL8P2UH7	8L2U	PowerFLAT™ 2x2	Tape and reel



For the P-channel Power MOSFET the actual polarity of the voltages and the current must be reversed.

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1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	20	V
V_{GS}	Gate-source voltage	± 8	V
I_D	Drain current (continuous) at $T_{pcb} = 25\text{ }^{\circ}\text{C}$	8	A
I_D	Drain current (continuous) at $T_{pcb} = 100\text{ }^{\circ}\text{C}$	5.3	A
$I_{DM}^{(1)}$	Drain current (pulsed)	32	A
P_{TOT}	Total dissipation at $T_{pcb} = 25\text{ }^{\circ}\text{C}$	2.4	W
T_{stg}	Storage temperature	- 55 to 150	$^{\circ}\text{C}$
T_j	Max. operating junction temperature	150	$^{\circ}\text{C}$

Notes:

⁽¹⁾Pulse width limited by safe operating area

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb max	52	$^{\circ}\text{C/W}$

Notes:

⁽¹⁾When mounted on 1inch² FR-4 board, 2 oz Cu



For the P-channel Power MOSFET the actual polarity of the voltages and the current must be reversed.

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 4: On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	V _{GS} = 0, I _D = 250 µA	20			V
I _{DSS}	Zero gate voltage drain current	V _{GS} = 0, V _{DS} = 20 V			1	µA
I _{GSS}	Gate-body leakage current	V _{DS} = 0, V _{GS} = ± 5 V			± 5	µA
V _{GS(th)}	Gate threshold voltage	V _{DS} = V _{GS} , I _D = 250 µA	0.4		1	V
R _{DS(on)}	Static drain-source on- resistance	V _{GS} = 4.5 V, I _D = 4 A		0.0195	0.0225	Ω
		V _{GS} = 2.5 V, I _D = 4 A		0.02	0.025	Ω
		V _{GS} = 1.8 V, I _D = 4 A		0.036	0.043	Ω
		V _{GS} = 1.5 V, I _D = 4 A		0.05	0.085	Ω

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C _{iss}	Input capacitance	V _{GS} = 0, V _{DS} = 16 V, f = 1 MHz	-	2390	-	pF
C _{oss}	Output capacitance		-	220	-	pF
C _{rss}	Reverse transfer capacitance		-	188	-	pF
Q _g	Total gate charge	V _{DD} = 16 V, I _D = 8 A, V _{GS} = 4.5 V	-	22	-	nC
Q _{gs}	Gate-source charge		-	4.2	-	nC
Q _{gd}	Gate-drain charge		-	3.6	-	nC



For the P-channel Power MOSFET the actual polarity of the voltages and the current must be reversed.

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
t _{d(on)}	Turn-on delay time	V _{DD} = 16 V, I _D = 8 A, R _G = 1 Ω, V _{GS} = 4.5 V	-	12.5	-	ns
t _r	Rise time		-	30.5	-	ns
t _{d(off)}	Turn-off delay time		-	128	-	ns
t _f	Fall time		-	84.5	-	ns

Table 7: Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		8	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		32	A
$V_{SD}^{(2)}$	Forward on voltage	$V_{GS} = 0, I_{SD} = 1 \text{ A}$	-		1	V
t_{rr}	Reverse recovery time	$V_{DD} = 16 \text{ V}$ $di/dt = 100 \text{ A}/\mu\text{s},$ $I_{SD} = 1 \text{ A}$	-	15.8		ns
Q_{rr}	Reverse recovery charge		-	5.9		nC
I_{RRM}	Reverse recovery current		-	0.7		A

Notes:

⁽¹⁾ Pulse width limited by safe operating area.

⁽²⁾ Pulsed: pulse duration = 300 μs , duty cycle 1.5%



For the P-channel Power MOSFET the actual polarity of the voltages and the current must be reversed.

2.1 Electrical characteristics (curves)

Figure 2: Safe operating area

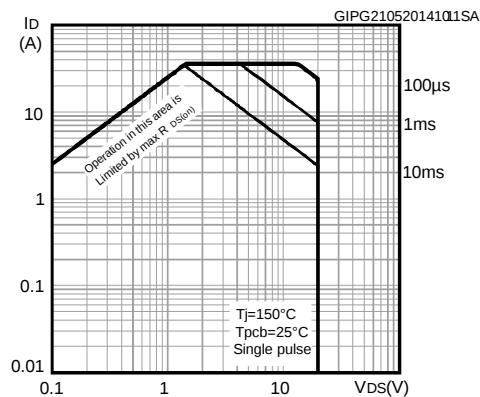


Figure 3: Thermal impedance

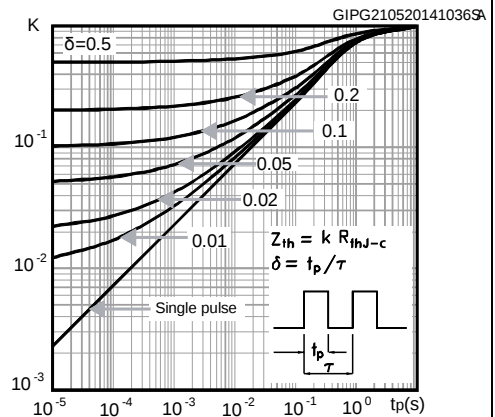


Figure 4: Output characteristics

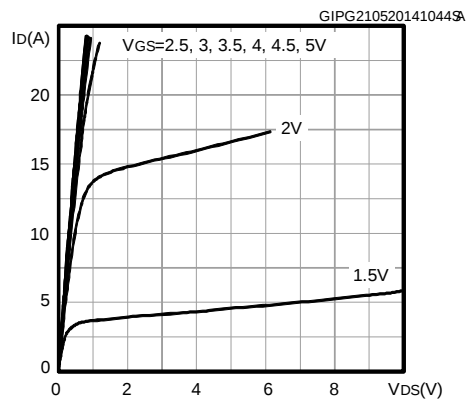


Figure 5: Transfer characteristics

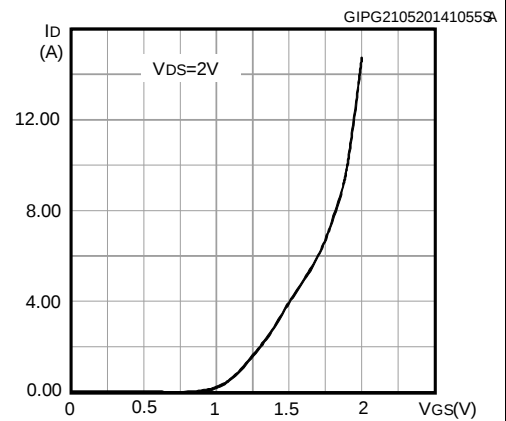


Figure 6: Gate charge vs gate-source voltage

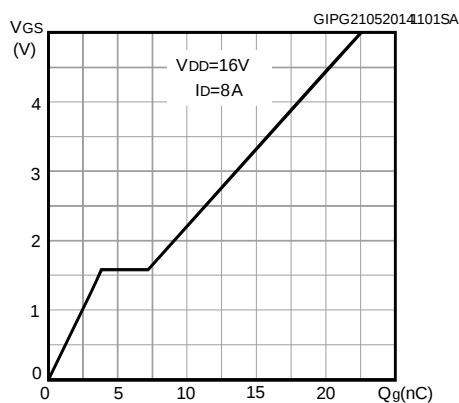


Figure 7: Static drain-source on-resistance

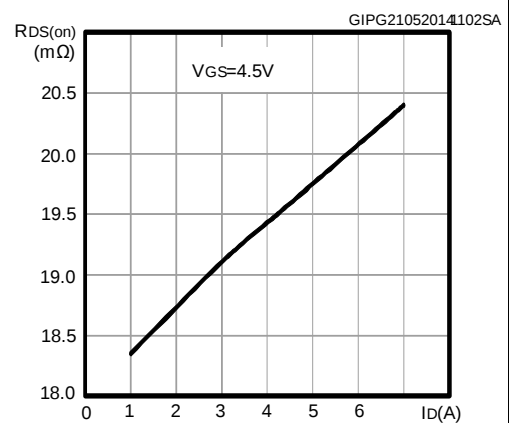


Figure 8: Capacitance variations

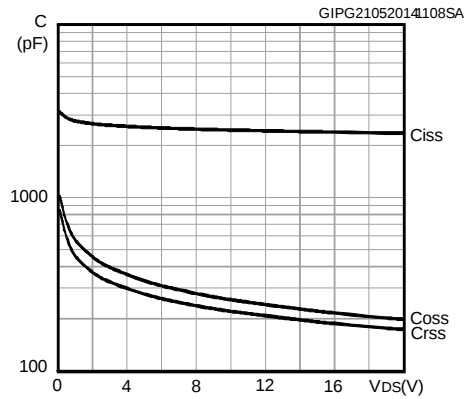


Figure 9: Normalized gate threshold voltage vs temperature

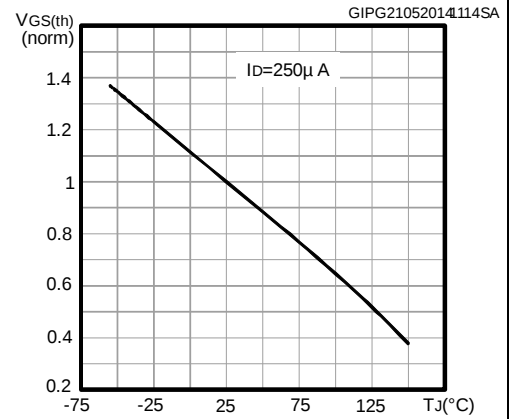


Figure 10: Normalized on-resistance vs temperature

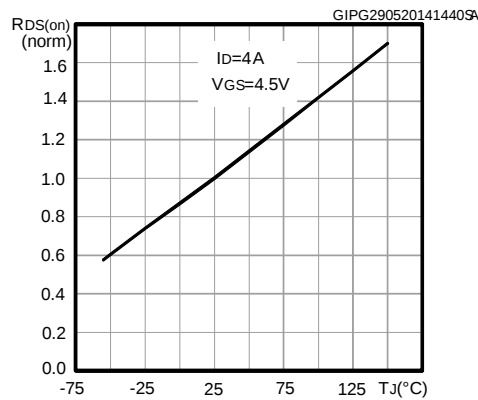


Figure 11: Normalized V(BR)DSS vs temperature

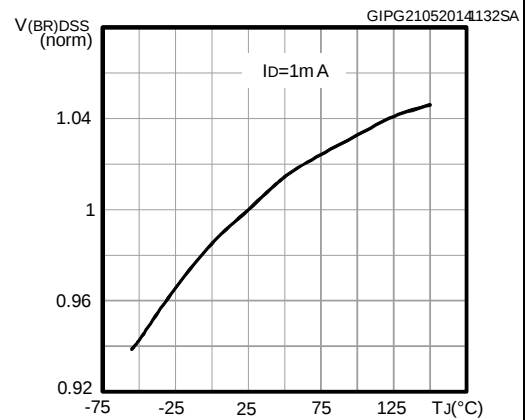
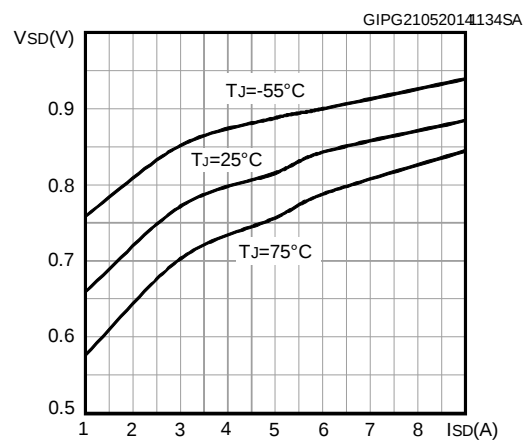


Figure 12: Source-drain diode forward characteristics



3 Test circuits

Figure 13: Switching times test circuit for resistive load

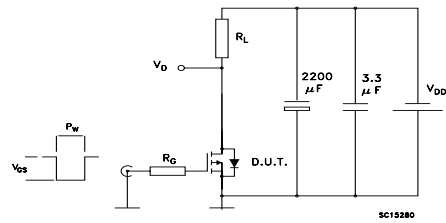


Figure 14: Gate charge test circuit

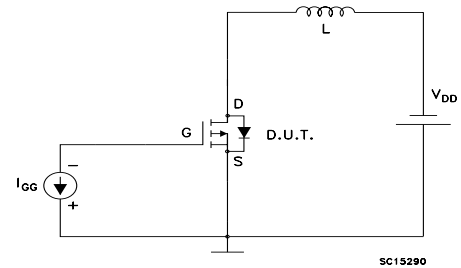
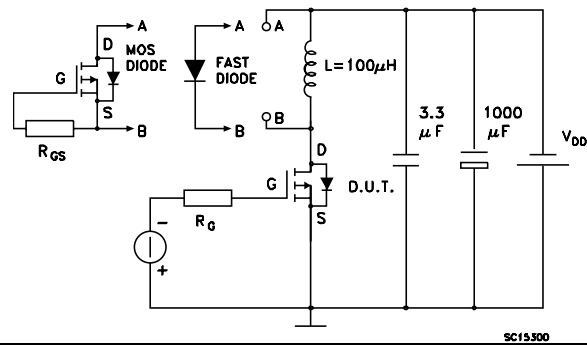


Figure 15: Test circuit for inductive load switching and diode recovery times



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: **www.st.com**. ECOPACK[®] is an ST trademark.

4.1 PowerFLAT™ 2x2 package mechanical data

Figure 16: Drawing dimension PowerFLAT™ 2 x 2

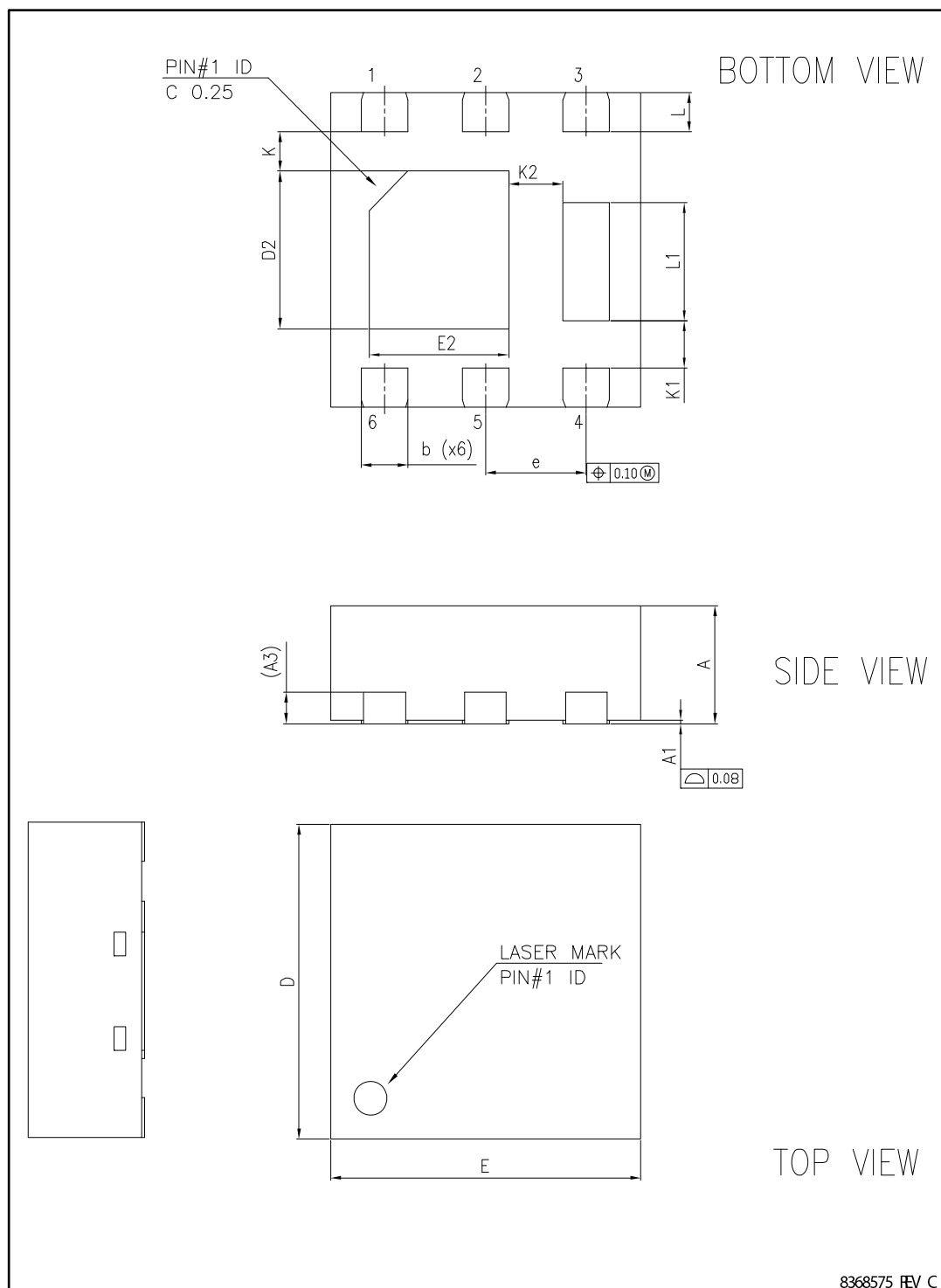
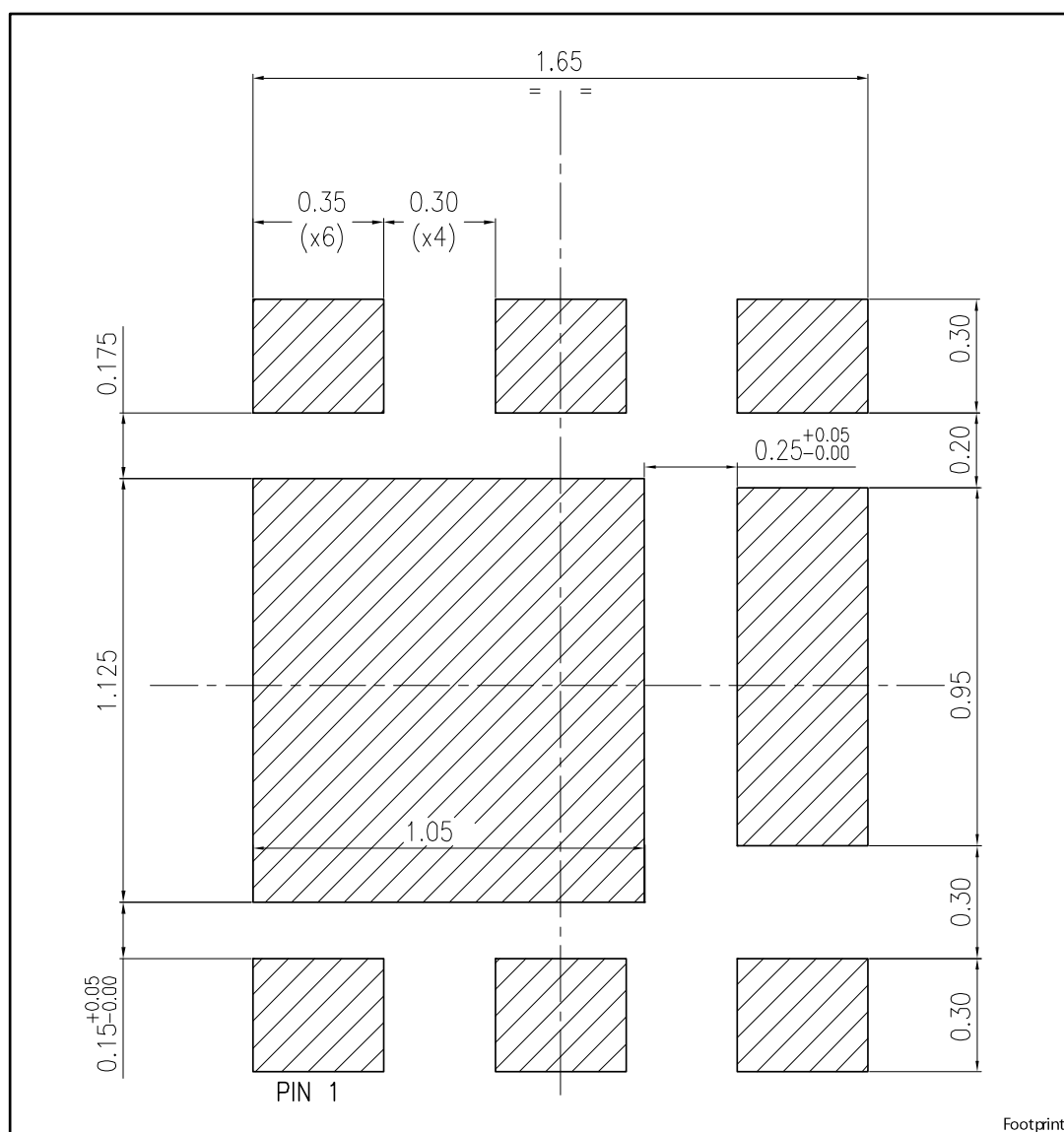


Table 8: PowerFLAT™ 2 x 2 mechanical data

Dim.	mm.		
	Min.	Typ.	Max.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.20	
b	0.25	0.30	0.35
D	1.90	2.00	2.10
E	1.90	2.00	2.10
D2	0.90	1.00	1.10
E2	0.80	0.90	1.00
e	0.55	0.65	0.75
K	0.15	0.25	0.35
K1	0.20	0.30	0.40
K2	0.25	0.35	0.45
L	0.20	0.25	0.30
L1	0.65	0.75	0.85

Figure 17: PowerFLAT™ 2 x 2 footprint



5 Revision history

Table 9: Document revision history

Date	Revision	Changes
20-Aug-2013	1	First release.
04-Jun-2014	2	Document status promoted from preliminary data to production data Modified: title Modified: $R_{DS(on)}$ max value in cover page Modified: $R_{DS(on)}$ (typical and maximum) values in Table 4: "On /off states" Modified: the entire typical values in Table 5: "Dynamic" , Table 6: "Switching times" and Table 7: "Source drain diode" Added Section 8.1: "Electrical characteristics (curves)" Minor text changes

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