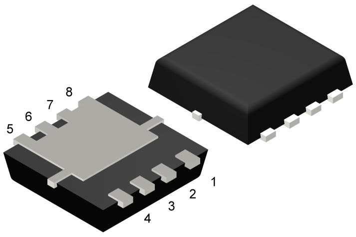
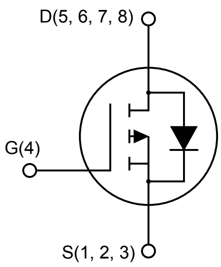
STL9P4LF6AG

Datasheet

Automotive P-channel enhancement mode Power MOSFET STripFET F6 -40 V, -8 A in a PowerFLAT 3.3x3.3 package



PowerFLAT 3.3x3.3



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STL9P4LF6AG	-40 V	26 mΩ	-8 A

- AEC-Q101 qualified
- Very low on-resistance
- Very low gate charge
- High avalanche ruggedness
- Low gate drive power loss
- Logic level

Applications

- Switching applications

Description

This device is a P-channel Power MOSFET developed using the STripFET F6 technology, with a new trench gate structure. The resulting Power MOSFET exhibits very low $R_{DS(on)}$ in all packages.

Product status link
STL9P4LF6AG

Product summary	
Order code	STL9P4LF6AG
Marking	9P4LF
Package	PowerFLAT 3.3x3.3
Packing	Tape and reel

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	-40	V
V_{GS}	Gate-source voltage	±18	V
I_D (1)	Drain current (continuous) at T_C = 25 °C	-8	A
	Drain current (continuous) at T_C = 100 °C	-5	
I_D (2)	Drain current (continuous) at T_C = 25 °C	-31	A
	Drain current (continuous) at T_C = 100 °C	-20	
I_{DM} (1)(3)	Drain current (pulsed)	-32	A
P_{TOT} (1)	Total power dissipation at T_C = 25 °C	2.9	W
P_{TOT} (2)	Total power dissipation at T_C = 25 °C	50	W
T_{stg}	Storage temperature	-55 to 150	°C
T_J	Maximum junction temperature		

1. *The value is rated according to $R_{thj-pcb}$.*
2. *The value is rated according to R_{th-jC}.*
3. *Pulse width limited by safe operating area.*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case max.	2.5	°C/W
R_{thJB} (1)	Thermal resistance, junction-to-board, single operation	42.8	°C/W

1. *When mounted on FR-4 board of 1 inch², 2oz Cu, steady state.*

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 3. Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = -250 µA	-40			V
I_{DSS}	Zero gate voltage Drain current	V_{GS} = 0 V, V_{DS} = -40 V			-1	µA
		V_{GS} = 0 V, V_{DS} = -40 V, T_C = 125 °C			-10	
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = -18 V			-100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = -250 µA	-1		-2.5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = -10 V, I_D = -4 A		21	26	mΩ
		V_{GS} = -4.5 V, I_D = -4 A		28	35	

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = -25 V, f = 1 MHz, V_{GS} = 0 V	-	2540	-	pF
C_{oss}	Output capacitance		-	254	-	pF
C_{rss}	Reverse transfer capacitance		-	173	-	pF
Q_g	Total gate charge	V_{DS} = -20 V, I_D = -8 A, V_{GS} = -4.5 V (see Figure 13. Gate charge test circuit)	-	48	-	nC
Q_{gs}	Gate-source change	V_{DD} = -20 V, I_D = -8 A, V_{GS} = -4.5 V	-	6.8	-	nC
Q_{gd}	Gate-drain change	V_{DD} = -20 V, I_D = -8 A, V_{GS} = -4.5 V	-	7.8	-	

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

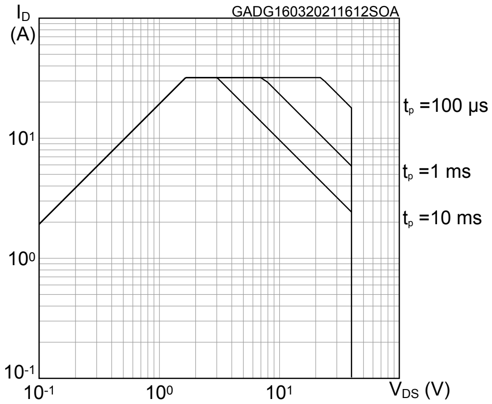


Figure 2. Thermal impedance

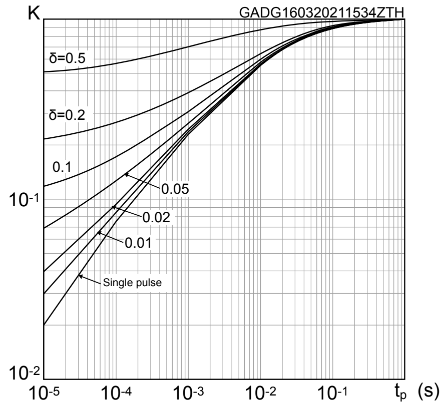


Figure 3. Output characteristics

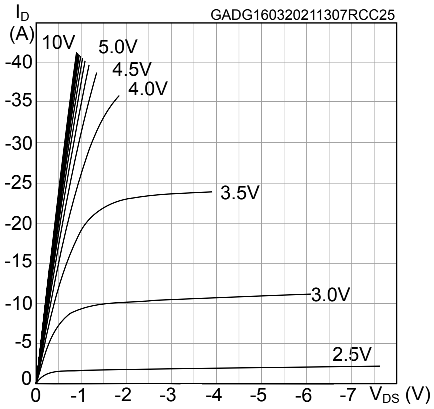


Figure 4. Transfer characteristics

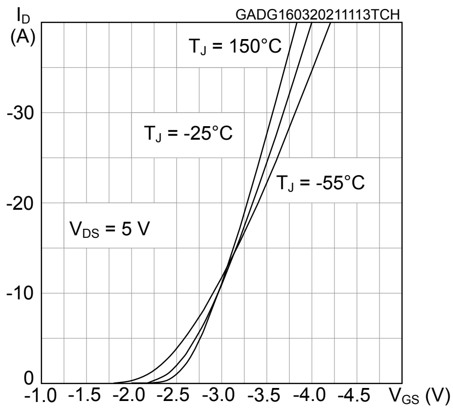


Figure 5. Gate charge vs gate-source voltage

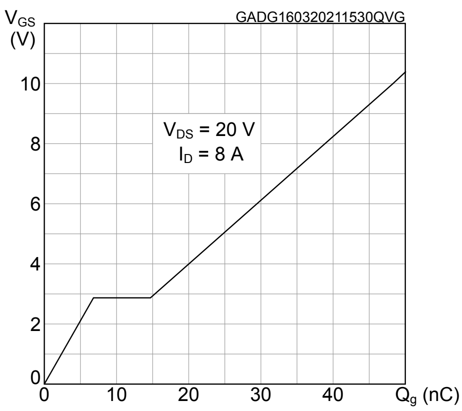


Figure 6. Typical static drain-source on-resistance

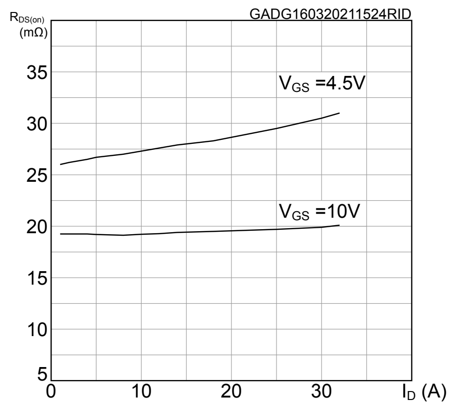


Figure 7. Capacitance variations

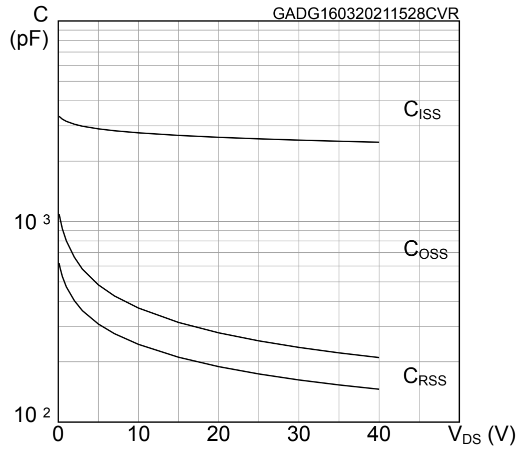


Figure 8. Normalized gate threshold voltage vs temperature

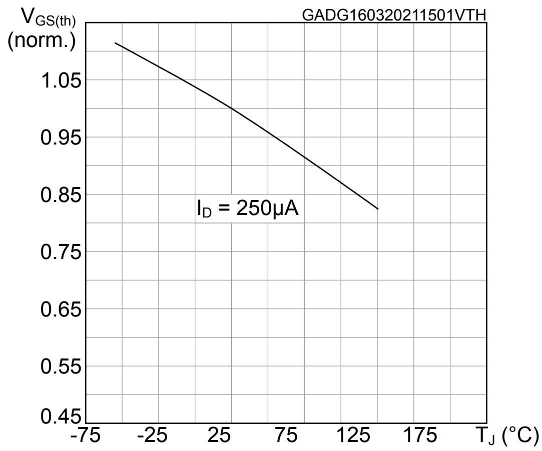


Figure 9. Normalized on-resistance vs temperature

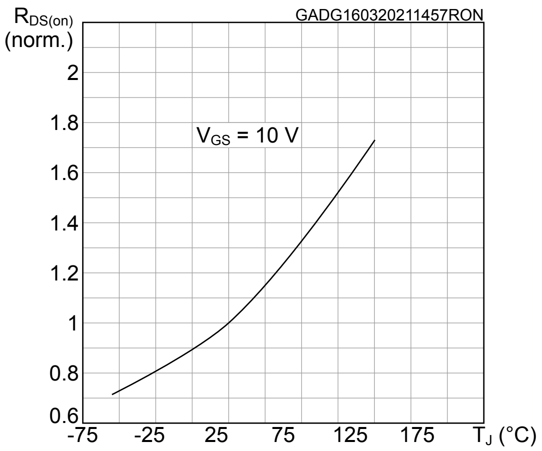


Figure 10. Normalized $V_{(BR)DSS}$ vs temperature

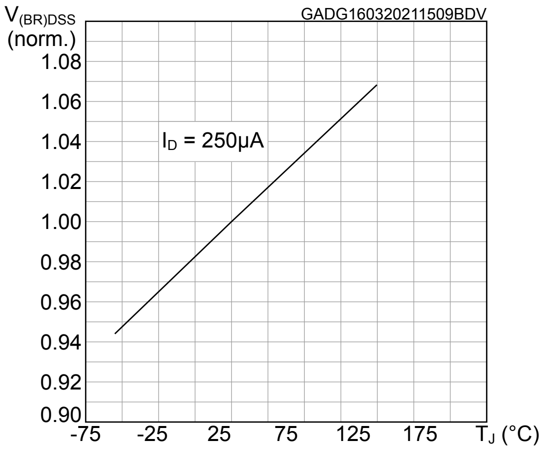
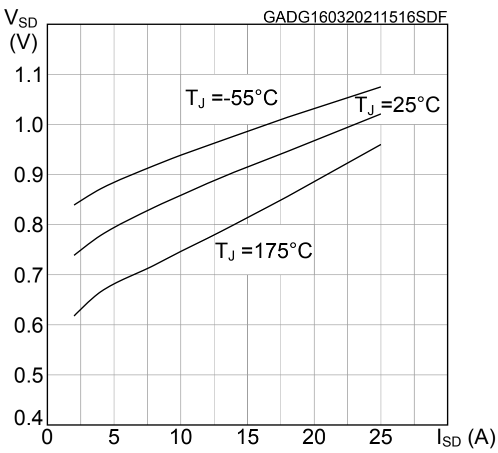


Figure 11. Source-drain diode forward characteristics



3 Test circuits

Figure 12. Switching times test circuit for resistive load

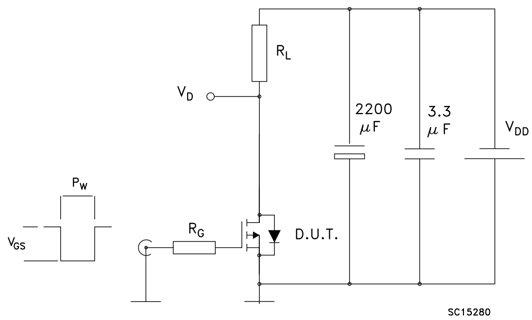


Figure 13. Gate charge test circuit

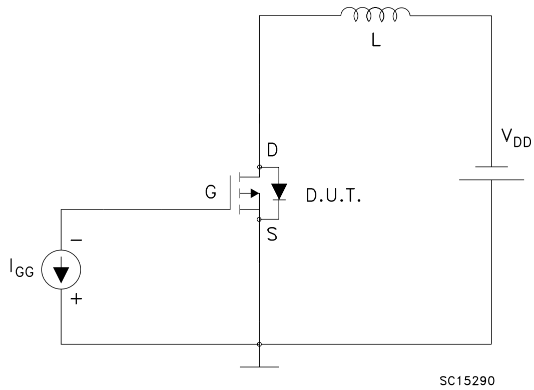
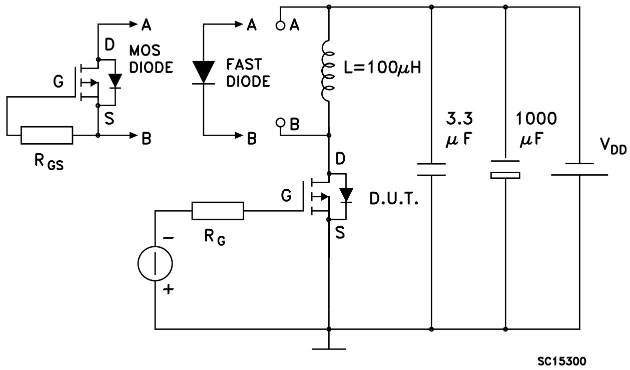


Figure 14. Test circuit for inductive load switching and diode recovery times



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 PowerFLAT 3.3x3.3 package information

Figure 15. PowerFLAT 3.3x3.3 package outline

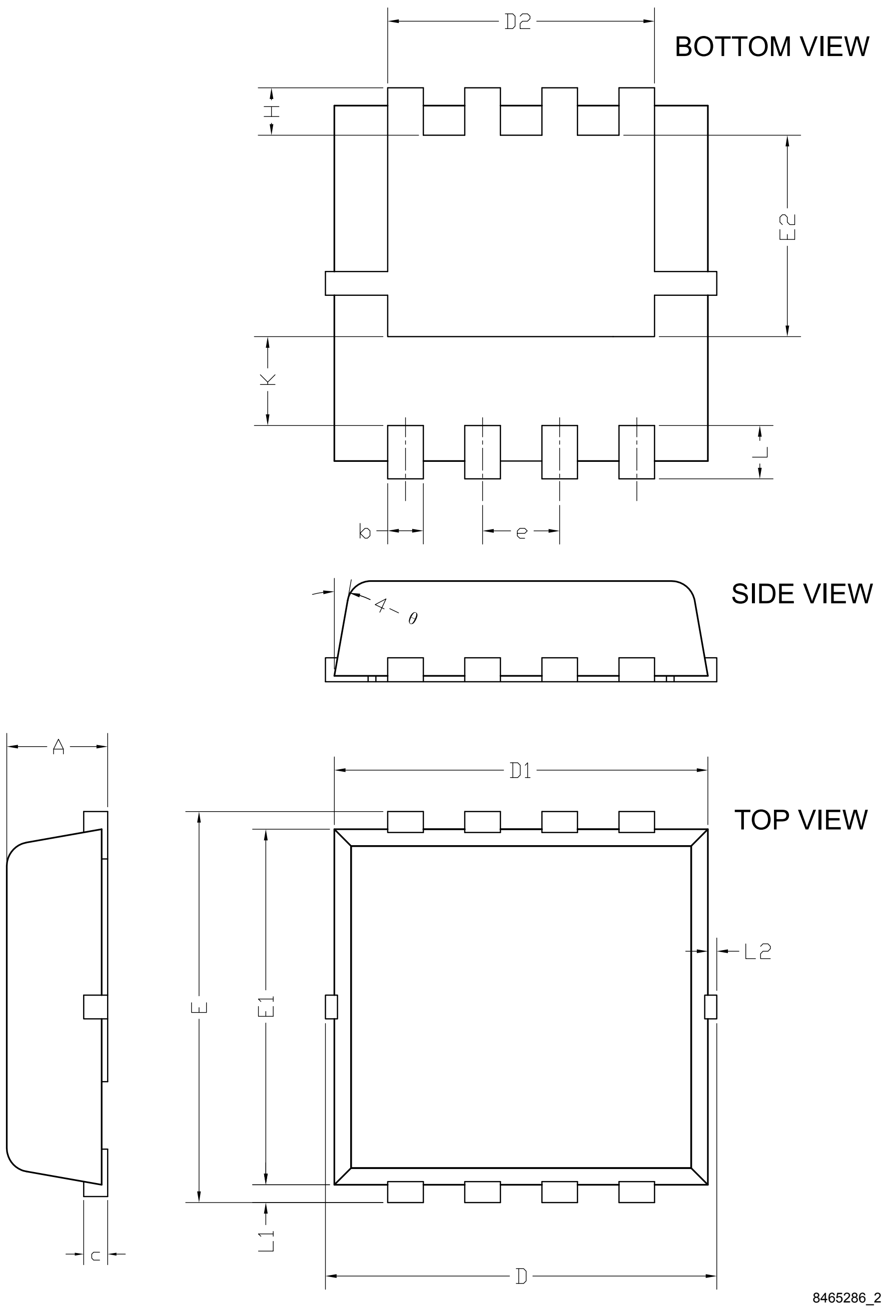
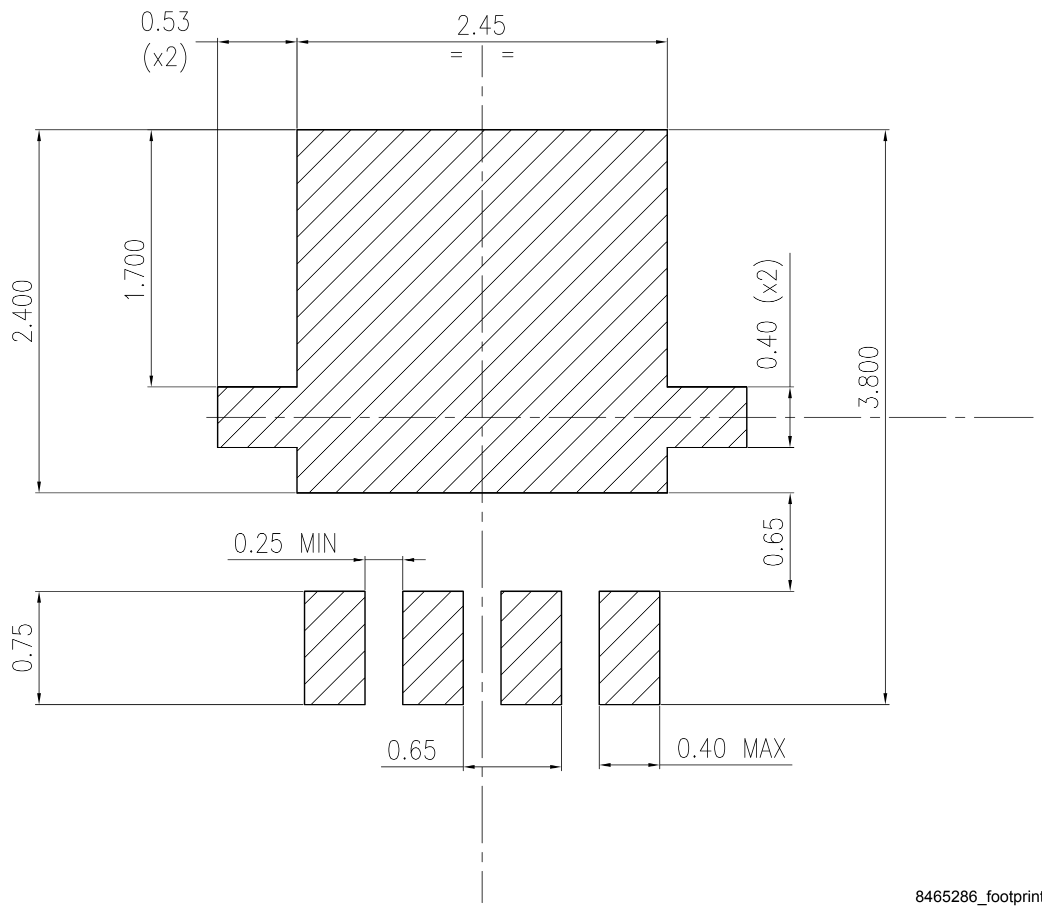


Table 5. **PowerFLAT 3.3x3.3 package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	0.70	0.80	0.90
b	0.25	0.30	0.39
c	0.14	0.15	0.20
D	3.10	3.30	3.50
D1	3.05	3.15	3.25
D2	2.15	2.25	2.35
e	0.55	0.65	0.75
E	3.10	3.30	3.50
E1	2.90	3.00	3.10
E2	1.60	1.70	1.80
H	0.25	0.40	0.55
K	0.65	0.75	0.85
L	0.30	0.45	0.60
L1	0.05	0.15	0.25
L2			0.15
θ	8°	10°	12°

Figure 16. PowerFLAT 3.3x3.3 recommended footprint (dimensions are in mm)



8465286_footprint

Revision history

Table 6. **Document revision history**

Date	Revision	Changes
01-Jul-2020	1	First release.
28-Apr-2021	2	Added Section 2.1 Electrical characteristics (curves). Minor text changes.

Contents