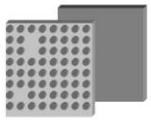
STLC2690

Bluetooth™ and FM transceiver system-on-chip

Datasheet - production data



WLCSP61R8

Features

- WLCSP 0.6 mm high, 0.4 mm pitch, lead-free/RoHs compliant, 61 pins
- 10 external components: 5 decoupling capacitors on the power supply, 1 B-BPF for Bluetooth, 1 inductor and 3 capacitors for FM RX
- PCB footprint < 36 mm^2
- Clocks
  - Fast clock input (digital or sine wave) at 13, 16, 16.8, 19.2, 26, 32, 33.6, 38.4, 52 MHz
  - Slow clock input at 32, 32.768 kHz
  - Direct external crystal input
- Power supply
  - Single power supply with internal regulators
- 1.65 V to 1.95 V I/O systems
- Various on-chip auto calibration features (VCO, Filters, …)

Description

The STLC2690 combines Bluetooth and FM transceiver functionality on a single chip and is fully optimized for mobile applications such as mobile phones, smart phones, PDAs and portable media players. The required board space has been minimized, power consumption levels are targeted for battery powered devices and the integration allows a cost effective solution. Amongst others the reduction of external components enables manufacturers to easily and fast integrate the STLC2690 on their product to enable a short time to market. Compared to its successful predecessor, the STLC2593, the STLC2690 is a system on chip device, it adds an FM transmitter, an audio processor and A2DP encapsulation and further optimizes in terms of RF performance and cost.

Table 1: Device summary

Order code	Package	Packing
STLC2690WTR	WLCSP61	Tape & Reel

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1 Introduction

The STLC2690 is a system-on-chip Bluetooth V3.0 transceiver and FM radio transceiver. The chip is packed in Wafer Level Chip Scale Package (WLCSP) of 0.6 mm high, 0.4 mm pitch.

The Bluetooth subsystem is the successor of the STLC2500D, a field-proven, single chip ROM-based Bluetooth solution for applications requiring integration up to HCI level. The STLC2690 supports in addition A2DP mediapacket encapsulation and SBC encoding/decoding. This allows to offload those functions from the Host for several use cases. Patch RAM is available, enabling multiple patches/upgrades and fast time to volume. The main interfaces are UART or SPI for HCI transport, PCM or I2S for voice and a WLAN coexistence interface. The radio has been designed specifically for single chip requirements, for low power and minimum BOM count.

The FM radio transceiver contains both a broadcast FM radio tuner and a broadcast FM radio transmitter for portable applications with worldwide FM band support. (De)multiplexing and (de)modulation are performed in a digital data path. A small embedded microcontroller manages the flexibility of the data path and the DSP parameters and takes care of the overall control of the transceiver. This microcontroller is also used for transmission and reception of the European Radio Data System (RDS) and the North American Radio Broadcast Data System (RBDS), including all required symbol decoding, block synchronization, error detection, and error correction functions. The FM can be controlled by the Host via a dedicated I2C interface or via the Bluetooth HCI interface. A Host-level API is offered in order to facilitate integration of the FM driver on the Host. Also a low-level API is supported.

The Bluetooth transceiver and FM transceiver are integrated on the same silicon, and they share at top-level power supplies, clocks and reset control. The chip integrates several regulators to generate the internally needed voltages from the Host platform supply input. The STLC2690 supports several use cases using simultaneous BT and FM and exchanging audio between the two subsystems.

For the Bluetooth transceiver, 5 decoupling capacitors and a band-pass filter are required as external BOM. For the FM transmitter, no external components are required, provided a loop antenna is used. For the FM receiver, 1 inductor and 3 capacitors are required. This results in a required PCB footprint smaller than 36 mm^2 (using 0201 components where possible and with a 0.3 mm spacing rule). The FM antenna matching network, which depends on the specific antenna implementation, is included in this footprint.

Bluetooth features

- Bluetooth™ specification compliance: V3.0
- Specific BT V3.0 features
  - Enhanced power control
  - Read encryption key size
- Adaptive frequency hopping (AFH)
- Channel quality driven data rate (CQDDR)
- Transmit Power
  - Power Class 2 and power Class 1.5 (above 4 dBm)
  - Programmable output power
- HCI
  - HCI H4 Transport Layer on UART and SPI
  - HCI proprietary commands (e.g. peripherals control)
  - Single HCI command for patch/upgrade download

  - (e)SCO over HCI
- Pitch-period error concealment (PPEC)
- Efficient and flexible support for WLAN coexistence scenarios
- Low power consumption
  - Ultra low power architecture with 3 different low-power levels
  - Deep sleep modes, including host-power saving feature
  - Dual wakeup mechanism
- Communication interfaces
  - UART (up to 4 MHz), SPI (up to 52 MHz), PCM/I2S, I2C
  - Up to 22 additional flexibly programmable GPIOs
  - External interrupts possible through the GPIOs
- Main processor
  - ARM7TDMI CPU
  - On-chip RAM, including provision for patches
  - On-chip ROM, preloaded with SW up to HCI and A2DP mediapacket encapsulation
- CoProcessor
  - Audio processor including RAM and ROM
  - ROM preloaded with SBC en-/decoding
- Ciphering support up to 128 bits key

FM receiver features

- Worldwide FM band (65.9 - 108 MHz)
- RDS/RBDS
- State of the art receiver sensitivity
- Excellent receiver selectivity for audio and RDS
- DSP-demodulation
- Adaptive signal processing, to provide best audio quality versus received signal quality or in-band blockers.
- Embedded microcontroller to control flexible DSP, to handle and (de)code RDS messages, supporting high-level and low level API
- Ultra fast checking for AF
- Analog and digital audio output
- Dual RF input with embedded FM TX/RX antenna switch to optimize for wire antennas and integrated antennas

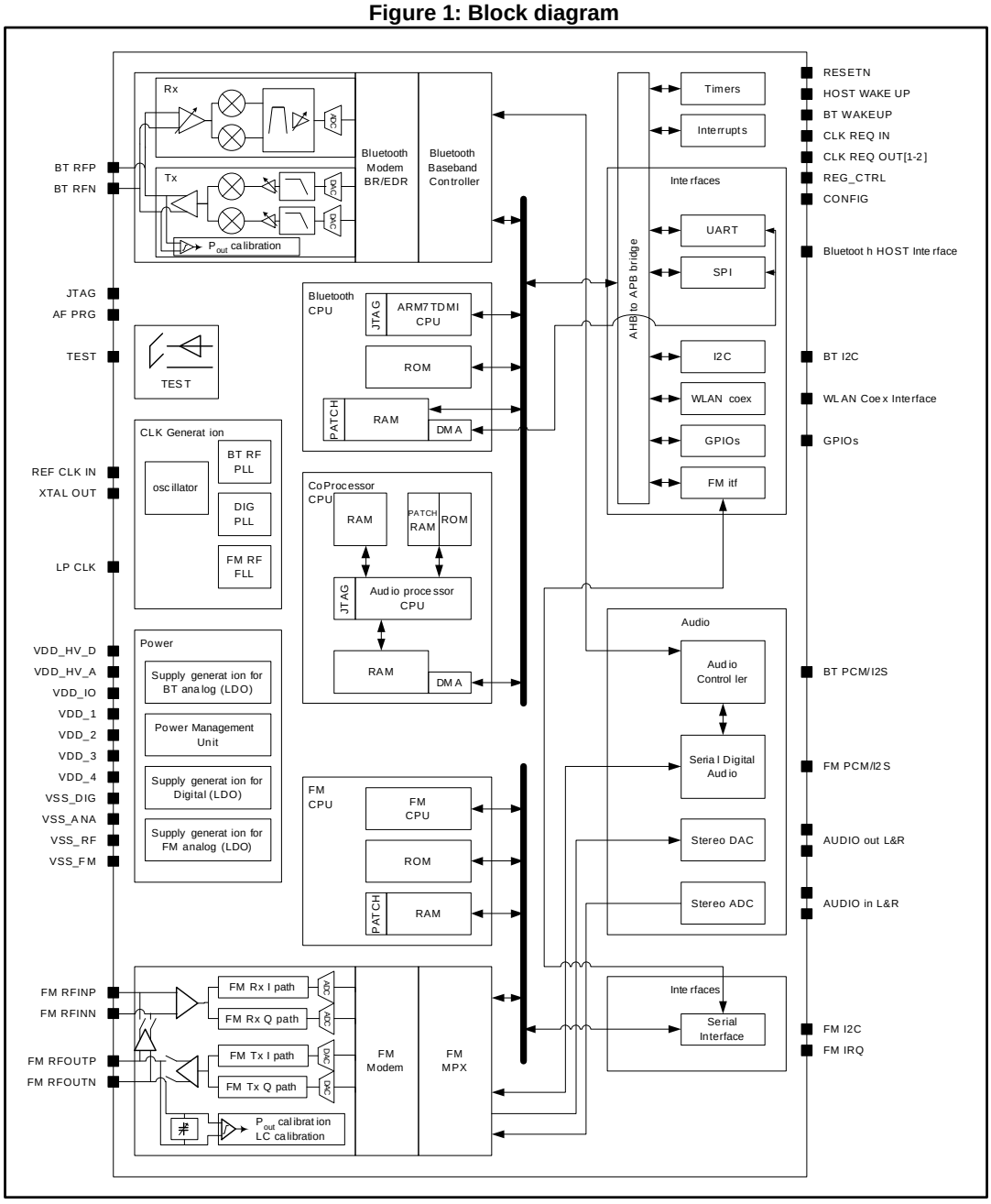
FM transmitter features

- Worldwide FM band (76 - 108 MHz)
- RDS/RBDS
- High output power (120 dBµVpdiff) linear transmitter
- Dual TX channel mode using AF list, with programmable separation
- SureTune™ to automatically select the optimal transmit frequency
- Embedded filtering for coexistence in mobile handset
- RF output optimized for integrated antennas
- Programmable AGC for optimized frequency deviation
- Programmable limiter to prevent over-modulation
- Highly flexible DSP (shared with FM RX)
- Embedded microcontroller (shared with FM RX)
- Analog and digital audio input

2 Generic description

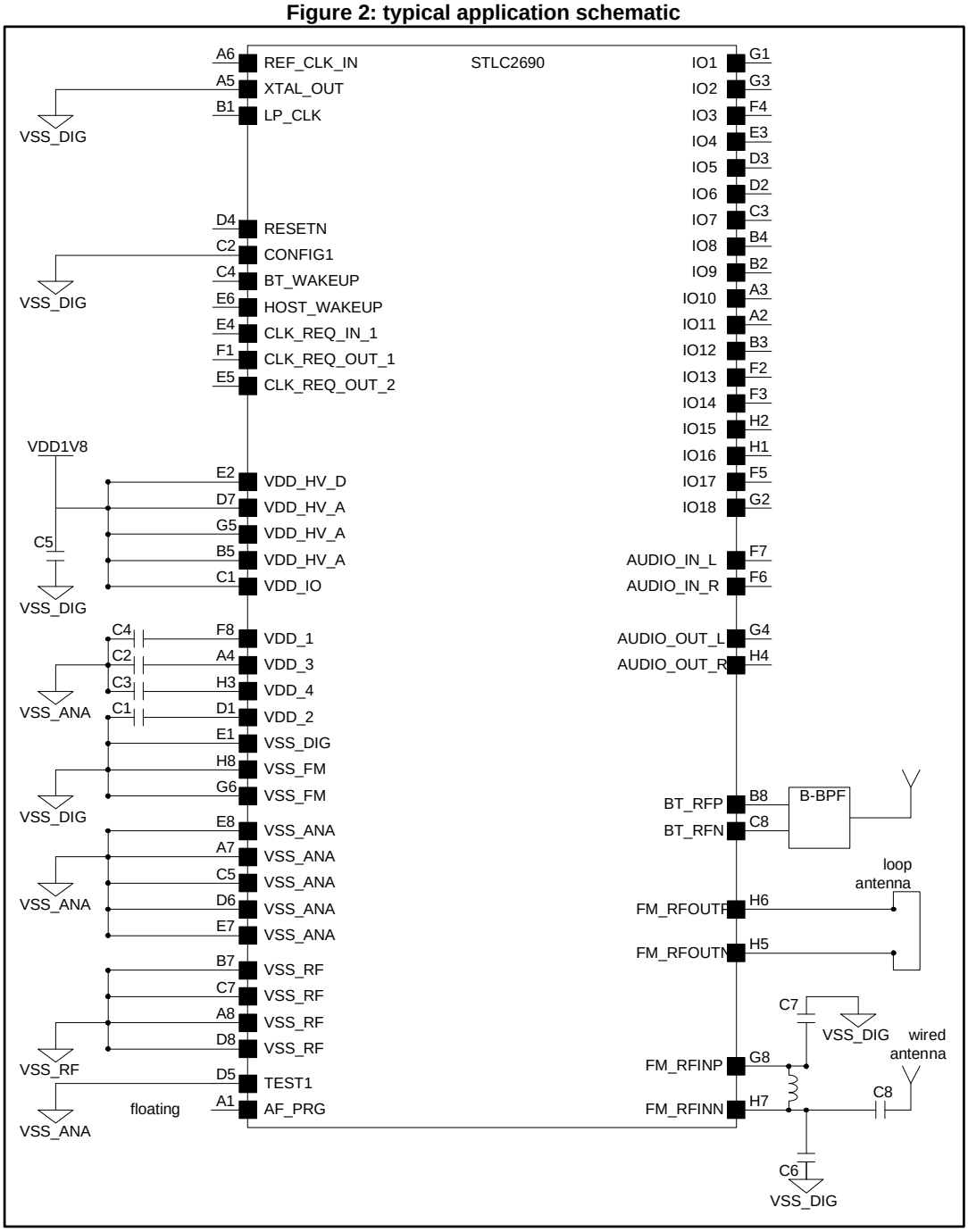
2.1 Block diagram

Figure 1: Block diagram



2.2 Application schematic

Figure 2: typical application schematic



For values of the components, refer to the HW manual.

Note that the application schematic shown is for a certain configuration. Other configurations are possible:

- The fast clock is provided from a digital or analog clock signal. This clock can also be generated from an external crystal directly connected to the chip, see *Section 3.6: "Clocks"*.

- FM RX is connected to a wired antenna. It can also be connected to the loop antenna, see *Section 5.2.1: "Dual RF input with RX/TX antenna switch"* for more details.
- VDD_HV_D, VDD_HV_A and VDD_IO are connected to the platform supply. Other configurations are possible, see *Section 3.5: "Power supply"*.
- The control signals and digital interfaces are not shown in the application schematic, since they depend on which digital interfaces are used in the application. See *Section 3.4: "Pinout"* and *Section 3.5: "Power supply"*.

2.3 Electrical data

VDD_HV_x means VDD_HV_A and VDD_HV_D.

2.3.1 Absolute maximum ratings

The absolute maximum rating (AMR) corresponds to the maximum value that can be applied without leading to instantaneous or very short-term unrecoverable hard failure (destructive breakdown).

Table 2: Absolute maximum ratings

Symbol	Parameter	Min.	Max.	Unit
VDD_HV_x	Core supply voltages (in case of pre-regulated power supply from the platform)	-0.3	2.5	V
VDD_IO	Supply voltage I/O	-0.3	2.5	V
Vin	Input voltage on any digital pin	-0.3	2.5	V
Vssdiff	Maximum voltage difference between different types of Vss pins.	-0.3	0.3	V
Tstg	Storage temperature	-65	+150	°C

2.3.2 Operating ranges

Operating ranges define the limits for functional operation and parametric characteristics of the device. Functionality outside these limits is not guaranteed.

Table 3: Operating ranges

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_{amb}	Operating ambient temperature	-40	25	+85	°C
VDD_HV_x	Core supply voltages (in case of pre-regulated power supply from the platform)	1.65	1.8	1.95	V
VDD_IO	I/O supply voltage	1.65	1.8	1.95	V

2.3.3 I/O specifications

The I/Os comply with the EIA/JEDEC standard JESD8-B.

Table 4: DC input specification

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IL}	Low level input voltage	-0.2		0.35 * VDD_IO	V
V_{IH}	High level input voltage	0.65 * VDD_IO		(VDD_IO + 0.2) and (≤ 2.0)	V

Symbol	Parameter	Min.	Typ.	Max.	Unit
C_{in}	Input capacitance, including package(1)			5	pF
R_{pu}	Pull-up equivalent resistance (with V_{in} = 0 V)		50		kΩ
R_{pd}	Pull-down equiv. resistance (with V_{in} = VDD_IO)		50		kΩ
V_{hyst}	Schmitt trigger hysteresis	150			mV

Notes:

(1) Typical input capacitance without package is 0.9 pF.

Table 5: DC output specification

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{OL}	Low level output voltage	Id = X(1) mA			0.2	V
V_{OH}	High level output voltage	Id = X(1) mA	VDD_IO - 0.2			V

Notes:

(1)X is the source/sink current under worst-case conditions according to the drive capabilities (see *Section 3.4.1: "Pinout"*).

2.3.4 Clock specifications

For more details on the clocks see *Section 3.6: "Clocks"*.

Table 6: Fast clock supported frequencies

Symbol	Parameter	Values	Unit
F_{IN}	Clock input frequency list	13, 16, 16.8, 19.2, 26, 32, 33.6, 38.4, 52	MHz

Table 7: Fast clock overall specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
F_{INTOL}	Tolerance on input frequency	-20		20	ppm

Table 8: Fast clock, sine wave specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
VPP	Peak to peak voltage range	0.2	0.5	1.8	V
NH	Total harmonic content of input signal			-25	dBc
ZINRe	Real part of parallel input impedance at pin	30	100		kΩ
ZINIm	Imaginary part of parallel input impedance at pin		2	4.7	pF
ZIDRe	Change in real part of parallel input impedance at pin, when changing mode (expressed in equivalent parallel resistance added or removed)	150			kΩ
ZIDim	Change in imaginary part of parallel input impedance at pin, when changing mode (expressed in equivalent parallel capacitance added or removed)			500	fF
	Phase noise @ 10 kHz			-130	dBc/ Hz

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Phase noise @ 100 kHz			-135	dBc/ Hz

Table 9: Fast clock, digital clock AC specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_{RISE}	10% - 90% rise time			70% of the clock period	ns
T_{FALL}	90% - 10% fall time			70% of the clock period	ns
D_{CYCLE}	Duty cycle	35	50	65	%
	Phase noise @ 10 kHz			-130	dBc/ Hz
	Phase noise @ 100 kHz			-135	dBc/ Hz

Table 10: Slow clock specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
F_{IN}	Clock input frequencies	32, 32.768			kHz
	Duty cycle	30		70	%
	Tolerance on input frequency	•-250		250(1)	ppm
V_{IL}	Low level input voltage			0.35 * VDD_IO	V
V_{IH}	High level input voltage	0.65 * VDD_IO			V
V_{hyst}	Schmitt trigger hysteresis	150			mV
C_{IN}	Input capacitance			5	pF
T_{RISE}	10% - 90% rise time (1)			500	ns
T_{FALL}	90% - 10% fall time(2)			500	ns
	Total jitter(3)			250(3)	ppm

Notes:

(1) For use of the slow clock for FM, in case the accuracy of the externally applied slow clock is not sufficient, the STLC2690 provides a calibration mechanism to calibrate the slow clock versus the fast clock.

(2) The rise and fall time are not the most important parameters for the slow clock input due to the Schmitt trigger logic. It is more important that the noise on the slow clock line remains substantially below the hysteresis in amplitude.

(3) The total jitter is defined as the error that can appear on the actual frequency between two clock edges compared to the perfect frequency. Due to this, the total jitter value must contain the jitter itself and the error due to the accuracy on the clock frequency. The lower the accuracy, the smaller the jitter is allowed to be.

2.3.5 Current consumption

Current consumption of the Bluetooth subsystem

(Tamb = 25 °C, 26 MHz digital clock, 4 dBm output power for BR packets, 3 dBm output power for EDR packets, VDD_HV_x = VDD_IO = 1.8 V. With HCI interface in sleep mode.)

Table 11: Current consumption - Bluetooth subsystem

State	Typ.	Unit
Complete power down	1	µA
Deep Sleep mode	18	µA
Functional Sleep mode(1)	1.47	mA
HW Inquiry scan (1.28 s period, 11.25 ms window), combined with H4 UART Deep Sleep mode (*Section 4.3.1: "HCI transport layer"*)	210	µA
HW page scan (1.28 s period, 11.25 ms window), combined with H4 UART Deep Sleep mode (*Section 4.3.1: "HCI transport layer"*)	210	µA
HW inquiry and page scan (1.28 s period, 11.25 ms window), combined with H4 UART Deep Sleep mode (*Section 4.3.1: "HCI transport layer"*)	390	µA
Sniff mode (1.28 s, 4 attempts, 0 timeouts), combined with H4 UART Deep Sleep mode (*Section 4.3.1: "HCI transport layer"*) - Master - Slave	 79 105	 µA µA
Idle ACL connection - Master - Slave	 2.9 4.9	 mA mA
Active: data: DH1/DH1 symmetrical transfer (172.8 kbps), Master or Slave	21	mA
Active: data: DH5/DH1 asymmetrical transfer (TX 723.2 kbps & RX 57.6 kbps), Master or Slave Active: data: DH5/DH5 symmetrical transfer (433.9 kbps), Master or Slave	30.7 27.1	mA mA
Active: data: 2-DH5/2-DH5 symmetrical transfer (869.7 kbps), Master or Slave	28	mA
Active: data: 3-DH5/3-DH5 symmetrical transfer (1306.9 kbps), Master or Slave	28	mA
Active: audio: HV3, Master, not sniffed	8.7	mA
Active: audio: HV3, Slave, Sniff (1.28 s, 2 attempts, 0 timeouts)	8.3	mA
Active: audio: eSCO (EV3), (64 kbps symmetrical, T_{SCO} = 6) - Master - Slave (1 retransmission)	 9 9.4	 mA mA
Active: audio: eSCO (2-EV3), (64 kbps symmetrical, T_{SCO} = 12) - Master - Slave (1 retransmission)	 5.9 5.4	 mA mA
Active: audio: eSCO (3-EV3), (64 kbps symmetrical, T_{SCO} = 18) - Master - Slave (1 retransmission)	 5 4.3	 mA mA

Notes:

(1) In functional Sleep mode, the baseband clock is still running.

Current consumption of the FM subsystem

(Tamb = 25 °C, VDD_HV_x = VDD_IO = 1.8 V. With HCI interface in sleep mode. Using dedicated I2C and I2S interfaces. FM in mono operation. Using the HCI interface for control would add typically the Sleep mode current of the Bluetooth subsystem except if the HCI interface is put in Sleep mode.)

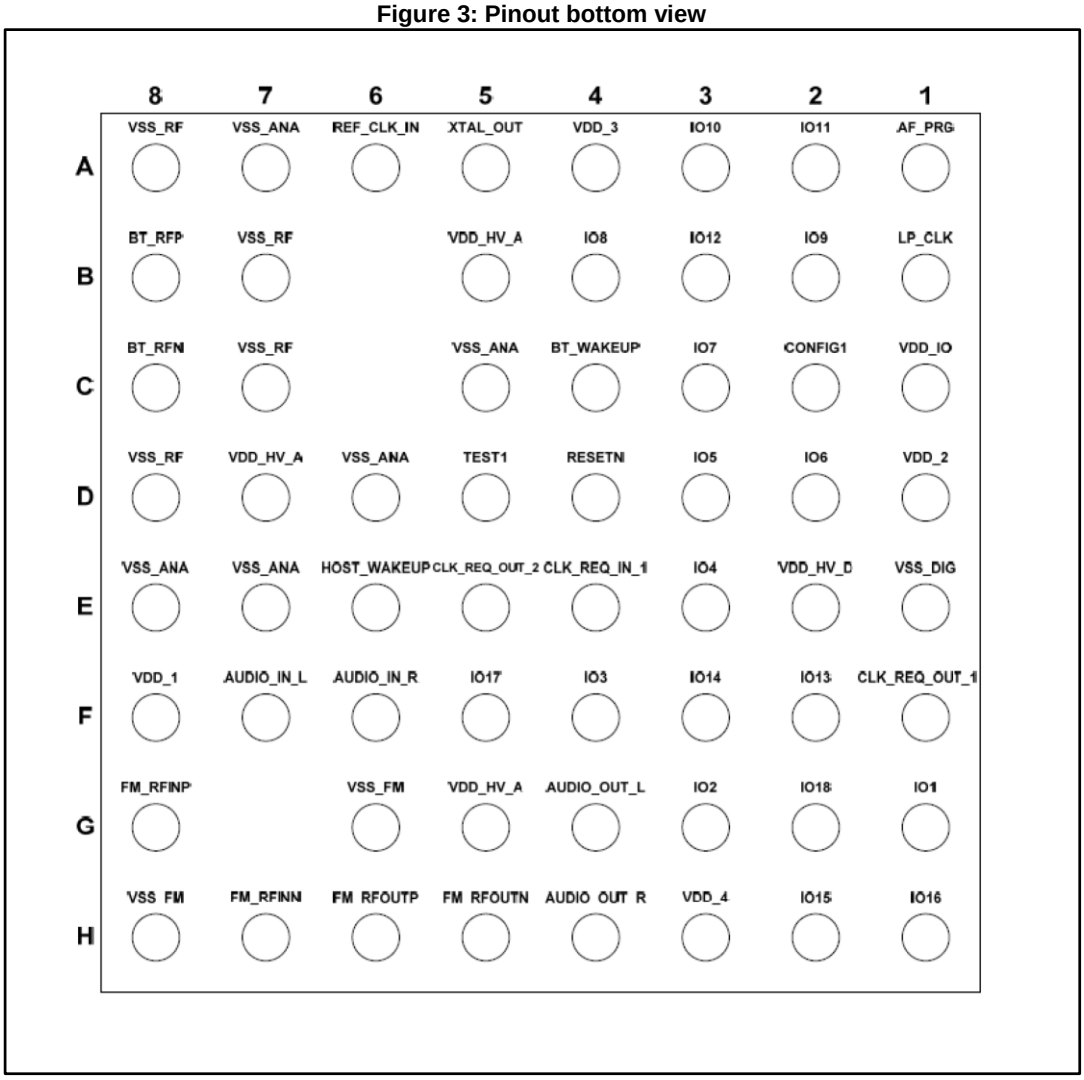
Table 12: Current consumption - FM subsystem

State	Typ.	Unit
Complete power down	1	µA
Active RX on slow clock	15	mA
Active TX (at 120 dBµVpdiff output power)	21	mA

2.4 Pinout

2.4.1 Pinout

Figure 3: Pinout bottom view



2.4.2 Pin list

Table 13: "The STLC2690 pin list (functional and supply)" shows the pin list of the STLC2690 during and after reset.

In columns “Reset” and “Default after reset”, the “PD/PU” shows the pads implementing an internal pull-down/up.

The column “Reset” shows the state of the pins during hardware reset; the column “Default after reset” shows the state of the pins after the hardware reset state is left, but before any Host activity on the Host interface and before the SW Parameter File download.

The column “Type” describes the pin directions:

- I for Input (All digital inputs have a Schmitt trigger function.)
- O for Output
- I/O for Input/Output (All digital inputs have a Schmitt trigger function.)
- O/t for tri-state output

For the output pins the default drive capability is 2 mA, except for the pins HOST_WAKEUP, IO7, IO9 and IO11 where it is 8 mA.

Table 13: The STLC2690 pin list (functional and supply)

Name	Pin#	Type	Description	Function during and after reset	Reset(1)	Default(2) after reset
Clock signals						
REF_CLK_IN	A6	I	Fast clock input when XTAL_OUT is strapped to VSS_DIG Otherwise XTAL input		Input	Input
XTAL_OUT	A5	I/O	Strapped to VSS_DIG when fast clock on REF_CLK_IN Otherwise XTAL feedback			
LP_CLK	B1	I	Slow clock input		Input	Input
Digital control signals						
RESETN	D4	I	Global reset – active low		Input	Input
CONFIG1	C2	I	Configuration pin, strapped to VSS_DIG		Input = 0	Input = 0
BT_WAKEUP	C4	I	Wake-up signal to Bluetooth (active high), should be strapped to VSS_DIG if not used		Input	Input
HOST_WAKEUP	E6	I/O(3)	Programmable pin	HOST_WAKEUP / SPI_INT	Input PD	Output low
CLK_REQ_IN_1	E4	I/O(3)	Programmable pin	CLK_REQ_IN	Input PD	Input PD
CLK_REQ_OUT_1	F1	I/O(3)	Programmable pin	CLK_REQ_OUT	Input PD	Output high
CLK_REQ_OUT_2	E5	I/O(3)	Programmable pin	CLK_REQ_OUT_N	Input PU	Output low
Digital interfaces						
IO1	G1	I/O(3)	Programmable pin	UART_RXD	Input PU	Input PU
IO2	G3	I/O(3)		UART_TXD	Input PU	Output high
IO3	F4	I/O(3)		UART_CTS	Input PU	Input PU

Name	Pin#	Type	Description	Function during and after reset	Reset[1]	Default[2] after reset
IO4	E3	I/O[3]		UART_RTS	Input PU	Output high
IO5	D3	I/O[3]	Programmable pin	SPI_CLK	Input PD	Input PD
IO6	D2	I/O[3]		SPI_DI	Input PD	Input PD
IO7	C3	I/O[3]		SPI_DO	Input PD	Tristate PD
IO8	B4	I/O[3]		SPI_CSN	Input PU	Input PU
IO9	B2	I/O[3]	Programmable pin	Not used	Input PD	Input PD
IO10	A3	I/O[3]		Not used	Input PD	Input PD
IO11	A2	I/O[3]		Not used	Input PD	Input PD
IO12	B3	I/O[3]		Not used	Input PD	Input PD
IO13	F2	I/O[3]	Programmable pin	FM_I2C_CLK	Input PU	Input PU
IO14	F3	I/O[3]		FM_I2C_DATA	Input PU	Input PU
IO15	H2	I/O[3]	Programmable pin	Not used	Input PD	Input PD
IO16	H1	I/O[3]		Not used	Input PD	Input PD
IO17	F5	I/O[3]		Not used	Input PD	Input PD
IO18	G2	I/O[3]		Not used	Input PD	Input PD
Bluetooth RF interface						
BT_RFP	B8	I/O	Differential Bluetooth RF port			
BT_RFN	C8	I/O				
FM RF interfaces						
FM_RFINP	G8	I	Differential FM RF input			
FM_RFINN	H7	I				
FM_RFOUTP	H6	I/O	Differential FM RF output and input, see *Section 5.2.1: "Dual RF input with RX/TX antenna switch"*			
FM_RFOUTN	H5	I/O				
Analog audio interfaces						
AUDIO_IN_L	F7	I	Left analog audio input			
AUDIO_IN_R	F6	I	Right analog audio input			
AUDIO_OUT_L	G4	I/O	Left analog audio output			

Name	Pin#	Type	Description	Function during and after reset	Reset[1]	Default[2] after reset
AUDIO_OUT_R	H4	I/O	Right analog audio output			
Power supply						
VDD_HV_D	E2		Power supply – Connect to platform supply			
VDD_HV_D	D7		Power supply – Connect to platform supply			
	G5					
	B5					
VDD_IO	C1		I/Os supply			
VDD_1	F8		Internal supply decoupling / Regulator output. Need 220 nF decoupling capacitor to VSS_ANA.			
VDD_2	D1		Internal supply decoupling / Regulator output. Need 220 nF decoupling capacitor to VSS_DIG.			
VDD_3	A4		Internal supply decoupling / Regulator output. Need 220 nF decoupling capacitor to VSS_ANA.			
VDD_4	H3		Internal supply decoupling / Regulator output. Need 220 nF decoupling capacitor to VSS_ANA.			
VSS_DIG	E1		Digital ground			
VSS_ANA	A7		Analog ground			
	E8					
	C5					
	E7					
	D6					
VSS_RF	B7		RF ground			
	C7					
	A8					
	D8					
VSS_FM	G6		FM ground			
	H8					
Other pins						
TEST1	D5		Test pin, to be strapped to VSS_ANA			
AF_PRG	A1	I/O	Test pin (leave unconnected)[4]		Open	Open

Notes:

(1) Pin behavior during HW reset (RESETN low).

(2) Pin behavior immediately after HW reset and internal chip initialization, but before any Host activity on the Host interface and the SW Parameter File download.

(3) Reconfigurable I/O pin. The functionality and type of these I/Os can be configured through different procedures (see *Section 3.4.3: "Pin mapping"*).

(4) Pin is ST-reserved for test function and it must be soldered to an isolated pad (not connected to anything, just floating).

2.4.3 Pin mapping

Some control signals and the digital interface pins are programmable pins, see . Different functions and different pull-up/down can be mapped on these pins. The control signals, digital interfaces and GPIOs of *Section 3.5: "Power supply"* can be mapped to these programmable pins.

Following procedure determines the final pin mapping.

- When using SPI as Host interface, the Host has the option to change the default settings of the SPI by writing in the SPI configuration register. One of the configurations is the mapping of the flow control, SPI_FLOW, to a pin.
- After reset, when the Host starts sending data over UART or SPI, this interface is recognized as being the Host interface. The I/Os are automatically remapped as indicated in *Section 7: "References"*.
- After the procedures described above are finished, a SW Parameter File can be downloaded to remap some of the pins and to configure pulls, see also *Section 4.1.7: "Download of the SW parameter file"*. This can also be done with HCI commands.

A detailed list of which functions map to which pins is available in *Section 7: "References"*.

2.5 Power supply

The chip runs from one single pre-regulated power supply from the platform for the core functions, VDD_HV_D (digital functions) and VDD_HV_A (analog functions), and one supply for the I/Os, VDD_IO. These supplies could be connected to the same platform supply or to different supplies. A decoupling capacitor is needed on these supplies. Also a dedicated regulator can be used, see *Section 3.5.1: "Dedicated STLC2690 regulator operation"*.

Internal regulators generate the core voltages. VDD_1, VDD_2, VDD_3, VDD_4 are the outputs of these internal regulators. Supply decoupling capacitors are needed on these outputs.

The grounds VSS_DIG, VSS_ANA, VSS_RF and VSS_FM have to be connected to the platform ground.

Specific layout guidelines need to be taken into account to ensure the full chip performance, see *[11]*.

For the absolute maximum ratings and operating conditions, see *Section 3.3.1: "Absolute maximum ratings"*.

2.5.1 Dedicated STLC2690 regulator operation

The signal REG_CTRL allows the control of an external battery regulator dedicated to the STLC2690. This regulator is meant to supply the STLC2690 with 1.8 V. It allows to partly decouple the core supply of the STLC2690 from the platform, while keeping the best implementation in terms of power consumption.

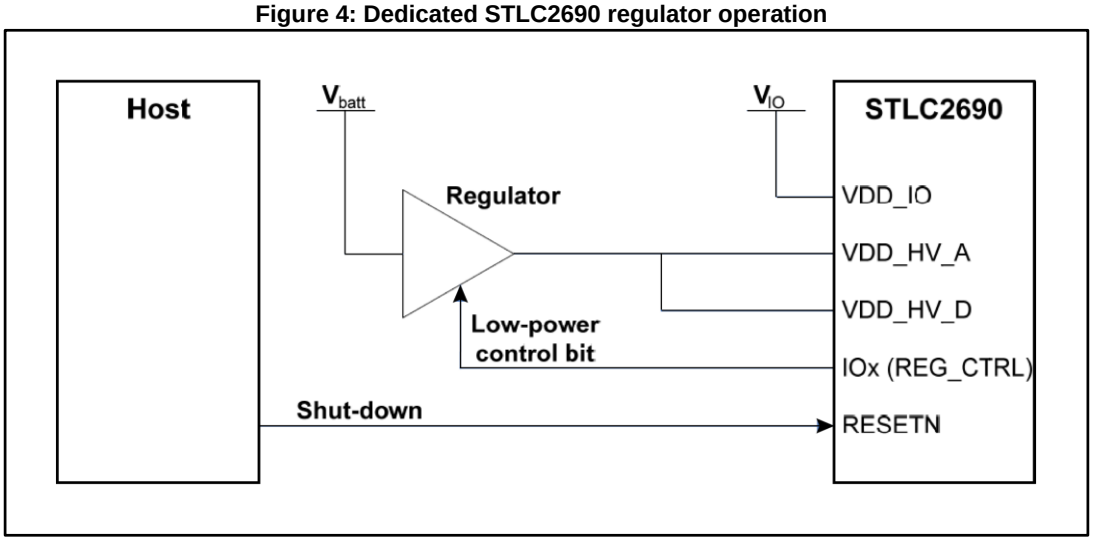
This mode requires a regulator that supports low power mode providing for two modes of operations:

- **Active mode**: High current/accuracy capability;
- **Low power mode**: Small current/lower accuracy, with internal consumption of a few µA.

The low power control bit of this regulator is connected to the REG_CTRL. When REG_CTRL = 0, the regulator is in low power mode, when REG_CTRL = 1, the regulator is in active mode.

The next picture gives an example of the connections. Possible decoupling capacitors are not shown on this drawing.

Figure 4: Dedicated STLC2690 regulator operation

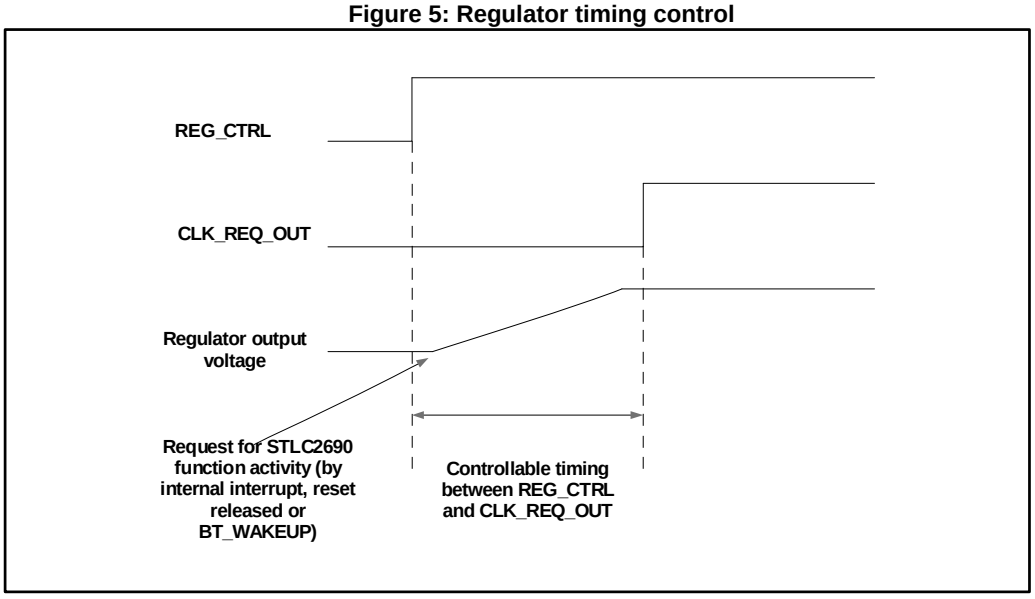


The low power mode usage or active mode of the external regulator is linked with the low power modes of the Bluetooth subsystem (Deep Sleep mode and Complete Power Down) and FM subsystem (Deep Sleep mode and Complete Power Down).

This means that REG_CTRL is low when the Bluetooth and FM subsystem go in low power mode and is high in all other cases.

Based on the time it takes for an external regulator to settle the voltage, the timing of REG_CTRL can be adjusted to become active before CLK_REQ_OUT_x is active. The picture below shows the behavior for both signals.

Figure 5: Regulator timing control



The timing of REG_CTRL is controllable between 0 and 30 ms in several steps and is set to 30 ms at startup. This parameter is defined via the SW Parameter File download and depends on the regulator and the platform behavior.

2.6 Clocks

2.6.1 Fast clock (system clock)

This clock is the main clock of the chip. It is used for most of the Bluetooth operation like transmission, reception, Host communication, ... The FM transmitter and receiver can work with this clock in all their modes. It is selected by an FM Parameter, whether the FM works with this clock (and requests it via CLK_REQ_OUT_x) or with the slow clock.

This clock needs only to be present when the STLC2690 is requesting it via CLK_REQ_OUT_x, see *Section 3.6.4: "Clock request signals"*. When the fast clock is generated from an external crystal directly connected to the chip, these clock request signals are not used.

This clock is provided to the chip either as a digital square wave input, a sinusoidal low amplitude signal, or is generated using an external crystal directly connected to the chip.

- When the clock is provided as a digital square wave or as an analog sine wave from the platform, the supported frequencies are 13, 16, 16.8, 19.2, 26, 32, 33.6, 38.4 and 52 MHz. The clock input pin is REF_CLK_IN. In this case the XTAL_OUT should be strapped to ground.
- When the fast clock is generated from an external crystal directly connected to the chip, the supported crystal frequencies are 13, 16, 16.8, 19.2, 26, 32, 33.6 and 38.4 MHz. The integrated oscillator cell supports the crystal characteristics listed in the table below. The input pin of the crystal is REF_CLK_IN, the feedback pin of the crystal is XTAL_OUT.

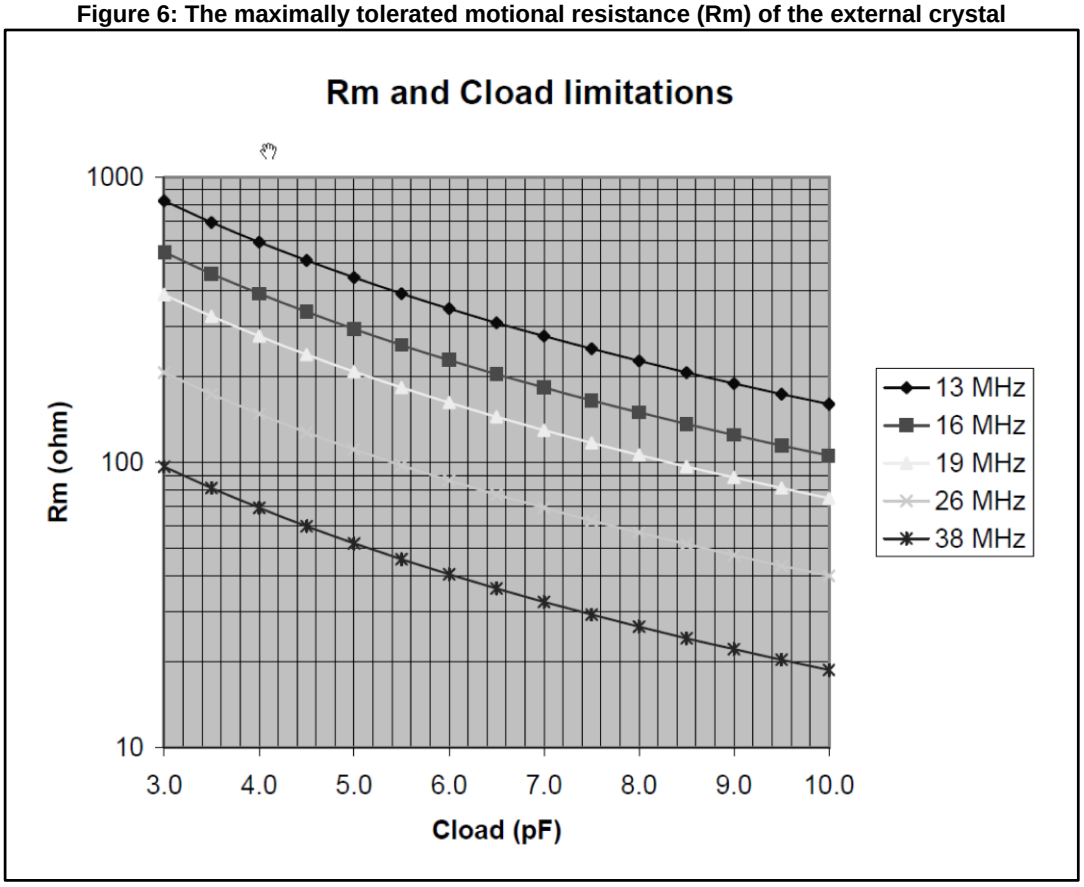
For detailed characteristics, see *Section 3.3.4: "Clock specifications"*.

Table 14: External crystal characteristics

Specification	Min.	Typ.	Max.	Unit
Initial crystal frequency accuracy			± 25	ppm
Crystal pullability	10		150	ppm/pF
Crystal drift (aging & temperature drift)			± 15	ppm

The maximally tolerated motional resistance (R_m) of the crystal depends both on the frequency and load capacitance seen by the crystal, as shown in *Figure 6: "The maximally tolerated motional resistance (Rm) of the external crystal"*.

Figure 6: The maximally tolerated motional resistance (Rm) of the external crystal



2.6.2 Slow clock (low power clock)

This clock is used for the low power modes support of BT. The FM transmitter and receiver can work with this clock in all their modes. It is selected by an FM parameter, whether the FM works with this clock or with the fast clock.

After power-up, the slow clock must be available before the reset is released. It must remain active all the time until the chip is powered off.

This clock is provided to the chip through a standard digital input, LP_CLK, with default characteristics. The input contains a Schmitt trigger and does not contain any pull, see also .

The slow clock can be 32 kHz or 32.768 kHz with an accuracy of ±250 ppm. For detailed characteristics, see *Section 3.3.4: "Clock specifications"*.

For use of the slow clock for FM, in case the accuracy of the externally applied slow clock is not sufficient, the STLC2690 provides a calibration mechanism to calibrate the slow clock versus the fast clock.

2.6.3 Clock detection

An integrated automatic detection algorithm detects the system and slow clock frequencies after a hardware reset. The steps in the clock detection routine are:

- Identification of the fast clock frequency (13 MHz, 16 MHz, 16.8 MHz, 19.2 MHz, 26 MHz, 32 MHz, 33.6 MHz, 38.4 MHz, 52 MHz)
- Identification of the slow clock (32.768 kHz or 32 kHz)

- The slow clock frequency can be confirmed during parameter download and is mandatory if 32 kHz frequency is used

2.6.4 Clock request signals

To allow minimum power consumption, a clock request feature is available so that the fast clock (REF_CLK_IN) can be stopped when not needed by the Bluetooth or FM system. The clock request signal can be active high or active low, and the STLC2690 supports internal propagation of clock request signal coming from another device in the system. When the fast clock is generated from an external crystal directly connected to the chip, these clock request signals are not used.

Different configurations as described below are supported during reset and in all operation modes, provided that VDD_IO is available. For the propagation of the external request signal, both VDD_HV_D and VDD_IO need to be present.

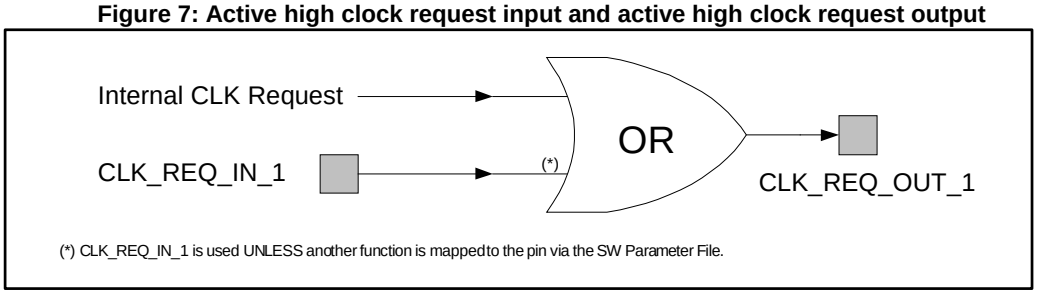
The clock request functionality is based on three different signals: CLK_REQ_OUT_1, CLK_REQ_OUT_2 and CLK_REQ_IN_1, with the following function. The signals are available depending on the pin mapping, see *Section 3.4.3: "Pin mapping"*.

- CLK_REQ_OUT_1: active high clock request output. Support for either push-pull or open drain output.
- CLK_REQ_OUT_2: active low clock request output. Support for either push-pull or open drain output.
- CLK_REQ_IN_1: active high clock request input from another device.

The following modes are supported:

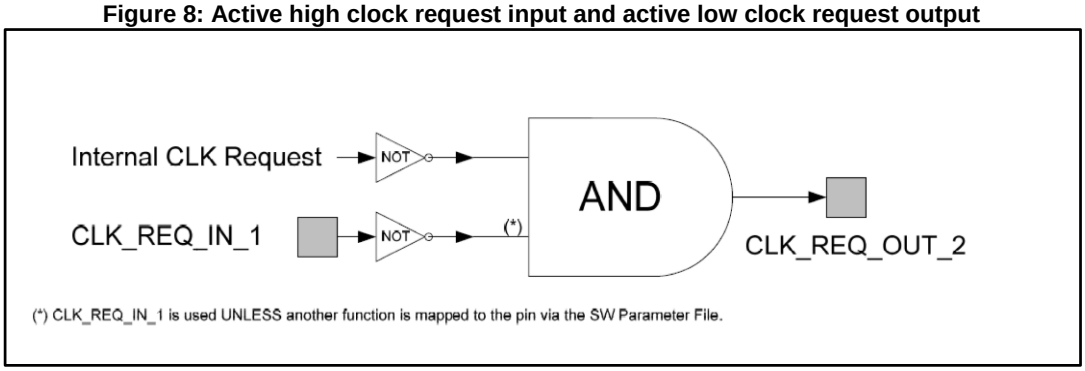
- Active high clock request input and active high clock request output:

Figure 7: Active high clock request input and active high clock request output



- Active high clock request input and active low clock request output:

Figure 8: Active high clock request input and active low clock request output



2.7 Reset and power-up

The behavior of the chip is independent of the power supplies (VDD_HV_x and VDD_IO) activation sequence.

In case of pre-regulated power supply from the platform, the RESETN pin should be active while powering up VDD_HV_x and should stay active at least two cycles of the slow clock (LP_CLK) after power-up is completed.

The chip is able to start without the fast clock being present. It requests it through CLK_REQ_OUT_x before using it.

The time between the Bluetooth subsystem making CLK_REQ_OUT_x active and the platform providing a stable clock should maximally be 15 ms. If the clock is starting faster on the platform, this timing can be reduced through parameter download.

As the FM radio and the Bluetooth are sharing the same reset pin in STLC2690, the start-up sequences of both functions are not completely independent. Hence, a typical start-up should be compliant with the sequence below:

- Supplies are powered up
- LP_CLK (slow clock) is running and stable
- RESETN pin is released after at least two LP_CLK cycles.
- After around 30 ms, CLK_REQ_OUT_x is set to request the fast clock (REF_CLK_IN).
- After 15 ms, REF_CLK_IN should be stable and the system can start using it. The SW is starting, doing clock recognition, internal configuration, and the HCI interface becomes operational.
- The host performs the SW Parameter File download of the Bluetooth subsystem. This allows the Bluetooth subsystem to correctly operate, but this allows also and mainly to set the device in the optimal power mode for the application in which it resides.
- From this point on, the Host can either decide to use Bluetooth only, or it can also start configuring or using the FM radio, either through the FM I2C interface, or through the BT HCI interface. The signals REG_CTRL and CLK_REQ_OUT_x indicate which supply is needed and whether the fast clock is needed or can be shut down.

However, it is possible to use the FM radio through the FM I2C interface without doing the Bluetooth SW Parameter File download.

2.8 Power down

The power down of the chip does not contain any constraints. It is possible to power-off VDD_IO and VDD_HV_x independently and in whatever order without resulting in increased static current consumption. If any of the two supplies is removed, the chip goes back to reset state. It is however recommended that the platform activates the RESETN at least 2 LP_CLK cycles before powering-off of the supplies.

2.9 Low power modes

2.9.1 Overview

The STLC2690 is designed for lowest power operation in all modes. To achieve this, several power modes are supported. Due to their different ways of operating (in bursts for Bluetooth, constant for FM), different low power modes are defined both for Bluetooth and FM as listed below.

On top of these internal power modes, and linked to them, the HCI interface also has the capability to be put in a low power mode (called Sleep mode). This is the only way for the Bluetooth subsystem of the system to go in Deep Sleep mode or Complete Power Down. When no data have to be transferred on the HCI interface for some time, the Host should place it in Sleep mode so that the power consumption is always minimized for the system.

Table 15: Bluetooth low power modes

Low power mode	Description
Sleep mode	The Bluetooth subsystem: - Accepts HCI commands from the Host. - Supports all types of Bluetooth links. - Can transfer data over Bluetooth links. - Dynamically switches between sleep and active mode when needed. - The fast clock is still active in part of the design. - Parts of the chip are dynamically powered off depending on the Bluetooth activity.
Deep sleep mode	The Bluetooth subsystem: - Does not accept HCI commands from the host. - Supports Page and Inquiry scans. - Supports Bluetooth links that are in Sniff or Sniff Subrating. - Dynamically switches between deep sleep and active mode during Bluetooth activity. The deep sleep mode entry is initiated by the Host, the Bluetooth subsystem acknowledges or not. The wake-up mechanism must be enabled by the SW Parameter File download before it can be used. - The fast clock is not active in any part of the design. - Parts of the chip are dynamically powered off depending on the Bluetooth activity.
Complete power down	The Bluetooth subsystem is effectively powered down: - No Bluetooth activity is supported. - The HCI interface is shut down. - The fast clock is not active in any part of the design. - Most parts of the chip are completely powered off. - RAM content is not maintained (initialization is required at wake-up). - Some pins (4 UART, CLKREQIN) keep their previous configuration (input or output, pull behavior) during Complete Power Down. - The host needs to send once an HCI command to allow the Bluetooth subsystem to go in Complete Power Down. The Bluetooth subsystem then goes into Complete Power Down each time the Host sends a Deep Sleep command and there is no activity anymore on the Bluetooth subsystem, this in order to ensure a smooth transition from active to Complete Power Down state. In order to go out of this mode, either a HW reset or BT_WAKEUP = ‘1’ is needed.

Table 16: FM low power modes

Low power mode	Description
Active mode	The FM radio is running and is either receiving or transmitting FM signal. The necessary logic for operation is powered and clocked. The user can define what operation mode is selected and can transfer audio or RDS data through I2C, I2S or analog audio interfaces.
Complete Power Down	The FM radio is not operating. FM radio restart is done either through a dedicated command through the FM I2C interface or through the BT HCI interface. Most parts of the FM radio are powered off to reduce leakage to the minimum. If SW download is necessary for FM operation, the SW needs to be downloaded again when going out of Complete Power Down mode. The switch between Active and Complete Power Down mode for FM is done on request of the Host.

2.9.2 Examples for the usage of the Bluetooth low power modes

Sniff or sniff subrating

The Bluetooth subsystem is in active mode with a Bluetooth connection. Once the transmission is concluded, Sniff or Sniff Subrating is programmed. When one of these two states is entered, the Bluetooth subsystem goes into Sleep mode. After that, the Host may decide to place the Bluetooth subsystem in deep sleep mode. The deep sleep mode allows for lower power consumption. When the Bluetooth subsystem needs to send or receive a packet (e.g. at T_{sniff} or at the beacon instant), the Bluetooth subsystem requests the fast clock and enters active mode for the needed transmission/reception. Immediately afterwards, the Bluetooth subsystem goes back to Deep Sleep mode. If some HCI transmission is needed, the UART or SPI link is reactivated and the Bluetooth subsystem moves from Deep Sleep mode to Sleep mode.

Inquiry/page scan

When only Inquiry scan or Page scan is enabled, the Bluetooth subsystem goes in Sleep mode or Deep Sleep mode outside the receiver activity. The selection between Sleep mode and deep sleep mode depends on the UART/SPI activity as in Sniff or Sniff Subrating.

No connection

If the host allows deep sleep mode and there is no activity, then the Bluetooth subsystem puts itself in deep sleep mode. The Host can decide to exit the deep sleep mode by the wake-up mechanisms described in *Section 4.3.1: "HCI transport layer"*. In this Deep Sleep mode (no connection), the Host can also decide to put the Bluetooth subsystem in Complete Power Down to further reduce the power consumption. In this case some part of the Bluetooth subsystem is completely powered off. The request to quit the Complete Power Down is done either by putting the BT_WAKEUP signal to ‘1’ or with an HW reset.

Active link

When there is an active link ((e)SCO or ACL), the Bluetooth controller does not go in deep sleep mode and not in Complete Power Down. But the Bluetooth controller is made in such a way that whenever it is possible, depending on the scheduled activity (number of link, type of link, amount of data exchanged), it goes in sleep mode.

2.9.3 Bluetooth and FM operation modes

The different low power modes of BT and FM are combined for the different mode of operation, especially when FM is controlled through the HCI interface. The table below summarizes these different operation modes and the related used power modes for the two functions.

Table 17: Bluetooth and FM operation modes

Operation mode	BT Power mode	FM Power mode	HCI mode
System startup, reset released, fast clock available	Active/Sleep	Complete power down	Active
- BT SW Parameter File download done - no Bluetooth activity - no FM activity -HCI interface active	Sleep	Complete power down	Active

Operation mode	BT Power mode	FM Power mode	HCI mode
- BT SW Parameter File download done - no Bluetooth activity - no FM activity - HCI interface in sleep	Deep sleep	Complete power down	Sleep
- Bluetooth active (ACL or SCO) - FM not active - HCI interface active	Active/Sleep	Complete power down/Sleep	Active
- Bluetooth in low power mode (sniff or scan) - FM not active - HCI in sleep	Deep sleep (with regular switch to sleep/active for BT activity)	Complete power down/Sleep	Sleep
- Bluetooth active (ACL or SCO) - FM active - HCI interface active	Active/Sleep	Active	Active
- Bluetooth in low power mode (sniff or scan) - FM active, using dedicated I2C and I2S or analog audio output - HCI in sleep	Deep sleep (with regular switch to sleep/active for BT activity)	Active	Sleep
- Bluetooth not active - FM active, using dedicated I2C and I2S or analog audio output - HCI in sleep	Deep sleep	Active	Sleep
- Bluetooth in complete power down (set by HCI command) - FM active, using dedicated I2C and I2S or analog audio output	Deep sleep (can not go in real CPD until FM radio is off)	Active	Sleep
- Bluetooth in virtual reset - FM not active	Complete power down	Complete power down	Sleep
- Bluetooth not active - FM active, using HCI for control - HCI mode under control of the Host	Sleep/Active	Active	Active/Sleep
- Bluetooth not active - FM active, using dedicated I2C for control and PCM/I2S of Bluetooth for audio - HCI mode under control of the Host	Deep sleep	Active	Active/Sleep

2.10 Multimedia features

Thanks to its ultra low power audio DSP, the STLC2690 offers efficient offloading to reduce the Host computation needs and to optimize overall platform power.

2.10.1 Direct loopback of FM Rx to BT A2DP link

The STLC2690 implements the streaming of FM radio over a BT A2DP link without any involvement of the Host during the streaming. This leads to a drastic reduction of the power consumptions as the Host can stay continuously in Sleep mode.

All the necessary processing that is normally done in the host is handled inside the STLC2690. This includes SBC encoding and A2DP/L2CAP framing.

2.10.2 SBC host offloading for BT A2DP

BT A2DP offloading can also be performed with audio data transferred from the host over the BT PCM or BT I2S interface. This slightly reduces the processing needs at the host side for BT A2DP streaming (becomes similar to playback with wired headset).

In that mode, the host sends stereo audio data samples (44.1 or 48 kHz) to the STLC2690. This data is encoded internally on the STLC2690 using SBC and encapsulated in A2DP and L2CAP frames for sending over the air.

2.11 Examples of Bluetooth and FM use cases

This paragraph lists the most common use cases that are supported. Each use case defines the mode of operation of the Bluetooth and the FM subsystem, and the active voice or audio interfaces. The HCI and FM I2C interfaces are not listed because in all use cases, HCI can be active or in sleep and FM I2C can be used or not, depending if FM is controlled through I2C or through BT HCI. This list does not include BT only or FM only use cases.

Table 18: Bluetooth and FM use cases

ID	Use case details	FM mode	BT mode	BT PCM	FM I2S
1	Transfer Bluetooth data while listening to radio.	Active Rx	Active ACL	No	Yes
2	Listening to radio with BT stereo headset using A2DP. The audio data are SBC encoded in the application processor or cellular baseband.	Active Rx	Active ACL	No	Yes
3	Listening to radio with BT stereo headset using A2DP. Audio is transferred from FM to BT inside the chip. The audio data are SBC encoded on the STLC2690.	Active Rx	Active ACL	No	No
4	Listening to radio (low quality) with BT voice headset. Audio is transferred from FM to BT at 8 kHz inside the chip.	Active Rx	Active SCO	No	No
5	Listening to radio (low quality) with BT voice headset. Audio is transferred from FM to BT outside the chip.	Active Rx	Active SCO	Yes (8 kHz)	Yes
6	Background RDS (RDS info retrieval) with tones over BT to headset.	Active Rx	Active SCO	Yes	No
7	Listening to radio (lo w quality) with BT voice headset, while streaming RDS data to laptop/PDA/…	Active Rx	Active ACL + SCO	Yes	Yes
8	Listening to radio (low quality) with BT voice headset, while transferring data over Bluetooth. Audio is transferred from FM to BT inside the chip.	Active Rx	Active ACL + SCO	No	No
9	Listening to radio (low quality) with BT voice headset, while transferring ACL data (for example DUN).	Active Rx	Active ACL + (e)SCO	Yes	Yes
10	Listening to radio with BT stereo headset using A2DP while transferring other data over Bluetooth. The audio data are SBC encoded in the application processor or cellular baseband.	Active Rx	Active ACL (A2DP) + ACL (other data)	No	Yes

ID	Use case details	FM mode	BT mode	BT PCM	FM I2S
11	Car radio hands free: voice call on GSM with BT headset connected. The received voice is sent to the car radio through FM Tx in place of the headset speaker.	Active Tx	Active (e)SCO	Yes	No (the FM transmit signal goes through BT PCM interface)
12	Audio FM transmit while doing gaming on Bluetooth (piconet with low latency).	Active Tx	Active ACLs	No	Yes

2.12 Digital interfaces

Some of these interfaces are available by default on the pins during and after reset, others become available by default as soon as the STLC2690 has detected which host interface is used, others can be mapped to the programmable pins according to *Section 3.4.3: "Pin mapping"*.

2.12.1 General control signals

The STLC2690 supports several control signals that have impact on the operation of the full chip (not dedicated to a specific function). Some of these signals are available by default on a pin, others can be mapped to a pin according to *Section 3.4.3: "Pin mapping"*.

Table 19: Control signals

Signal	Direction	Function
RESETN	input	Overall RESET of the chip, active low. If the chip is in reset, its power consumption is reduced to the minimum. More info on the timing and behavior on the reset can be found in *Section 3.7: "Reset and power-up"*. The pin RESETN is used by default as input for this signal RESETN.
REG_CTRL	output	Signal allowing the control of an external regulator dedicated to core voltage supply. This signal can be used to switch a regulator between low current and high current mode. This signal is active high. For more info on this signal behavior, see *Section 3.5.1: "Dedicated STLC2690 regulator operation"*. This signal is not available by default on a pin, but can be mapped to a pin according to *Section 3.4.3: "Pin mapping"*.
CLK_REQ_OUT	Output/Open drain output	Signal that requests the fast clock only when needed to allow power saving. An active high and an active low version of this signal are available, CLK_REQ_OUT and CLK_REQ_OUT_N respectively. For more info on this signal behavior, see *Section 3.6.4: "Clock request signals"*, *Section 3.7: "Reset and power-up"* and *Section 3.9: "Low power modes"*. These signals are available by default on the pins CLK_REQ_OUT_1 and CLK_REQ_OUT_2. If this function is not used, these pins may be reused for other functions after reset.
CLK_REQ_IN	input	Signal that allows the sharing of the fast clock between several devices on a board without the need of external components for the control of the enable of this clock. The pin CLK_REQ_IN_1 is used by default as input or this signal. If this function is not used, the pin may be reused for other functions after reset. For more info on this signal behavior, see *Section 3.6.4: "Clock request signals"*, *Section 3.7: "Reset and power-up"* and *Section 3.9: "Low power modes"*
BT_WAKEUP	input	Wakeup of Bluetooth subsystem of the chip when in low power mode. For more info on this signal behavior, see *Section 3.7: "Reset and power-up"* and *Section 3.9: "Low power modes"*. The pin BT_WAKEUP is used by default as input for this signal.

Signal	Direction	Function
HOST_WAKEUP	output	Wakeup of the Host by the chip when in low power mode. For more info on this signal behavior, see *Section 3.7: "Reset and power-up"* and *Section 3.9: "Low power modes"*. This signal is available by default on the pin HOST_WAKEUP. If this function is not used, the pin may be reused for other functions after reset.
CONFIG1	input	Configuration signal. The pin CONFIG1 is used by default as input for this signal. Should be strapped to VSS_DIG.
FM_IRQ	output	Signal that indicates a state change in the FM subsystem of the chip. E.g. RDS data received, FM channel found, … For more info on this signal behavior, see *Section 5.1.2: "Interrupt to the host"*. This signal is not available by default on a pin, but can be mapped to a pin according to *Section 3.4.3: "Pin mapping"*.

2.12.2 UART interface

The UART interface is a 4-wire data interface (UART_RXD, UART_TXD, UART_RTS, and UART_CTS). The UART interface is compatible with the 16450, 16550 and 16750 standards.

The 4 signals of the UART interface are the following:

- UART_RXD: Data transfer from the host to the STLC2690. To be connected to the host TXD.
- UART_TXD: Data transfer from the STLC2690 to the host. To be connected to the host RXD.
- UART_RTS: Flow control. To be connected to the host CTS. If the STLC2690 UART_RTS output is low, then the host is allowed to send. If the STLC2690 UART_RTS output is high, then the host is not allowed to send.
- UART_CTS: Flow control. To be connected to the host RTS. If the STLC2690 CTS input is low, then the STLC2690 is allowed to send. If the STLC2690 CTS input is high, then the STLC2690 is not allowed to send.

The UART interface has following characteristics:

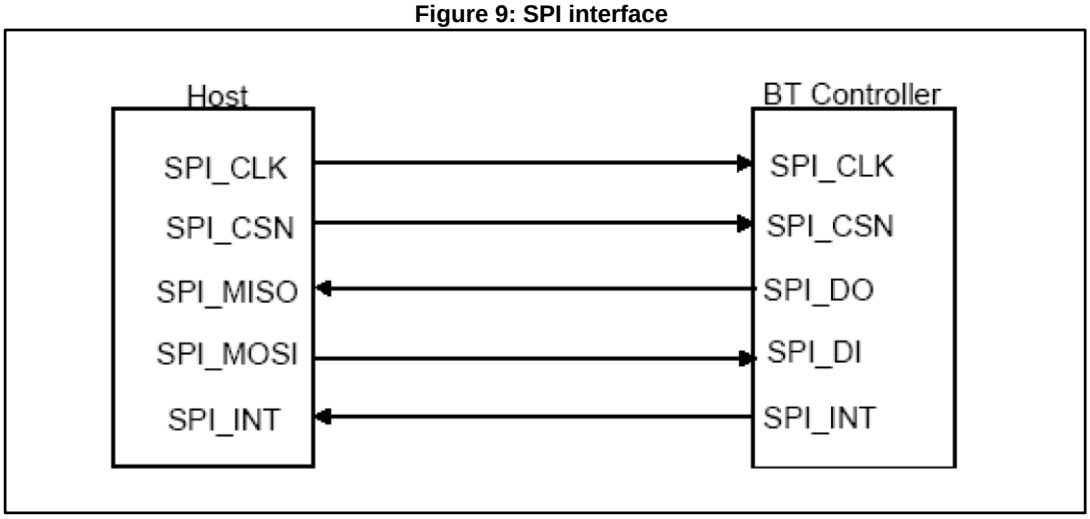
- It is running up to 4000 kbps (+1.5% / -1%). At startup, the UART baud rate is fixed at 115200 bps independently of the REF_CLK_IN frequency. A specific HCI command is provided to change the UART baud rate when necessary within the range 56 kbps to 4000 kbps. All standard baud rates and many other ones are supported.
- The configuration is 8 data bits, 1 start bit, 1 stop bit, and no parity bit.
- The transmit and receive paths contain a DMA function for low CPU load and high throughput. Auto RTS/CTS is implemented in HW, controllable by SW. RTS/CTS flow control is used to prevent temporary UART buffer overrun between the STLC2690 and the host.
- Flow-off response time is 500 µs. The flow-off response time defines the maximum time that the STLC2690 can still receive data after setting RTS high.

The UART interface is available on the pins by default during and after reset. When the STLC2690 has detected that the UART is not used as the host interface, these pins are remapped with different functions. See *Section 3.4.3: "Pin mapping"*.

2.12.3 SPI interface

The SPI interface is a 5-wire data interface (SPI_CSN, SPI_CLK, SPI_DO, SPI_DI and SPI_INT).

Figure 9: SPI interface



The 5 signals of the SPI interface are the following:

- SPI_CSN: chip select allows the use of multiple Slaves (1 chip select per Slave). This signal is active low. This signal is mandatory, even with only 1 Slave, because the Host must drive this signal to indicate SPI frames.
- SPI_CLK: clock signal, active for a multiple of data length cycles during an SPI transfer (SPI_CSN active). The clock is allowed to be active when SPI_CSN is not active, in order to serve other Slaves.
- SPI_DO: data transfer from Slave to Master. Data is generated on the negative edge of SPI_CLK by the Slave and sampled on the positive edge of SPI_CLK. When SPI_CSN is inactive, this STLC2690 output is in tristate mode.
- SPI_DI: data transfer from Master to Slave. Data is generated on the negative edge of SPI_CLK by the Master and sampled on the positive edge of SPI_CLK.
- SPI_INT: interrupt from the Slave, used to request an SPI transfer by the Slave to the Master. The signal is active high (Host input must be level sensitive).

The SPI interface has following characteristics:

- The maximum operating frequency is 52 MHz. The SPI interface in STLC2690 supports the timings defined below.
- The SPI interface is operating in half duplex mode.
- The SPI interface is Master at the Host side, and Slave at the STLC2690 side.
- The SPI data length, endianness and flow control are configurable. The Host can change the configuration by writing in the SPI configuration register.
- The flow control consists of an indication from the STLC2690 whether its receive buffers are ready to receive data. This indication is available in three ways:
  - On the SPI_DO during TSCS (time between SPI_CSN becoming active and SPI_CLK becoming high).
  - In a register that can be read by the Host.
  - Optionally on one of the programmable pins. This is enabled by writing the SPI configuration register, see .
- The default SPI configuration is:
  - 16 bit data length
  - Most significant byte first
  - Most significant bit first
  - Flow control on SPI_DO and in a register

The SPI interface is available on the pins by default during and after reset, except for the SPI_INT. When the STLC2690 has detected that the SPI is used as Host interface, the

SPI_INT is mapped to one of the other programmable pins. When the STLC2690 has detected that the SPI is not used as the Host interface, these pins are remapped with different functions. See .

For more detailed information on the SPI interface refer to *[14]*.

Figure 10: SPI data transfer from the Host (Master) to the STLC2690 (Slave)

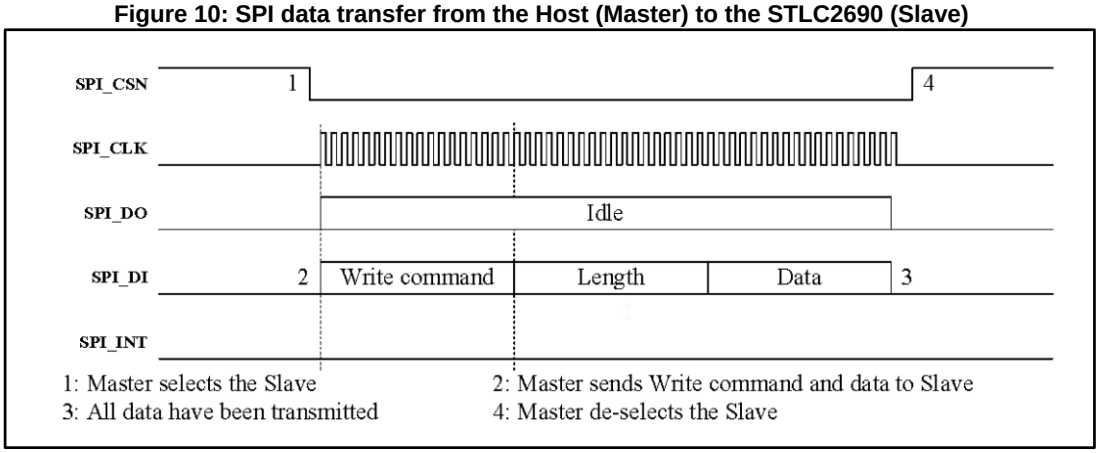


Figure 11: SPI data transfer from the STLC2690 (Slave) to the Host (Master)

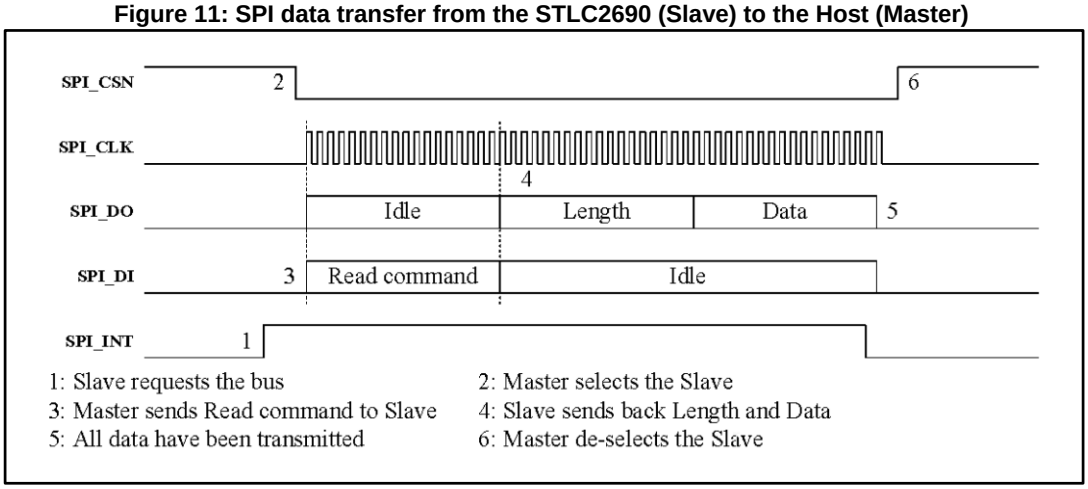


Figure 12: SPI Setup and hold timing

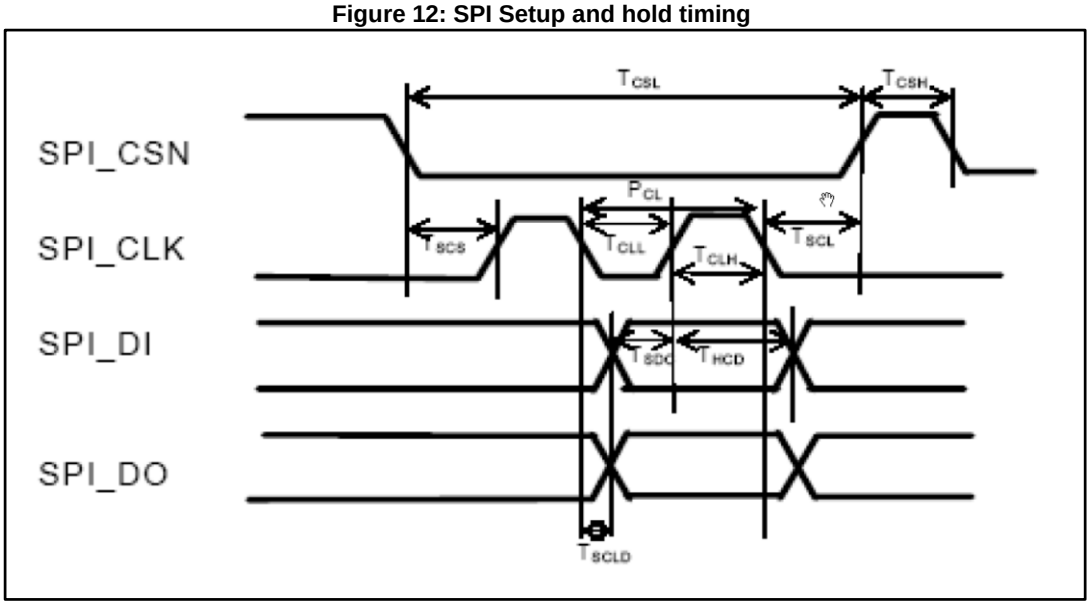


Table 20: SPI timing parameters

Symbol	Description	Min.	Typ.	Max.	Unit
P_{CL}	SPI_CLK full period	19.23			ns
T_{CLH}	High period of SPI_CLK	9			ns
T_{CLL}	Low period of SPI_CLK	9			ns
T_{CSH}	High period of SPI_CSN	1 * PCL			ns
T_{CSL}	Low period of SPI_CSN	9 * PCL			ns
T_{SCS}	Setup time, SPI_CSN low to SPI_CLK high	1 * PCL			ns
T_{SCL}	Setup time, SPI_CLK low to SPI_CSN high	1/2 * PCL			ns
T_{SDC}	Setup time, SPI_DI valid to SPI_CLK high	5			ns
T_{HCD}	Hold time, SPI_DI valid after SPI_CLK high	1			ns
T_{SCLD}	Setup time, SPI_CLK low to SPI_DO valid			9	ns

2.12.4 FM I2C interface

The FM I2C interface is a 2-wire low speed data interface (I2C_SCL and I2C_SDA) to access I2C peripherals. It is compatible with the I2C specification version 2.1, see *[9]*.

The 2 signals of the I2C interface are the following:

- I2C_SCL: clock signal.
- I2C_SDA: bidirectional data.

The FM I2C interface has following characteristics:

- The FM I2C interface is Slave at the STLC2690 side.
- It supports the fast mode operation, meaning 400 kHz I2C_SCL clock frequency. The I2C interface supports the timings below.
- It supports the 7-bits addressing mode and is able to coexists with the 10-bits addressing mode.

The FM I2C interface is present on chip pins in reset and default after reset, however all I2C traffic on these pins is not considered until the FM I2C address has been programmed by the Host via a vendor-specific HCI command on the Bluetooth HCI interface. The Host can decide to remap these pins with other functions. See *Section 3.4.3: "Pin mapping"*.

Figure 13: I2C interface timing

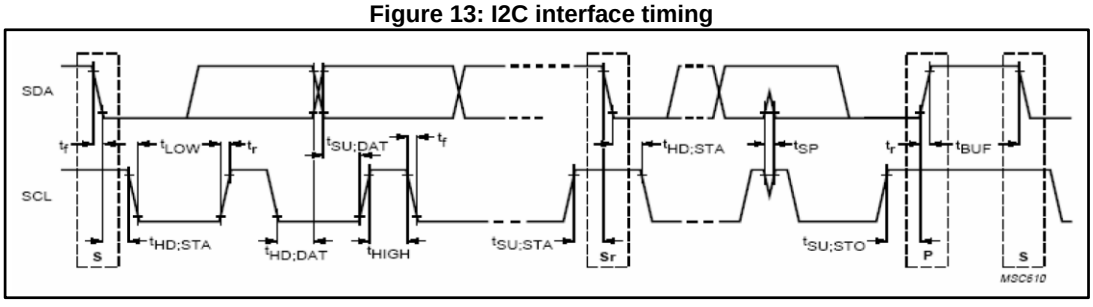


Table 21: I2C interface timing

Symbol	Parameter	Min.	Typ.	Max.	Unit
f_{SCL}	SCL clock frequency	0		400	kHz

Symbol	Parameter	Min.	Typ.	Max.	Unit
$t_{HD;STA}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated	0.6		-	µs
t_{LOW}	Low period of the SCL clock	1.3		-	µs
t_{HIGH}	High period of the SCL clock	0.6		-	µs
$t_{SU;STA}$	Setup time for repeated START condition	0.6		-	µs
$t_{HD;DAT}$	Data hold time for I2C-bus devices	0		0.9	µs
$t_{SU;DAT}$	Data setup time	100		-	ns
t_r	Rise time of both SDA and SCL signals (Cb is bus line capacitance)	20 + 0.1 * Cb		300	ns
t_f	Fall time of both SDA and SCL signals (Cb is bus line capacitance)	20 + 0.1 * Cb		300	ns
$t_{SU;STO}$	Setup time for stop condition	0.6			µs
t_{BUF}	Bus free time between a STOP and a START condition	1.3			µs
t_{SP}	Pulse width of spikes which must be suppressed by input filter	0		50	ns

2.12.5 Generic I2C interface

This I2C interface has the same specification as the FM I2C interface. Except that it is Master at the STLC2690 side.

The generic I2C interface can be used for any purpose, e.g. control of peripherals, and is controllable from HCI.

The generic I2C interface is not present on chip pins in reset or default after reset, and does not become default available once the STLC2690 has detected which interface is used as the host interface. The generic I2C interface can be mapped to the programmable pins by the SW Parameter File download or an HCI command. See *Section 3.4.3: "Pin mapping"*.

2.12.6 BT PCM interface

The BT PCM interface is a 4 wire voice/audio interface (PCM_CLK, PCM_SYNC, PCM_A and PCM_B) that allows direct voice/audio sample transfer between chips or to a standard codec.

The 4 signals of the PCM interface are the following:

- PCM_CLK : PCM clock
- PCM_SYNC : PCM synchronization signal, typically 8 kHz
- PCM_A : PCM data
- PCM_B : PCM data

The BT PCM interface has following characteristics (configurable through the SW Parameter File download or through HCI commands):

- By default PCM_A is the STLC2690 TX data and PCM_B is the STLC2690 RX data. This can be swapped.
- The following external PCM data formats are supported: linear (13 up to 16 bits), µ-law (8 bits) and A-law (8 bits).

- The air data format can be chosen independently from the external format and can be one of the following: CVSD, µ-law, A-law. Another possible air data format is “transparent data”, meaning that no coding or conversion is done on the data. In that case the external format has to be 8 bits wide.
- The interface can be programmed to act as a PCM Master or as a PCM Slave. By default the interface is in Slave mode, i.e. the 4 pins are in input mode, with pull-down active.
- In Master mode the PCM clock can be configured to be on only during the active PCM slots, or it can be on all the time there is an (e)SCO link.
- As a Master the interface by default generates a PCM clock rate of 2048 kHz, it can be configured to rates from 128 kHz up to 2048 kHz. As a Slave, it can automatically handle external PCM clock rates from 128 kHz up to 4000 kHz.
- When configured as a Master, the number of PCM clock cycles in one PCM_SYNC period can be reconfigured. In this way, the PCM_SYNC rate can be set to 8 kHz for narrow-band speech
- When configured as a Master, by default the PCM_SYNC signal is locked to the PCM clock. Alternatively, in order to address clock drift between the local and the remote PCM clock, the PCM_SYNC signal can be locked to the Bluetooth piconet clock. In that case the number of PCM clock cycles in one PCM_SYNC period is adjusted from time to time by 1 clock cycle at most. E.g. in the default configuration there may be some periods of 255 or 257 PCM clock cycles.
- In Master mode the PCM_SYNC length is configurable to 1 (short frame), 8 or 16 (long frame) PCM_CLK clock periods. In Slave mode all possible PCM_SYNC lengths are automatically supported, including “short frame” (taking 1 PCM_CLK clock period) and “long frame” PCM_SYNC signals (taking more than 1 PCM_CLK clock period).
- The interface also supports multi-port PCM operations: up to 3 different voice streams are supported by using up to 3 slots per PCM frame. This can also be used to generate stereo traffic in PCM interface.
- The start of the PCM data is configurable in the following ways:
  - The PCM_SYNC pulse (or pulses, see below) can be delayed with respect to the internal reference. The delay is expressed as a number of PCM clock cycles and is programmable between 0 and 255.
  - Alternatively, the start of each PCM slot can be delayed with respect to the rising edge of the PCM_SYNC signal. The delay is expressed as a number of PCM clock cycles and is programmable between 0 and 255.
- TX data are by default generated on the rising edge of PCM_CLK and expected to be latched by the external device on the falling edge, while RX data are latched on the falling edge of PCM_CLK. The inverted clock mode is also supported, whereby the generation of TX data is on the falling edge and the latching of TX and RX data is on the rising edge.
- When the STLC2690 is Master, one additional PCM_SYNC signal can be provided via the GPIO pins.
- Outside the active PCM slot(s) the PCM TX signal (PCM_A or PCM_B) can be configured in tristate or as output driving ‘0’.

The BT PCM interface is not present on chip pins in reset or default after reset, but becomes available once the STLC2690 has detected which interface is used as the Host interface. See *Section 3.4.3: "Pin mapping"*.

Figure 14: PCM (A-law, µ-law) Standard Mode

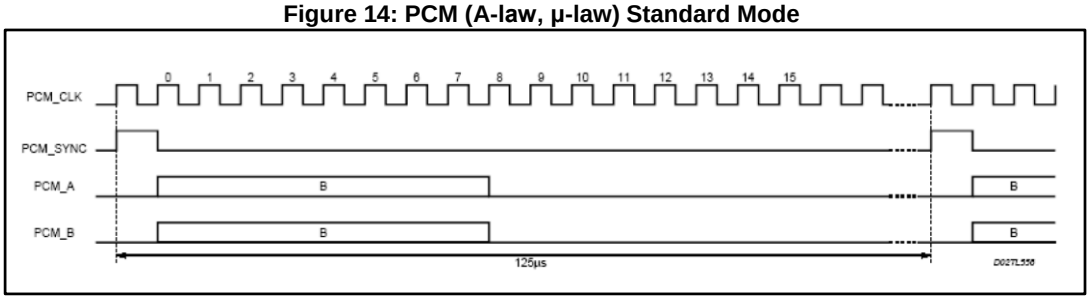


Figure 15: Linear Mode

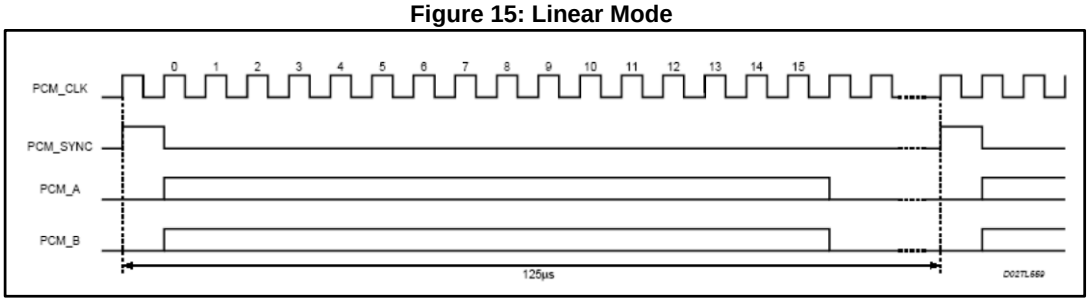


Figure 16: Multi-Slot operation

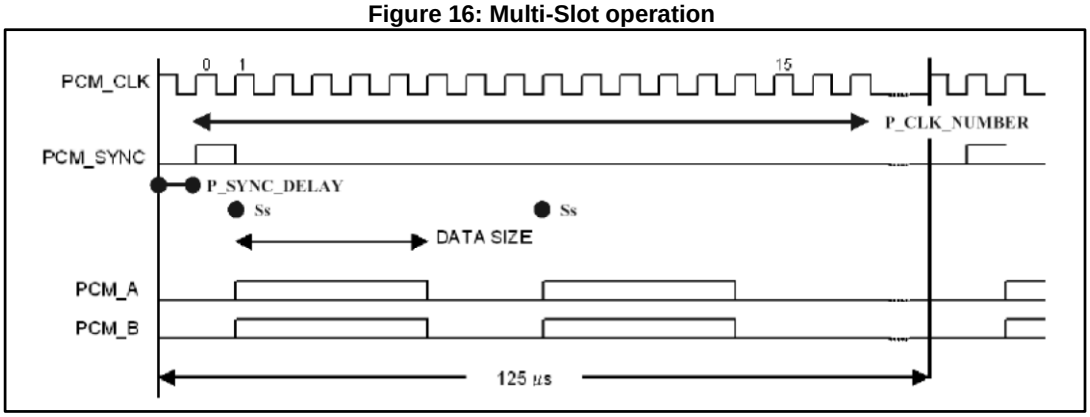


Table 22: PCM interface parameters

Symbol	Description	Min.	Typ.	Max.	Unit
PCM interface					
F_{PCM_CLK}	Frequency of PCM_CLK	128(1)	2048	4000(2)	kHz
F_{PCM_SYNC}	Frequency of PCM_SYNC		8		kHz
P_{sync_delay}	Delay of the starting of the first slot	0		255	cycles
S_s	Slot start (programmable for every slot)	0		255	cycles
D	Data size	8		16	bits
N	Number of slots per frame	1		3	

Notes:

(1) Note that it is not possible to use 16 bits in Slave case if PCM_CLK is 128 kHz. This is the only exception.

(2) In Master case, the maximum PCM_CLK frequency is limited to 2048 kHz.

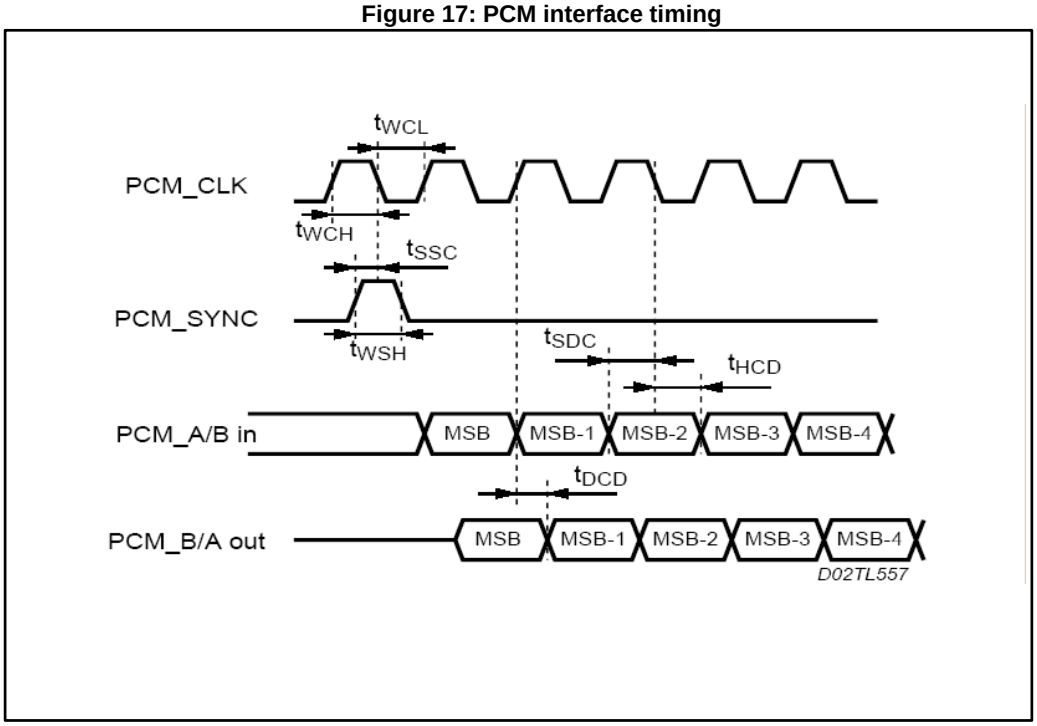
1. Note that it is not possible to use 16 bits in Slave case if PCM_CLK is 128 kHz. This is the only exception.

2. In Master case, the maximum PCM_CLK frequency is limited to 2048 kHz.

Table 23: PCM interface timing (at PCM_CLK = 2048 kHz)

Symbol	Description	Min.	Typ.	Max.	Unit
t_{WCH}	High period of PCM_CLK	200			ns
t_{WCL}	Low period of PCM_CLK	200			ns
t_{WSH}	High period of PCM_SYNC	200			ns
t_{SSC}	Setup time, PCM_SYNC high to PCM_CLK low	100			ns
t_{SDC}	Setup time, PCM_A/B input valid to PCM_CLK low	100			ns
t_{HCD}	Hold time, PCM_CLK low to PCM_A/B input valid	100			ns
t_{DCD}	Delay time, PCM_CLK high to PCM_A/B output valid			150	ns

Figure 17: PCM interface timing



2.12.7 FM PCM interface

The FM PCM interface is a 4 wire voice/audio interface (PCM_CLK, PCM_SYNC, PCM_A and PCM_B) that allows direct voice/audio sample transfer between chips or to a standard codec.

The 4 signals of the PCM interface are the following:

- PCM_CLK : PCM clock
- PCM_SYNC : PCM synchronization signal, typically 8 kHz
- PCM_DIN : STLC2690 PCM input data
- PCM_DOUT : STLC2690 PCM output data

The FM PCM interface has the following characteristics (configurable by FM commands) :

- The external PCM data format is linear (up to 16 bits).

- The interface can be programmed to act as a PCM Master or as a PCM Slave. By default the interface is in Slave mode, i.e. the 4 pins are in input mode, with pull-down active.
- In Master mode the PCM clock can be configured to be on only during the active PCM slots, or it can be on all the time when the interface is enabled.
- Supported PCM_SYNC rates range from 8 kHz to 48 kHz.
- When configured as a Master, the number of PCM clock cycles in one PCM_SYNC period can be configured, with a maximum number of 512.
- In Master mode the PCM_SYNC length is configurable to 1 PCM_CLK clock period (short frame) or to the entire length of the transfer (long frame). In Slave mode all possible PCM_SYNC lengths are automatically supported, including “short frame” (taking 1 PCM_CLK clock period) and “long frame” PCM_SYNC signals (taking more than 1 PCM_CLK clock period).
- Both the early PCM_SYNC case (PCM_SYNC preceding the data transfer by one PCM_CLK period) and the non-early PCM_SYNC case (PCM_SYNC starting simultaneously with the data transfer) are supported.
- TX data are by default generated on the rising edge of PCM_CLK and expected to be latched by the external device on the falling edge, while RX data are latched on the falling edge of PCM_CLK. The inverted clock mode is also supported, whereby the generation of TX data is on the falling edge and the latching of TX and RX data is on the rising edge.
- Outside the active PCM slot(s) the PCM DOUT signal can be configured in tristate or as output driving ‘0’.
- Similarly, when the PCM interface is disabled the PCM DOUT signal can be configured in tristate or as output driving ‘0’.

The FM PCM interface is not present on chip pins in reset or default after reset, and does not become default available once the STLC2690 has detected which interface is used as the Host interface. The FM PCM interface can be mapped to the programmable FM I2S pins by FM commands. See *Section 3.4.3: "Pin mapping"*.

2.12.8 FM I2S interface

The I2S interface is a 4-wire voice/audio interface (I2S_CLK, I2S_WS, I2S_DIN and I2S_DOUT). It is compatible with the I2S specification, see *[10]*.

The 4 signals of the I2S interface are the following:

- I2S_CLK : I2S clock
- I2S_WS: I2S word select signal at sampling frequency
- I2S_DIN : I2S STLC2690 input data
- I2S_DOUT : I2S STLC2690 output data

The interface has following characteristics (configurable through the SW Parameter File download or through HCI commands):

- The external data format is linear with 16 bits. Data are transferred with the most significant bit first and are left aligned.
- Both mono and stereo modes are supported. In mono mode the same data are sent in the two slots. In stereo mode the left data are sent when the I2S_WS signal is low while the right data are sent when the I2_WS signal is high.
- The FM I2S interface is operating in half-duplex.
- The interface can be programmed to act as a Master or as a Slave.
- Both as a Master and as a Slave the interface supports I2S clock rates from 192 kHz up to 6144 kHz in steps of 8 kHz.
- Both as a Master and as a Slave the interface supports I2S sample rates from 8 kHz up to 192 kHz.

- When configured as a Master, the STLC2690 generates and outputs I2S_CLK and I2S_WS; in this mode, the clock rate is fixed to 32 times the I2S_WS rate.
- By default, data is shifted out on I2S_DOUT on the falling edge of I2S_CLK and expected to be latched by the external device on the rising edge, while data shifted in through I2S_DIN is latched on the rising edge of I2S_CLK.
- The polarity of I2S_CLK, I2S_WS, I2S_DIN and I2S_DOUT is, however, programmable.
- By default, the MSB bits are transmitted in the I2S clock cycle following the transition of the I2S_WS signal, but the interface can also be configured to have the MSB bits coincide with the transitions of the I2S_WS signal, to connect to CODECs that are not compliant with I2S but use a left aligned or 16-bit right aligned data format instead.
- When more than 16 bits per channel are transferred, i.e. the clock rate is higher than 32 times the I2S_WS rate, the data output on I2S_DOUT is padded with zeros as LSBs, and the LSBs of incoming data on I2S_DIN are ignored.

The FM I2S interface is not present on chip pins in reset or default after reset, but becomes available once the STLC2690 has detected which interface is used as the Host interface. See *Section 3.4.3: "Pin mapping"*.

2.12.9 BT I2S interface

This I2S interface has the same specification as the FM I2S interface, except for the following:

- Both as a Master and as a Slave the interface supports I2S clock rates from 256 kHz up to 4000 kHz in steps of 8 kHz.
- Both half-duplex and full-duplex are supported.
- The position of the rising edge of the I2S_WS signal can be configured for the case where the clock rate is faster than 32 times the I2S_WS rate.
- When the clock rate is faster than 32 times the I2S_WS rate, during the non-active clock cycles the I2S_DOUT signal can be configured in tristate or as output driving ‘0’. The I2S clock can be configured to remain on during these non-active clock-cycles, or it can be configured to be off.

The BT I2S interface is not present on chip pins in reset or default after reset, and does not become default available once the STLC2690 has detected which interface is used as the host interface. The BT I2S interface can be mapped to the programmable PCM pins by the SW Parameter File download or an HCI command. See *Section 3.4.3: "Pin mapping"*.

2.12.10 WLAN/WiMAX coexistence interface

The WLAN/WiMAX coexistence interface is a 1 to 4-wire interface (WLAN1, WLAN2, WLAN3 and WLAN4) to a WLAN and/or WiMAX chip that allows optimal coexistence between Bluetooth and WLAN and/or WiMAX, when both functions are collocated.

The 4 signals of the WLAN/WiMAX coexistence interface and the characteristics are defined in *Section 4.1.9: "Bluetooth – WLAN/WiMAX coexistence in collocated scenario"*.

The WLAN/WiMAX coexistence interface is not present on chip pins in reset or default after reset, but becomes available once the STLC2690 has detected which interface is used as the Host interface. See *Section 3.4.3: "Pin mapping"*.

2.12.11 JTAG interface

The JTAG interface is a 5-wire interface (TCK, TMS, TDI, TDO, nTRST) that allows both the boundary scan of the digital pins and the debug of the ARM7TDMI application when connected with the standard ARM7 developments tools. It is also used for the industrial test of the device. It is compliant with the JTAG IEEE Standard 1149.1.

2.13 RF/analog interfaces

2.13.1 BT RF port

The BT RF port is a differential port. In order to ensure the performances, typically a balanced band-pass filter needs to be connected to this port. A list of recommended filters is available on request. For RF performance and modem features, see *Section 4: "Bluetooth"*.

2.13.2 FM RF in and out

The FM RF input port and output port are differential ports. For RF performance and modem features, see *Section 5: "FM transceiver"*. Both FM_RFINx and FM_RFOUTx can be used as FM RX input ports. The STLC2690 includes an internal switch to connect the FM_RFOUTx to the FM TX or FM RX path. For more details see *Section 5.2.1: "Dual RF input with RX/TX antenna switch"*.

When using a loop antenna for FM TX, no external components are required.

For the FM receiver using the FM_RFINx as input port an external matching and blocking circuit is needed. For the FM receiver using the FM_RFOUTx as input port an external blocking circuit is needed, connected to the FM_RFINx pins.

2.13.3 FM analog audio in

A left and right analog audio input is available.

For audio performance and features, see *Section 5: "FM transceiver"*.

2.13.4 FM analog audio out

A left and right analog audio output is available.

For audio performances and features, see *Section 5: "FM transceiver"*.

2.14 GPIOs

Up to 22 GPIOs can be mapped to the programmable pins. These GPIOs can be used as generic output or input (interrupt) signals.

3 Bluetooth

3.1 Bluetooth functional description

3.1.1 Modem receiver

The Bluetooth subsystem implements a low-IF receiver for Bluetooth modulated input signals. The radio signal is taken from a balanced RF input and amplified by an LNA. The mixers are driven by two quadrature LO signals, which are locally generated from a VCO signal running at twice the frequency. The I and Q mixer output signals are band pass filtered by a poly-phase filter for channel filtering and image rejection. The band pass filter amplifies the signals to the optimal input range for the ADC. Further channel filtering is done in the digital part. The digital part demodulates the GFSK, π/4-DQPSK or 8-DPSK coded bit stream by evaluating the phase information. RSSI data is extracted. Overall automatic gain amplification in the receive path is controlled digitally. The RC time constants for the analog filters are automatically calibrated on chip.

3.1.2 Modem transmitter

The transmitter uses the serial transmit data from the Bluetooth controller. The transmitter modulator converts this data into GFSK, π/4-DQPSK or 8-DPSK modulated I and Q digital signals for respectively 1, 2 and 3 Mbps transmission speed. These signals are then converted to analog signals that are low pass filtered before up-conversion. The carrier frequency drift is limited by a closed loop PLL.

3.1.3 RF PLL

The on-chip VCO is part of a PLL. The tank resonator circuitry for the VCO is completely integrated without need of external components. Variations in the VCO center frequency are calibrated out automatically.

3.1.4 Bluetooth controller

V1.2 and V2.0 + EDR Features

The Bluetooth controller is backward compatible with the Bluetooth specification V1.2 *[4]* and V2.0 + EDR *[3]*. Here below is a list with the main features of those specifications:

- Adaptive Frequency Hopping (AFH)
- Fast connection: interlaced scan for page and inquiry scan, answer FHS at first reception, RSSI used to limit range
- Extended SCO (eSCO) links: supports EV3, EV4 and EV5 packets
- Channel quality driven data rate change (CQDDR)
- QoS flush
- Synchronization: BT clocks are available at HCI level for synchronization of parallel applications on different Slaves
- L2CAP flow & error control
- LMP SCO handling
- Scatternet support
- 2 Mbps packet types
- ACL: 2-DH1, 2-DH3, 2-DH5
- eSCO: 2-EV3, 2-EV5
- 3 Mbps packet types
  - ACL: 3-DH1, 3-DH3, 3-DH5

- eSCO: 3-EV3, 3-EV5

Bluetooth controller V2.1 + EDR features

- Encryption pause/resume (EPR)
- Extended inquiry response (EIR)
- Link supervision time out (LSTO)
- Secure simple pairing (SSP)
- Sniff subrating (SSR)
- Quality of service (QoS)
  - Packet boundary flag (PBF)
  - Erroneous data delivery (ED)

Bluetooth controller V3.0 features

- Enhanced power control
- Read encryption key size

TX output power control

The Bluetooth subsystem supports output power control:

- With the standard TX power control algorithm enabled, the Bluetooth subsystem adapts its output power when a remote BT device supports the RSSI feature; this allows the remote device to measure the link strength and to request the Bluetooth subsystem to decrease/increase its output power. In case the remote device does not support the RSSI feature, the Bluetooth subsystem uses its ‘default’ output power level

The Bluetooth subsystem supports operation at Class 1 output power levels up to 10 dBm.

3.1.5 Main processor and memory

- ARM7TDMI
- On-chip RAM, including provision for patches
- On-chip ROM preloaded with
  - SW up to HCI
  - A2DP mediapacket encapsulation
- Patch RAM
  - The Bluetooth subsystem includes a HW block that allows patching of the ROM code.
  - Additionally, a SW patch mechanism allows replacing complete SW functions without changing the ROM image.
  - A part of the RAM memory is used for HW and SW patches.

3.1.6 CoProcessor

- Audio processor
- RAM, including provision for patches
- ROM, preloaded with
  - SBC encoding/decoding
- Patch RAM
  - a SW patch mechanism allows replacing complete SW functions without changing the ROM image.
  - A part of the RAM memory is used for SW patches.

3.1.7 Download of the SW parameter file

To change the device configuration a set of customizable parameters have been defined and put together in one file, the SW Parameter File. This SW Parameter File is downloaded at start-up into the Bluetooth subsystem.

Examples of parameters are: radio configuration, PCM settings etc.

The same HCI command is used to download the file containing the patches (both those for the SW and HW mechanism).

For a more detailed description of the SW Parameter File refer to *[16]*.

3.1.8 Pitch period error concealment (PPEC)

PPEC stands for pitch period error concealment. It is an algorithm and associated hardware used in the STLC2690 chip to improve the quality of voice transfer over the Bluetooth air channel. It provides for increased speech quality in the vicinity of interference, and improves the coexistence with WLAN. The algorithm works at the receiver side and has no implications at all on the implementation of the Bluetooth specification.

PPEC works as follows: whenever a received packet is completely lost, instead of muting the output some previously received CVSD samples are inserted. These inserted samples are retrieved from a buffer. The PPEC algorithm continuously analyzes the samples that were previously received, and it uses fundamental speech properties to determine which samples from the buffer need to be inserted. As samples are just replaced, the PPEC algorithm does not add any latency to the voice transfer.

3.1.9 Bluetooth – WLAN/WiMAX coexistence in collocated scenario

The coexistence interface uses up to 4 WLAN control signal pins, which can be mapped via the SW Parameter File download on different pins of the Bluetooth subsystem (see *Section 4.1.7: "Download of the SW parameter file"*).

The functionality of the 4 WLAN control signal pins depends on the selected algorithm, as explained below and summarized in *Table 24: "WLAN HW signal assignment"*.

Bluetooth and WLAN 802.11 technologies occupy the same 2.4 GHz ISM band. The Bluetooth subsystem implements a set of mechanisms to avoid interference in a collocated scenario.

The Bluetooth subsystem supports 5 different algorithms in order to provide efficient and flexible simultaneous functionality between the two technologies in collocated scenarios:

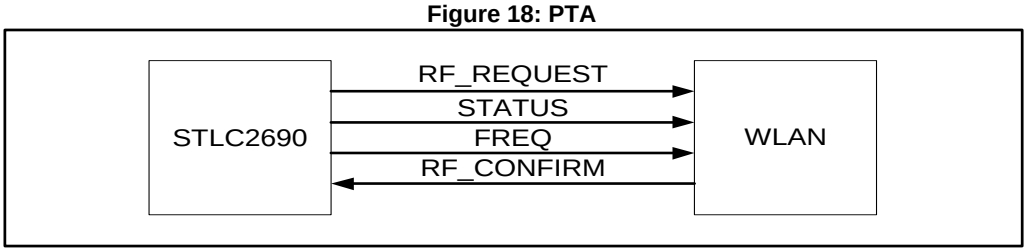
- **Algorithm 1:** PTA (packet traffic arbitration) based coexistence algorithm defined in accordance with the IEEE 802.15.2 recommended practice *[7]*.
- **Algorithm 2:** the WLAN is the Master and it indicates to the Bluetooth subsystem when not to operate in case of simultaneous use of the air interface.
- **Algorithm 3:** the Bluetooth subsystem is the Master and it indicates to the WLAN chip when not to operate in case of simultaneous use of the air interface.
- **Algorithm 4:** Two-wire mechanism
- **Algorithm 5:** Alternating wireless medium access (AWMA), defined in accordance with the WLAN 802.11 technologies.

The algorithm is selected via an HCI command. The default algorithm is algorithm 1.

Algorithm 1: PTA (packet traffic arbitration)

The algorithm is based on a bus connection between the Bluetooth subsystem and the WLAN chip:

Figure 18: PTA



By using this coexistence interface it is possible to dynamically allocate bandwidth to the two devices when simultaneous operations are required while the full bandwidth can be allocated to one of them in case the other one does not require activity.

The algorithm involves

- a priority mechanism, which allows preserving the quality of certain types of link.
- a mechanism to indicate that a periodic communication is ongoing.

A typical application would be to guarantee optimal quality to the Bluetooth voice communication while an intensive WLAN communication is ongoing.

Several algorithms have been implemented in order to provide a maximum of flexibility and efficiency for the priority handling. ST specific HCI commands are implemented to select the algorithm and to tune the priority handling.

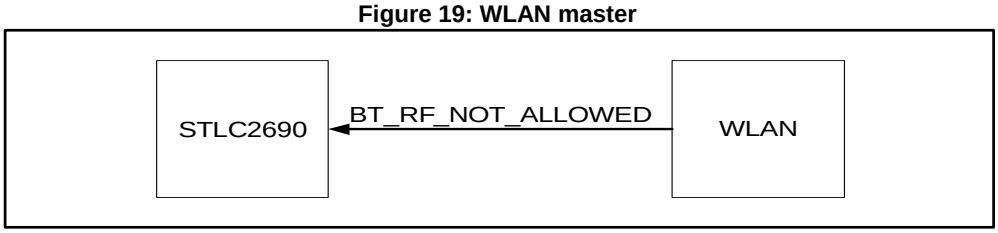
The combination of time division multiplexing and the priority mechanism avoids the interference due to packet collision. It also allows the maximization of the 2.4 GHz ISM bandwidth usage for both devices while preserving the quality of some critical types of link.

Algorithm 2: WLAN master

In case the Bluetooth subsystem has to cooperate, in a collocated scenario, with a WLAN chip not supporting a PTA based algorithm, it is possible to put in place a simpler mechanism.

The interface is reduced to 1 line:

Figure 19: WLAN master



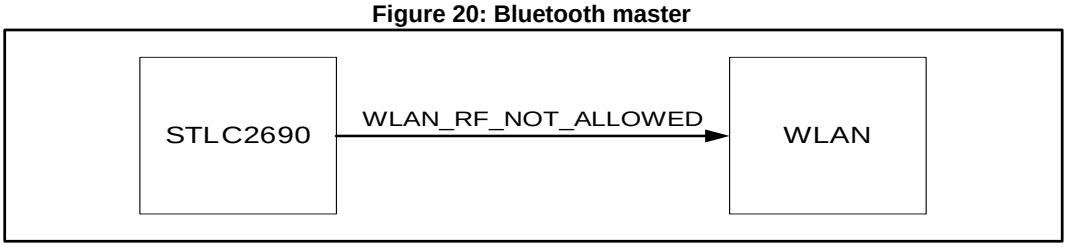
When the WLAN has to operate, it alerts high the BT_RF_NOT_ALLOWED signal and the Bluetooth subsystem does not operate while this signal stays high.

This mechanism permits to avoid packet collision in order to make an efficient use of the bandwidth but cannot provide guaranteed quality over the Bluetooth links.

Algorithm 3: Bluetooth Master

This algorithm represents the symmetrical case of algorithm 2. Also in this case the interface is reduced to 1 line:

Figure 20: Bluetooth master



When the Bluetooth subsystem has to operate it alerts high the WLAN_RF_NOT_ALLOWED signal and the WLAN does not operate while this signal stays high.

This mechanism permits to avoid packet collision in order to make an efficient use of the bandwidth, it provides high quality for all Bluetooth links but cannot provide guaranteed quality over the WLAN links.

Algorithm 4: Two-wire mechanism

Based on algorithm 2 and 3, the Host decides, on a case-by-case basis, whether WLAN or Bluetooth is Master. The Master role can be checked and changed at run-time by the Host via an HCI command.

Algorithm 5: Alternating wireless medium access (AWMA)

AWMA utilizes a portion of the WLAN beacon interval for Bluetooth operations. From a timing perspective, the medium assignment alternates between usage following WLAN procedures and usage following Bluetooth procedures.

The timing synchronization between the WLAN and the Bluetooth subsystem is done by the HW signal MEDIUM_FREE.

WiMax co-existence interface

The WiMax co-existence interface connects a single wire between the STLC2690 and the WiMax controllers. The goal of the WiMax PTA implementation is to protect the traffic in the WiMax licensed bands adjacent to both ends of the 2.4 GHz ISM band used by Bluetooth. The WiMax disable pin is interpreted as a request to immediately shut down any ongoing or scheduled RF activity on the Bluetooth side. The WiMax system should assert this pin each time the Wimax RX activity takes place. The disable pin is directly connected to the BT radio control and BT shutdown can happen in less than 20 µs.

WLAN HW signal assignment

Table 24: WLAN HW signal assignment

WLAN control signal	Scenario 1: PTA	Scenario 2: WLAN Master	Scenario 3: BT Master	Scenario 4: 2-wire	Scenario 5: AWMA
WLAN 1	RF_CONFIRM	BT_RF_NOT_ALLOWED	Not used	BT_RF_NOT_ALLOWED	MEDIUM_FREE
WLAN 2	RF_REQUEST	Not used	WLAN_RF_NOT_ALLOWED	WLAN_RF_NOT_ALLOWED	Not used
WLAN 3	STATUS	Not used	Not used	Not used	Not used
WLAN 4	FREQ (optional)	Not used	Not used	Not used	Not used

3.2 Bluetooth RF performance

All the values are provided according to the Bluetooth specification V3.0 unless otherwise specified.

3.2.1 Receiver

All specifications below are given at device pin level and with the conditions as specified. Parameters are given for each of the 3 modulation types supported.

(Typical is defined at T_{amb} = 25 °C, VDD_HV_x = 1.8 V. Minimum and maximum are worst cases over corner lots and temperature. Parameters are given at device pin, except for receiver interferers measured at antenna with a filter having a typical attenuation of 2.3 dB, for filter details see *[12]*. Measured with an impedance of 26+j32 at the IC pins (this impedance is at 25 degrees, at low/high temp the impedance is changing with temperature).)

Table 25: 1 Mbps receiver parameters - GFSK

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
RFin	Input frequency range		2402		2480	MHz
RXsensC	Receiver sensitivity (Clean transmitter)	@ BER 0.1%	-92.5	-91	-86.5	dBm
RXsensD	Receiver sensitivity (Dirty transmitter(1))	@ BER 0.1%	-91.5	-90	-86	dBm
RXmax	Maximum useable input signal level	@ BER 0.1%	10		10	dBm
Receiver blocking performance @ BER 0.1% on channel 58 (without filter)						
	CW signal in GSM band 900 MHz (824 MHz to 960 MHz)	@ Input signal strength = -67 dBm		-7		dBm
	CW signal in GSM band 1800 MHz (1805 MHz to 1990 MHz)	@ Input signal strength = -67 dBm		-3		dBm
	CW signal in WCDMA band (2010 MHz to 2170 MHz)	@ Input signal strength = -67 dBm		-1		dBm
Receiver interferer performance @ BER 0.1%						
$C/I_{co\text{-}channel}$	Co-channel interference	@ Input signal strength = -60 dBm		8.5	10	dB
C/I_{1MHz}	Adjacent (±1 MHz) interference	@ Input signal strength = -60 dBm		-9	0	dB
C/I_{+2MHz}	Adjacent (+2 MHz) interference	@ Input signal strength = -60 dBm		-39	-30	dB
C/I_{-2MHz}	Adjacent (-2 MHz) interference	@ Input signal strength = -67 dBm		-25	-9	dB
C/I_{+3MHz}	Adjacent (+3 MHz) interference	@ Input signal strength = -67 dBm		-46.5	-40	dB
C/I_{-3MHz}	Adjacent (-3 MHz) interference	@ Input signal strength = -67 dBm		-43	-20	dB
$C/I_{\geq 4MHz}$	Adjacent (≥ ±4 MHz) interference	@ Input signal strength = -67 dBm		-45	-40	dB

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Receiver inter-modulation						
IMD	Inter-modulation	Measured as defined in BT test specification *[6]*	-39	-32.3		dBm

Notes:

(1) Dirty transmitter including carrier frequency drift, as defined in the BT SIG spec *[6]*.

(Typical is defined at T_{amb} = 25 °C, VDD_HV_x = 1.8 V. Minimum and maximum are worst cases over corner lots and temperature. Parameters are given at device pin, except for receiver interferers measured at antenna with a filter having a typical attenuation of 2.3 dB, for filter details see *[12]*. Measured with an impedance of 26+j32 at the IC pins (this impedance is at 25 degrees, at low/high temp the impedance changes with temperature).)

Table 26: 2 Mbps receiver parameters - π/4-DQPSK

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
RFin	Input frequency range		2402		2480	MHz
RXsensC	Receiver sensitivity (Clean transmitter)	@ BER 0.01%	-91.5	-90	-86	dBm
RXsensD	Receiver sensitivity (Dirty transmitter(1))	@ BER 0.01%	-91	-89.5	-85.5	dBm
RXmax	Maximum useable input signal level	@ BER 0.1%		6		dBm
Receiver blocking performance @ BER 0.1% on channel 58 (without filter)						
	CW signal in GSM band 900 MHz (824 MHz to 960 MHz)	@ Input signal strength = -67 dBm		-6		dBm
	CW signal in GSM band 1800 MHz (1805 MHz to 1990 MHz)	@ Input signal strength = -67 dBm		-1		dBm
	CW signal in WCDMA band (2010 MHz to 2170 MHz)	@ Input signal strength = -67 dBm		1		dBm
Receiver interferer performance @ BER 0.1%						
$C/I_{co\text{-}channel}$	Co-channel interference	@ Input signal strength = -60 dBm		11.8	13	dB
C/I_{1MHz}	Adjacent (±1 MHz) interference	@ Input signal strength = -60 dBm		-15	0	dB
C/I_{+2MHz}	Adjacent (+2 MHz) interference	@ Input signal strength = -60 dBm		-40	-30	dB
C/I_{-2MHz}	Adjacent (-2 MHz) interference	@ Input signal strength = -67 dBm		-20	-7	dB
C/I_{+3MHz}	Adjacent (+3 MHz) interference	@ Input signal strength = -67 dBm		-48.5	-40	dB
C/I_{-3MHz}	Adjacent (-3 MHz) interference	@ Input signal strength = -67 dBm		-47	-20	dB

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$C/I_{\geq 4MHz}$	Adjacent (≥ ±4 MHz) interference	@ Input signal strength = -67 dBm		-47	-40	dB

Notes:

(1) Dirty transmitter including carrier frequency drift, as defined in the BT SIG spec *[6]*.

(Typical is defined at T_{amb} = 25 °C, VDD_HV_x = 1.8 V. Minimum and maximum are worst cases over corner lots and temperature. Parameters are given at device pin, except for receiver interferers measured at antenna with a filter having a typical attenuation of 2.3 dB, for filter details see *[12]*. Measured with an impedance of 26+j32 at the IC pins (this impedance is at 25 degrees, at low/high temp the impedance changes with temperature).)

Table 27: 3 Mbps receiver parameters - 8-DPSK

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
RFin	Input frequency range		2402		2480	MHz
RXsensC	Receiver sensitivity (Clean transmitter)	@ BER 0.01%	-85	-83	-78.5	dBm
RXsensD	Receiver sensitivity (Dirty transmitter(1))	@ BER 0.01%	-84	-82	-77.5	dBm
RXmax	Maximum useable input signal level	@ BER 0.1%		-3		dBm
Receiver blocking performance @ BER 0.1% on channel 58 (without filter)						
	CW signal in GSM band 900 MHz (824 MHz to 960 MHz)	@ Input signal strength = -67 dBm		-11		dBm
	CW signal in GSM band 1800 MHz (1805 MHz to 1990 MHz)	@ Input signal strength = -67 dBm		-7		dBm
	CW signal in WCDMA band (2010 MHz to 2170 MHz)	@ Input signal strength = -67 dBm		-9		dBm
Receiver interferer performance @ BER 0.1%						
$C/I_{co\text{-}channel}$	Co-channel interference	@ Input signal strength = -60 dBm		19	21	dB
C/I_{1MHz}	Adjacent (±1 MHz) interference	@ Input signal strength = -60 dBm		-5	5	dB
C/I_{+2MHz}	Adjacent (+2 MHz) interference	@ Input signal strength = -60 dBm		-37	-25	dB
C/I_{-2MHz}	Adjacent (-2 MHz) interference	@ Input signal strength = -67 dBm		-12	0	dB
C/I_{+3MHz}	Adjacent (+3 MHz) interference	@ Input signal strength = -67 dBm		-46	-33	dB
C/I_{-3MHz}	Adjacent (-3 MHz) interference	@ Input signal strength = -67 dBm		-40	-13	dB
$C/I_{\geq 4MHz}$	Adjacent (≥ ±4 MHz) interference	@ Input signal strength = -67 dBm		-42	-33	dB

Notes:

(1) Dirty transmitter including carrier frequency drift, as defined in the BT SIG spec *[6]*.

3.2.2 Transmitter

(Unless otherwise stated, typical is defined at T_{amb} = 25 °C, VDD_HV_x = 1.8 V. Minimum and maximum are worst cases over corner lots and temperature. Parameters are given at device pin, except for in-band spurious measured at antenna with a filter having a typical attenuation of 2.3 dB, for filter details see *[12]*. Measured with an impedance of 26+j32 at the IC pins (this impedance is at 25 degrees, at low/high temp the impedance changes with temperature).)

Table 28: Transmitter Parameters

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
RFout	Output frequency range		2400		2483.5	MHz
RF transmit power						
TXpout (GFSK)	Maximum output power(1)	@ 2402 - 2480 MHz @ 25 °C	8	10	12	dBm
TXpout (GFSK)	Maximum output power(1)	@ 2402 - 2480 MHz @ worst cases over corner lots and temperature	7	10	13	dBm
TXprange (GFSK, π/4-DQPSK, 8-DPSK)	Power control range	@ 2402 - 2480 MHz		40		dB
	Resolution of power control(2)			0.25		dB
TXpout (π/4-DQPSK)	Maximum output power(1) (3)	@ 2402 - 2480 MHz @ 25 °C	5	7	9	dBm
TXpoutrel (π/4-DQPSK)	Relative transmit power(4)	@ 2402 - 2480 MHz	0	-0.5	-1	dB
TXpout (8-DPSK)	Maximum output power(1) (2)	@ 2402 - 2480 MHz @ 25 °C	5	7	9	dBm
TXpoutrel (8-DPSK)	Relative transmit power(3)	@ 2402 - 2480 MHz	0	-0.5	-1	dB
In-band spurious emissions(5)						
FCC	FCC's 20 dB BW			935	970	kHz
ACP_2	Channel offset = ±2 MHz			-39	-20	dBm
ACP_3	Channel offset = ±-3 MHz			-47	-40	dBm
ACP_4	Channel offset ≥ ±4 MHz			-50	-40	dBm
EDR_IBS_1	Channel offset = ±1 MHz (2 and 3 Mbps)			-27	-26	dBc
EDR_IBS_2	Channel offset = ±2 MHz (2 and 3 Mbps)			-28	-20	dBm

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
EDR_IBS_3	Channel offset = ±3 MHz (2 and 3 Mbps)			-44	-40	dBm
EDR_IBS_4	Channel offset = ±4 MHz (2 and 3 Mbps)			-47	-40	dBm
Initial carrier frequency tolerance (for an exact reference)						
ΔF	|f_TX-f0|		-75	0(6)	75	kHz
Carrier frequency stability(7)						
|Δf_s|	Carrier frequency stability			3.2	10	kHz
Carrier frequency drift(8)						
|Δf_p1|	One slot packet			12(5)	25	kHz
|Δf_p3|	Three slots packet			14(5)	40	kHz
|Δf_p5|	Five slots packet			14(5)	40	kHz
Carrier frequency drift rate(7)						
|Δf/50us|	Frequency drift rate			8	20	kHz/50µs
Modulation accuracy(6) (7) (9)						
Δf1avg	Maximum modulation		140	163	175	kHz
Δf2avg	Minimum modulation		115	140		kHz
Δf2avg/ Δf1avg			0.8	0.9		
	2-DH5 RMS DEVM			7.2	20	%
	2-DH5 99% DEVM				30	%
	2-DH5 Peak DEVM			17.5	35	%
	3-DH5 RMS DEVM			7.2	13	%
	3-DH5 99% DEVM				20	%
	3-DH5 Peak DEVM			15	25	%
TX out of band emissions						
E100	Emission in FM band (76-108 MHz)	(7) (10)		-123		dBm/Hz
E700	Emission in CDMA2000 band (776-794 MHz)	(7) (9)		-135		dBm/Hz
E850	Emission in GSM band (869-960 MHz)	(7) (9)		-134		dBm/Hz
E900	Emission in GSM band (925-960 MHz)	(7) (9)		-134		dBm/Hz
E1500	Emission in GPS band (1570-1580 MHz)	(7) (9)		-140		dBm/Hz
E1800	Emission in GSM band (1805-1880 MHz)	(7) (9)		-136		dBm/Hz
E1900	Emission in GSM band (1930-1990 MHz)	(7) (9)		-136		dBm/Hz

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
E2100	Emission in WCDMA band (2110-2170 MHz)	(7) (9)		-136		dBm/Hz
E2600	Emission in WCDMA band (2620-2690 MHz)	(7) (9)		-135		dBm/Hz
E5000	Emission in WLAN band (5150-5825 MHz)	(7) (9)		-130		dBm/Hz

Notes:

(1) Lower transmit power (i.e. Class 2) can be obtained by programming the radio init power table via the SW Parameter File download or an HCI command.

(2) The step size can be controlled via the SW Parameter File.

(3) Power of GFSK part.

(4) Relative power of EDR part compared to the GFSK part.

(5) At antenna with maximum output power, filter attenuation of 2.3 dB.

(6) Phase noise adds maximum [-10 kHz;10 kHz] for worst case clock 200 mVpp at 13 MHz.

(7) Worst case clock 200 mVpp at 13 MHz. Measurement according to EDR RF test spec V2.0.E.3 *[6]*.

(8) With maximum output power.

(9) Measured on reference schematic following layout recommendations.

(10) Transmitting DH5 packets.

3.3 Bluetooth interfaces

3.3.1 HCI transport layer

H4 UART transport layer

The HCI transport layer supported on the UART is the H4 transport layer defined by the SIG *[5]*. The HCI UART transport layer assumes that the UART communication is free from line errors.

The UART interface is defined in *Section 3.12.2: "UART interface"*.

Two ways to enter and exit the low power modes are supported (For more details, refer to *[15]*):

- H4 UART: using CLK_REQ_OUT_x, UART_RXD and UART_RTS.
- H4 UART with handshake: using CLK_REQ_OUT_1, BT_WAKEUP and HOST_WAKEUP.

Enhanced H4 SPI transport layer

The HCI transport layer supported on the SPI is the H4 transport layer defined by the SIG *[5]*. The HCI SPI transport layer assumes that the SPI communication is free from line errors.

In addition a messaging protocol is defined for controlling the Deep Sleep mode entry and wake-up. Three messages are defined: SLEEP, WAKEUP and WOKEN. For more details, refer to *[14]*.

The SPI interface is defined in *Section 3.12.4: "FM I2C interface"*.

One way to enter and exit the low power modes is supported (for more details, refer to *[14]*):

- Enhanced H4 SPI: using CLK_REQ_OUT_x and the SPI in band signaling.

(e)SCO over HCI

The STLC2690 supports synchronous data packet transfer ((e)SCO) over HCI.

3.3.2 BT audio interface

The Bluetooth subsystem of STLC2690 supports one audio interface which can be used for (e)SCO voice transmission and reception or for A2DP. This interface can be either the BT PCM or the BT I2S as defined in *Sections 2.12.5* and *2.12.8*

The interface is fully configurable by the Host via the SW Parameter File download and when a SCO connection or A2DP connection is started-up (in order to allow different configuration based on use case). It is possible to configure 2 SCO connections on the PCM interface taking advantage of the multi-port PCM support. The configuration of the PCM for the second SCO is not disturbing the first SCO connection.

For Bluetooth voice operation (PCM/I2S and (e)SCO), the interface always works at 8 kHz. However, it is possible to configure the interface to other frame rates like 16 or 32 kHz, and link it to an eSCO link operating at the same rate. In I2S mode, it is possible to exchange voice on the left or on the right channel only. When two (e)SCO are active, each SCO uses one of the channels. The channel which is not used is padded with ‘0’ on data out.

For A2DP operation, the I2S sample rate is configurable e.g. 44.1 or 48 kHz. The audio is SBC encoded and A2DP encapsulated in the STLC2690, before being transmitted over the BT link.

3.3.3 WLAN/WiMAX coexistence interface

The WLAN/WiMAX coexistence interface to a WLAN and/or WiMAX chip allows optimal coexistence between the two functions when collocated. This interface can contain 1 to 4 wires (WLAN1, WLAN2, WLAN3 and WLAN4). For more details refer to *Section 4.1.9: "Bluetooth – WLAN/WiMAX coexistence in collocated scenario"*. The 4 control signals are mapped on the pins as indicated in *Section 3.4.3: "Pin mapping"*.

3.3.4 GPIOs

Up to 22 GPIOs can be mapped to the pins. These GPIOs can be used as a generic output or input (interrupt) signals.

4 FM transceiver

4.1 FM functional description

The FM subsystem of the chip contains a full receiver function and a full transmitter function. The Host selects which function is performed. Note that the two functions cannot be active at the same time.

The FM subsystem is compliant with all relevant international and regional standards and regulations, e.g.

- ITU BS.450-3
- ETSI 301 357
- FCC part 15 and 73
- For the transmitter function, depending on the platform in which the STLC2690 is integrated, the maximum radiated output power can be adjusted by the host to be in line with the local regulations.

Both the receiver and the transmitter fully support RDS/RBDS. The RDS/RBDS is compliant with all relevant international and regional standards, e.g.

- CENELEC EN50067 (1992), CENELEC EN62106 (2001)
- NRSC RBDS (04/1998), NRSC 4 A (04/2005) and Annexes

The FM transceiver uses a low-IF receiver and a quadrature up-conversion transmitter.

The RF frequency is generated by an on-chip frequency locked loop (FLL).

A small embedded microcontroller manages the flexibility of the data path and the DSP parameters. It reduces the load on the host by taking care of the encapsulation (for the transmitter) and extraction (for the receiver) of RDS/RBDS messages. It also takes care of the overall control of the transceiver.

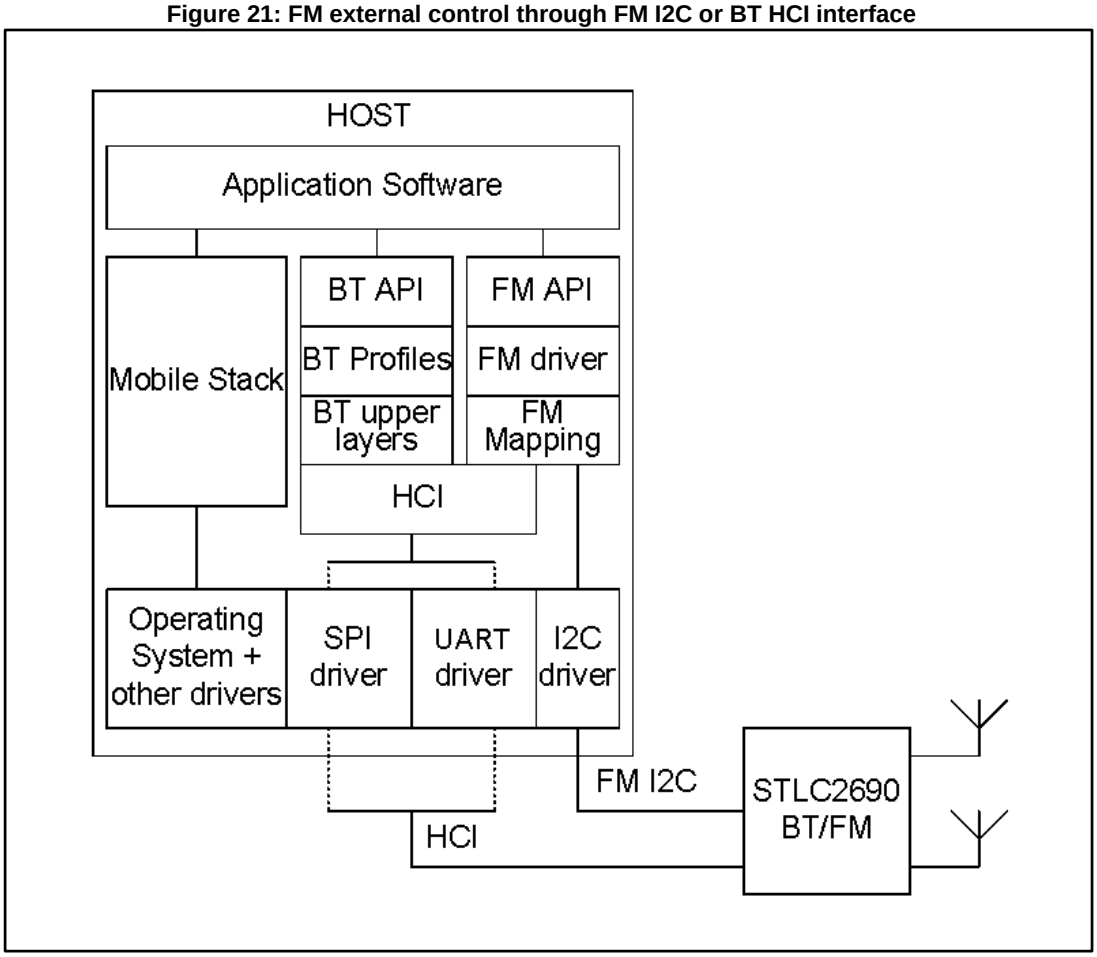
An integrated switch to connect either the FM transmitter or the FM receiver to an integrated FM antenna is available in the STLC2690.

4.1.1 FM external control

There are two alternatives to control the FM subsystem from the host side.

- The first way is to use the FM I2C interface.
- The second way is to control the FM subsystem over the Bluetooth HCI interface. Vendor-specific HCI commands and events have been defined for this purpose.

Figure 21: FM external control through FM I2C or BT HCI interface



The command encoding is exactly the same when using I2C or BT HCI such that the host driver can be the same for both.

As shown in not found19 a host-level API layer is offered in order to facilitate integration of the FM driver on the Host. This API consists of a limited set of primitives, hiding the details of the FM device. It also avoids polling, thereby reducing the load on the host. Source codes are provided for an example application as well as for the driver primitives itself.

As an example, the following primitives are offered:

- RadioBoot(<list of parameters>): to perform power-on of the FM subsystem and to perform platform dependent initialization
- RadioRxConfig(<list of parameters>): to configure different aspects of the receiver function
- RadioRxSetFreq(dwRxFrequency): to set the tuning frequency.

4.1.2 Interrupt to the host

In case the FM subsystem is controlled via I2C a dedicated signal on the chip, FM_IRQ, can be used as an interrupt line to the host. In order to map this signal to a pin of the chip a download of the Bluetooth parameter file is required. The interrupt line can be configured as an active high or active low signal.

In case the FM subsystem is controlled via HCI no hardware interrupt line needs to be used. Instead, the host is notified via a vendor-specific HCI event.

The interrupt (or event) can be generated for many functions in the FM subsystem, e.g. to signal the availability of information in the RDS data buffers. The host is able to configure when to generate an interrupt (or event) and for which function.

4.2 FM radio receiver

The receiver offers worldwide band support (65.9 MHz up to 108 MHz).

The receiver uses a low-IF architecture. The RF signal is down-converted, after which anti-aliasing filtering and coarse channel filtering is performed. An automatic gain control (AGC) circuit controls the gain of the input amplifier. A high resolution ADC then digitizes the baseband-analog signal for further digital signal processing.

Digital signal processing (DSP) involves channel selection, FM demodulation, stereo separation and RDS/RDBS processing. The DSP extracts additional information such as the RSSI level of the incoming signal and other quality characteristics This information is used by the embedded microprocessor for circumstantial control in order to optimize the user's audio experience on-the-fly.

As a reference clock the FM subsystem can either use the externally supplied slow clock or the fast clock supplied by the Bluetooth subsystem. The FM subsystem is in a handshaking process with the BT subsystem to exchange information on each other's power state and on the availability of reference clock sources. Optionally the FM subsystem can from time to time calibrate the slow clock using the fast clock, allowing for a larger inaccuracy of the slow clock.

4.2.1 Dual RF input with RX/TX antenna switch

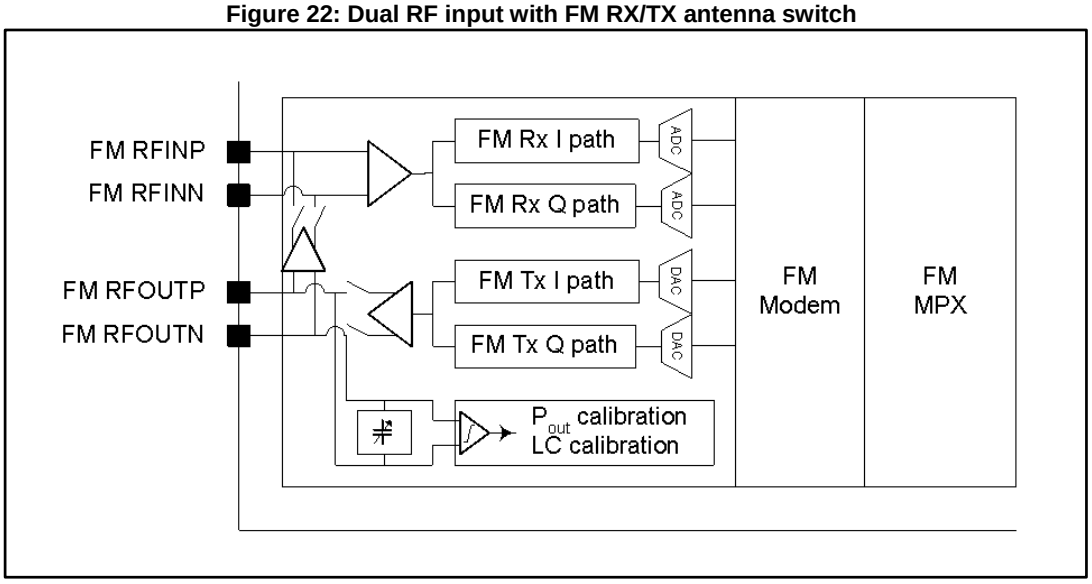
The STLC2690 supports two alternative RF inputs for the FM receiver:

- One RF input dedicated to the FM receiver, at pins FM_RFINP/FM_RFINN. This is a low-resistive input. This input is suited for external headset wire antennas. An external matching network is recommended to match to a typical headset wire antenna impedance and to fulfill blocking requirements, see *[13]*.
- One RF input shared with the FM transmitter, at pins FM_RFOUTP/FM_RFOUTN. This is a high- resistive and capacitive input. This input is suited for antennas integrated on the PCB. An internal switch inside the STLC2690 connects the pins FM_RFOUTP/FM_RFOUTN to the FM TX path or to the FM RX path. The STLC2690 integrates a tunable capacitor bank to perform an automatic calibration of the output power and the RF load including the antenna. An external matching network connected to FM_RFINP/FM_RFINN is recommended to fulfill blocking requirements, see *[13]*.
- Impedances and performances of the two RF inputs are listed in *Section 5.4.1: "FM radio receiver performance"*.

The implementation in STLC2690 (as depicted below) offers the following advantages:

- Isolation of the FM transmit path using a handset antenna towards the headset wire which can still be connected.
- Unchanged RF input impedance return loss in case of regular reception via a headset wire.
- High impedant RF input in case of reception via FM transmit antenna.

Figure 22: Dual RF input with FM RX/TX antenna switch



4.2.2 Receiver RF functions

Band selection

The chip can be configured either to the OIRT band (65.9 – 74 MHz), the Chinese band (70 – 108 MHz), the Japanese FM band (76 - 90 MHz), the Japanese FM wide band, the USA/Europe FM band (87.5 - 108 MHz) or to the worldwide band (70 - 108 MHz).

Scan up / scan down

An autonomous frequency scan can be requested. The scan stops when a station is found that exceeds the currently configured RSSI level. On top of the RSSI level the host can also impose a CNR value (Carrier-to-Noise Ratio) to be met.

Alternatively the PTY information can be used to stop the scan when a specified value is found. This value is configurable by the host.

The frequency step for the scan is programmable either to 30 kHz, 50 kHz, 100 kHz or 200 kHz.

RF AGC

The RF AGC prevents saturation and limits the amount of intermodulation products created by strong adjacent channels. The RF AGC is on by default but it can be turned off.

In addition there is an in-band AGC to prevent overloading by the wanted channel. The in-band AGC is always turned on.

Pre-demodulation RF bandwidth reduction

When the stereo blending function is activated and the signal level is close to sensitivity, the RF bandwidth is automatically, seamlessly reduced and the receiver is set in mono mode to improve the sensitivity by about 3 dB. The RF bandwidth reduction is on by default but it can be turned off.

RSSI level

The RSSI level can be retrieved by the host. It is also used internally for the Mute, Scan, Blend and Alternative Frequency functions. The information is low-pass filtered and the refresh cycle time can be configured.

Image detection

The image detector determines whether a received signal is from a true station, or is the image of a station after mixing.

The process is automatically enabled when the auto scan is running, but it can be switched off.

When an image is detected, an interrupt is generated if the FM frequency had been requested by the host. In autonomous mode (during a Scan or an Alternative Frequency), the interrupt is not generated.

4.2.3 Receiver audio functions

Volume control

The output level is adjustable by a simultaneous control of the left and right channel. The level can be set to 32 different levels in steps of 1.5 dB.

The volume control can be configured to apply to both analog and digital output simultaneously, or only to the analog output (providing a line-out function to the digital output).

Boost and audio equalizer

The equalizer can be configured either as a 3-band equalizer, by genre or according to the RDS PTY information. The genres are pre-defined and the following genres can be chosen: Normal (Speech), Classic, Rock and Pop.

When configured as a 3-band equalizer each band can be set at 15 different levels in steps of 1.5 dB, between -10.5 and +10.5 dB. The corner frequency for the low band is 300 Hz, the corner frequency for the high band is 3 kHz.

Soft mute

In case of low RF input levels the RSSI information, after being integrated and low-pass filtered, drives the soft mute attenuator. The audio output is faded when soft mute is being applied. The soft mute function can be switched off.

The RSSI level at which soft muting starts can be shifted up or down by 3 dB. See the following table for some parameters of the soft mute function.

Table 29: Soft mute parameters

Parameter	Conditions	Typical	Unit
Soft mute start level	Default mode (programmable +/- 3 dB)	10	dBµV
Soft mute attenuation	Vin = 0 dBµV, Δf_{audio} = 22.5 kHz, fmod = 1 kHz, L = R	14	dB

Audio mute

The left and right audio outputs can be muted completely. This can be done simultaneously but it can also be done for each channel individually.

Note that the audio output is automatically muted during an Alternative Frequency update.

Mono/Stereo configuration

The receiver can be set either to mono or to stereo.

The STLC2690 supports the pilot-tone system stereo decoding, it does not support polar-modulation stereo decoding.

Mono/Stereo indication

The receiver offers a mono/stereo indicator to the host. The indicator can be based either upon the measured pilot deviation or upon the degree of mono/stereo blending (see

below). In either case some hysteresis is used to avoid too frequent toggling of the indicator:

- in case the host configures the indicator to be based upon the pilot deviation, the indicator will toggle typically at 4.5 kHz (for increasing pilot deviation) or at 3 kHz (for decreasing pilot deviation).
- in case the host configures the indicator to be based upon the mono/stereo blending, the indicator will toggle when reaching 25% of stereo (for decreasing RSSI) or when reaching 75% of stereo (for increasing RSSI).

An interrupt can be configured to trigger when the indicator toggles.

Automatic audio bandwidth (high cut) control

An automatic audio bandwidth limitation can be set. This is used in case of low RSSI levels.

Signal dependent mono/stereo blending

As the RF input level drops the decoder makes a transition from stereo to mono in order to limit the output noise. This process is called blending. The transition can be smooth (in case gliding blending is configured) or fast (in case hard blending is configured).

Blending starts at a programmable threshold on the RF level (see the table below). The blending can also be switched off by the host.

Table 30: Mono/stereo blending parameters

Parameter	Conditions	Typical	Unit
Mono/stereo blend start level	Default mode (programmable +/- 3 dB)	42	dBµV

Adjacent channel detection

When a strong adjacent channel is about to interfere with the wanted signal, the RF bandwidth is seamlessly reduced. This option is enabled by default, but can be switched off.

4.2.4 Receiver RDS/RBDS support

RDS/RBDS decoder

In order to minimize the load on the host RDS/RBDS synchronization, error correction (whenever possible) and block identification are performed locally. The same is done for some specific RDS/RBDS information.

The host is able to set some parameters for acquisition, maintenance and loss of synchronization.

Up to a maximum of 85 blocks can be stored locally, including an extra 8 bits per block for status signaling: block identification (3 bits), error status (3 bits), FIFO status (1 bit) and a spare bit.

When the FIFO capacity reaches a certain configurable level an interrupt is generated to notify the host, so when the interrupt is received on a regular basis the host can download the complete RDS memory.

not found29 shows the processing that is embedded inside the chip so as to avoid frequent access to the host.

All RDS data, including the data that are not present in not found29, are still stored inside the chip and can be sent to the host upon request.

Table 31: RDS/RBDS data processed inside the chip

Acronym	Name	Note
AF	Alternative frequency	(1)
EON	Enhanced other network	(2)(3)
MS	Music speech	(3)
PI	Program identification	(1)
PTY	Program type	(3)
PTYN	Program type name	
TA	Traffic announcement	(4)
TP	Traffic program	(2)
CT	Clock time and date	
DI	Decoder identification	
ECC	Extended country code	
PIN	Program item number	
PS	Program service	
RT	Radio text	
RT+	Radio text plus as defined in *[8]*	

Notes:

(1) This is used in AF processing

(2) Equalizer can be programmed to automatically adapt to the music genre

(3) Used for TA/TP switching, for temporary switching to another RF channel when it broadcasts a traffic announcement

(4) Specifically used during automatic scan

Alternative frequency (AF)

The receiver can autonomously change the tuning frequency to the Alternative frequency which provides the same or an equivalent program of the same radio network with a better quality.

In this autonomous mode the receiver performs AF list acquisition, checks the quality of the station(s) at the alternative frequency(ies), performs image detection and checks the PI code. All these actions, including switching back to the original frequency in case the alternative frequency(ies) do not prove to be adequate, are completed within a time of 15 ms except for the PI check.

The AF feature can be switched off. The RSSI threshold level below which the process is started, can be configured. In order to avoid continuous switching the minimum RSSI level expected at the Alternative frequency can also be configured.

Audio pause detector

The pause detection is used to perform inaudible frequency jumps during silences. The detection is based on the sum of left and right channels with a programmable threshold on the audio level, specified in terms of corresponding FM deviation.

The pause time, being the minimum duration of an audio silence for the receiver to accept it as a valid pause, can be programmed.

The pause detector can be disabled. In that case the AF switch is triggered immediately when the RSSI drops below the configured threshold.

4.3 FM radio transmitter

The transmitter offers worldwide band support (76 MHz up to 108 MHz).

The transmitter circuit uses digital signal processing (DSP) to generate a stereo MPX signal, perform FM modulation and quadrature signal generation. After converting both quadrature signals to an analog signal, an up-converting mixer followed by a power amplifier produces the RF signal. The transmitter has extra filtering as to ensure coexistence with existing wireless applications in a handset. It has calibration circuits and variable gain in the transmit path to establish the correct output power. A tunable capacitor array is used to tune the antenna circuit.

The transmitter supports RDS/RDBS message handling.

The transmitter may run from the externally applied low power reference clock (in this case the embedded microprocessor should receive information on the clock inaccuracy to compensate for). It can also be configured to run from the fast clock supplied from the Bluetooth subsystem. Optionally the FM subsystem can from time to time calibrate the slow clock using the fast clock, allowing for a larger in accuracy of the slow clock.

4.3.1 SureTune™

The STLC2690 supports SureTune™ technology. This technology features a microprocessor controlled, fast auto search algorithm to identify suitable transmit frequencies at a 50, 100 or 200 kHz grid. The tuner in the transceiver scans the FM band in a few seconds. Based on the acquired information, the embedded microcontroller then determines the best transmit frequency, after which transmission can start. Several TX channel presets can be stored in memory. The frequency scan on FM RX can be done either on FM_RFINx or FM_RFOUTx, depending on the configuration, see *Section 5.2.1: "Dual RF input with RX/TX antenna switch"*.

4.3.2 Transmitter audio functions

Programmable analog input range

Three different analog input ranges are supported: 92 mVpeak, 147 mVpeak and 234 mVpeak.

MPX multiplexing

The following independent configurations to the MPX signal are possible:

- mono or stereo
- audio present or not
- pilot present or not
- RDS/RBDS present or not.

Pre-emphasis

The pre-emphasis can be set to either 50 or 75 µs.

Digital AGC/limiter

The digital part contains an AGC and a limiter to prevent overmodulation. The AGC has a peak detector with a programmable threshold and time constant. The limiter implements saturation at a programmable level.

Programmable maximum FM deviation

The maximum FM deviation can be programmed to a value of up to 100 kHz.

Programmable gains

The gains can be set separately for the audio signal and the RDS/RBDS component.

4.3.3 Transmitter RF functions

Programmable transmit level

The default transmit level is 120 dBµV peak in differential mode. A gain range of -30 to 0 dB is available.

Simultaneous transmission on two FM channels

The same MPX signal can be transmitted on two different RF frequencies. This allows an FM receiver to switch to an alternative frequency with better reception of the same broadcast source. The spacing between both FM channels is programmable, with a typical setting of 1.6 MHz. In this case the peak output power is equal to the one of a single FM channel, however divided over the two channels.

Automatic calibration

The transmitter performs an automatic calibration of the output power and the RF load including the antenna, by tuning a programmable capacitor bank at the RF output.

This tuning can be done periodically during operation, without audible effects.

4.3.4 Transmitter RDS/RBDS support

The programmable RDS/RBDS is compliant with international and regional standards:

- CENELEC EN50067 (1992), CENELEC EN62106 (2001)
- NRSC RBDS (04/1998), NRSC 4 A (04/2005) and Annexes

The transmitter supports RDS/RDBS message handling in a versatile way. It takes care of block framing and error coding, but also the scheduling and repeated transmission of a large series of blocks can be left to its embedded microcontroller if desired. In that case the same types or RDS/RBDS data are supported as for the receiver, including RT+, see not found29, except for TA/TP.

4.4 FM radio performance

4.4.1 FM radio receiver performance

(Typical is defined at T_{amb} = 25 °C, VDD_HV_x = 1.8 V. Minimum and maximum are worst cases over corner lots and temperature.)

Table 32: FM radio receiver performance

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
FM general parameters *(1)(2)(3)*						
F_{RF}	Operating frequency	At FM_RFINx	65.9		108	MHz
F_{RF}	Operating frequency	At FM_RFOUTx	76		108	MHz

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
S/Nmax	Maximum (S+N)/N	Mono *(4)(5)*		63		dB
S/Nmax	Maximum (S+N)/N	Stereo *(6)(3)*		58		dB
US	Useable max sensitivity	50 Ω matching network, @FM_RFINx, see section *4.2.1* (S+N)/N = 26 dB, T_{amb} = 25 °C *(1)*		-2	1 *(7)*	dBµV
US	Useable max sensitivity	50 Ω matching network, @FM_RFINx, see section *4.2.1* (S+N)/N = 26 dB, full temperature range *(1)*		-2	5 *(7)*	dBµV
US intermediate	Useable intermediate sensitivity	50 Ω matching network, @FM_RFINx, see section *4.2.1* (S+N)/N = 45 dB *(1)*		11		dBµV
Sel@200k	Selectivity	Interferer at ±200 kHz, measured as per EN55020	43			dB
Sel@400k	Selectivity	Interferer at ±400 kHz, measured as per EN55020	52			dB
IIP3	Overall input third order intercept point	Interferers at ±200 kHz, ±400 kHz, AGC OFF, Gain set at GMAX, at S+N)/N = 26 dB	85	90		dBµV
IIP3	Overall input third order intercept point	Interferers at ±1, ±2 MHz, AGC OFF Gain set at GMIN, at S+N)/N = 26 dB	130	135		dBµV
IIP3	Overall input third order intercept point	Interferers at ±1, ±2 MHz, AGC OFF Gain set at GMAX, at S+N)/N = 26 dB	85	88		dBµV
AM suppr	AM suppression	*(1) (3)*	58	67		dB
RDS S @1.2kHz	RDS sensitivity	50 Ω matching network, @FM_RFINx, see section *4.2.1* Δf_{RDS} = 1.2 kHz, L = -R 95% of blocks decoded with no errors, taken over 5000 blocks *(2)*		21	22	dBµV
RDS S @2kHz	RDS sensitivity	50 Ω matching network, @FM_RFINx, see section *4.2.1* Δf_{RDS} = 2 kHz, L = -R 95% of blocks decoded with no errors, taken over 5000 blocks *(2)*		16	18	dBµV
RDS Sel@200k	RDS selectivity at ±200 kHz	Wanted RF level = RDS sensitivity (S) + 3 dB, conditions as for RDS S @ 2 kHz Interferer: Δf = 40 kHz, fmod = 1 kHz	S + 20			dBµV

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
RDS Sel@400k	RDS selectivity at ±400 kHz	Wanted RF level = RDS sensitivity (S) + 3 dB, conditions as for RDS S @ 2 kHz Interferer: Δf = 40 kHz, fmod = 1 kHz	S + 40			dBµV
RF *(4) (5) (6)*						
R_{FM_RFIN}	RF input resistance	Differential at pins, @FM_RFINx, see section *4.2.1*		200		Ω
$V_{RF,max}$	RF maximum input level	Maximum input level, audio parameters are met.			105	dBµV
	RF blocking levels (at antenna input)	FM sensitivity degraded with 1 dB. With 5 component 50 Ω matching network, @FM_RFINx, see section *4.2.1* 824 – 915 MHz (modulations: EDGE, CDMA)		10		dBm
	RF blocking levels (at antenna input)	FM sensitivity degraded with 1 dB. With 5 component 50 Ω matching network, @FM_RFINx, see section *4.2.1* 1710 – 1980 MHz (modulations: EDGE, CDMA,WCDMA)		10		dBm
	RF blocking levels (at antenna input)	FM sensitivity degraded with 1 dB. With 5 component 50 Ω matching network, @FM_RFINx, see section *4.2.1* 2400 – 2483.5 MHz (modulations: BT, WLAN)		8		dBm
Stereo decoder and base band when in digital or analog output mode *(4) (5) (6)*						
THD	Total harmonic distortion	Mono, Df_{audio} = 75 kHz, not A-weighted *(1) (3)*		0.08	0.1	%
THD	Total harmonic distortion	Stereo, Df_{audio} = 67.5 kHz, not A-weighted *(2) (3)*		0.07	0.13	%
THD	Total harmonic distortion	Mono, Df_{audio} = 100 kHz, not A-weighted *(2) (3)*		0.07	0.15	%
AudSpur	Audio spurious products	*(1) (3)*			-60	dBc
StereoSep	Stereo separation	Stereo blending OFF, 32 dBµV input level, Df_{audio} = 67.5 kHz, R = 0, L = 1 *(2)*	43	44		dB
PilotSup	Pilot suppression	Stereo, Df_{audio} = 67.5 kHz, without 15 kHz LP filter in the audio analyzer, absolute value (i.e. difference between 1kHz(3) tone and pilot tone after filtering) *(2)*	80			dB
$T_{deemphasis}$	De-emphasis time constant		73	75	77	µs
$T_{deemphasis}$	De-emphasis time constant		49	50	51	µs
AudioMute	Audio soft muting attenuation	When FM function enabled and in auto-search or when soft mute active	60			dB

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Analog Audio outputs only (4) (5) (6)						
VAF	Audio output level	Rload > 30 kΩ, Df_{audio} = 22.5 kHz Mono(1) and stereo(2) (3)	61	69	71	mVrms
VAFmax	Maximum audio output level	Rload > 30 kΩ, Df_{audio} = 100 kHz Mono(1) (3)	293	307	315	mVrms
VAFL/VAFR	Audio left/right channel imbalance	(2) (3) at high volume levels	-0.1		0.1	dB
BW	Upper audio bandwidth (-3 dB point)	for both $T_{deemphasis}$ = 75 µs and 50 µs (3)	15.2			kHz
BW	Lower audio bandwidth (-3 dB point)	for both $T_{deemphasis}$ = 75 µs and 50 µs (3)			10	Hz
	Audio response flatness	100 Hz to 13 kHz, for both $T_{deemphasis}$ = 75 µs and 50 µs, pre-emphasis applied, after de-emphasis (3)			±0.8	dB
	Audio output impedance	When FM function enabled and in auto-search or when soft mute active			50	Ω
Digital audio outputs only (4) (5) (6)						
VAF	Audio output level	Mono(1) ,Δf_{audio} = 75 kHz		-7.5		dB/fullscale
Fs	Audio output sample rate		8		192	kHz
Synthesizer (4) (5) (6)						
Fstep	Minimum frequency step		30		200	kHz
Tsweep	Sweep time	Total time taken for an automatic search to sweep from 88 to 108 MHz or 76 to 90 MHz (or reverse direction) assuming no channels found.			5	s
RSSI level (4) (5) (6)						
Range	Range		10		60	dBµV
ΔL	Relative level error				±1	dB
ΔL	Absolute level error				±3	dB

Notes:

(1) F_{RF} = 65.9 to 108 MHz, unless otherwise stated

(2) with 15 kHz LP filter in the audio analyzer, A-weighted, unless otherwise stated

(3) @FM_RFINx and with a 50 Ω matching network, see section *4.2.1* , unless otherwise stated

(4) Mono, Δf_{audio} = 22.5 kHz, fmod = 1 kHz, unless otherwise stated

(5) Vin = 60 dBµV

(6) Stereo, Δf_{audio} = 22.5 kHz, fmod = 1 kHz, Δf_{Pilot} = 6.75 kHz, L = R, no RDS, unless otherwise stated

(7) Depending on application conditions, when BT is enabled, at 2 FM frequencies exceptions might occur.

4.4.2 FM radio transmitter performance

(Typical is defined at T_{amb} = 25 °C, VDD_HV_x = 1.8 V. Minimum and maximum are worst cases over corner lots and temperature.)

Table 33: FM radio transmitter performance

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
FM general parameters						
F_{RF}	Operating frequency		76		108	MHz
Synthesizer						
Fstep	Frequency step		50		200	kHz
	Frequency accuracy (1)		-10		10	kHz
RF output						
	Maximum spacing of dual FM TX channels	The spacing is programmable		1.6		MHz
	Maximum transmit output level	With as load a loop antenna with inductance of 120 - 150 nH and a minimum Q of 30		120		dBµVpdiff
	Gain range	With as load a loop antenna with inductance of 120 - 150 nH and a minimum Q of 30.	-28		0	dB
	Gain step at high output levels		0.4	1	1.6	dB
	Transmitter output accuracy	Over entire output power range	-1		1	dB
	Load inductance range that can be supported	F_{RF} = 76 to 108 MHz, with a minimum Q of 30, without external capacitance added	120		150	nH
	Occupied BW	± 100 kHz offset from nominal channel frequency			-20	dBc
ACP	Adjacent channel power, at max output power, single FM TX channel	> ±120 kHz		-35	-30	dBc
	Transmitter noise floor (4) (2)(3)(4)	746 - 764 MHz		-140		dBm/Hz
	Transmitter noise floor (4) (5) (6) (8)	869 - 894 MHz, 925 - 960 MHz, 1805 - 1880 MHz, 1930 - 1990 MHz		-140		dBm/Hz
	Transmitter noise floor(5)(5) (6) (8)	2110 - 2170 MHz		-140		dBm/Hz
	Transmitter noise floor (4) (5) (6) (8)	1570 - 1580 MHz		-140		dBm/Hz
	Transmitter spurious (4) (5) (6) (8)	746 - 764 MHz		-99		dBm
	Transmitter spurious (4) (5) (6) (8)	869 - 894 MHz, 925 - 960 MHz, 1805 - 1880 MHz, 1930 - 1990 MHz		-109		dBm

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
	Transmitter spurious (4) (5) (6) (8)	2110 - 2170 MHz		-96		dBm
	Transmitter spurious (4) (5) (6) (8)	1570 - 1580 MHz		-106		dBm
Analog audio input						
VAF1	Analog audio input level(6)	Mono(7), Δf_{audio} = 75 kHz Stereo(8), Δf_{audio} = 67.5 kHz with input gain step 1			78	mVp
VAF1	Analog audio input level(7)	Mono(1) , Δf_{audio} = 75 kHz Stereo(2) , Δf_{audio} = 67.5 kHz with input gain step 2			134	mVp
VAF1	Analog audio input level(7)	Mono(1) ,Δf_{audio} = 75 kHz Stereo(2) , Δf_{audio} = 67.5 kHz with input gain step 3			212	mVp
ZAF	Analog Input impedance			25		kΩ
Digital audio input (I2S)						
	Audio input level	Mono(1) ,Δf_{audio} = 75 kHz Stereo(2) , Δf_{audio} = 67.5 kHz		-6		dB/fullscale
Fs	Audio input sample rate		8		192	kHz
Stereo encoder and base band						
Δf	Total peak deviation	Absolute maximum peak deviation - programmable		75	100	kHz
Δf_{Pilot}	Pilot deviation	Relative to maximum peak deviation - programmable	8		10	%
Δf_{RDS}	RDS deviation	Absolute maximum peak deviation - programmable		1.2	10	kHz
	Transmitted deviation flatness	Stereo(2) , Δf_{audio} = 67.5 kHz over F_{RF} = 76 - 108 MHz			±1	dB
	Channel imbalance	Stereo(2)	-1		1	dB
	Stereo separation	Stereo(2) , R = 0, L = 1	30	42		dB
	Lower sudio bandwidth (-3 dB point)	For both $T_{preemphasis}$ = 75 µs and 50 µs.			50	Hz
	Upper audio bandwidth (-3 dB point)	For both $T_{preemphasis}$ = 75 µs and 50 µs, for analog audio input or digital audio input with sample rates Fs ≥ 32 kHz	15			kHz
	Upper audio bandwidth (-3 dB point)	for digital audio input with sample rates Fs < 32 kHz	0.8 * Fnyq			kHz
	Audio response flatness	100 Hz to 13 kHz, for both $T_{preemphasis}$ = 75 µs and 50 µs, pre-emphasis applied, measured after de-emphasis, for sample rates > 32 kHz	-1.5		+1.5	dB
$T_{preemphasis}$	Pre-emphasis time constant high value			75		µs

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$T_{preemphasis}$	Pre-emphasis time constant low value			50		µs
	Pre-emphasis time constant tolerance				±5	%
THDdig	Total harmonic distortion for digital input	Stereo(2) , Δf_{audio} = 67.5 kHz		0.07	1	%
THDana	Total harmonic distortion for analog input	Stereo(2) , Δf_{audio} = 67.5 kHz		0.18	1	%
S/Nmono,d	Transmitted S/N for mono for digital input	Mono(1) for digital input. A-weighted filter on RX measurement equipment.	60			dB
S/Nmono,a	Transmitted S/N for mono for analog input	Mono(1) for analog input. A-weighted filter on RX measurement equipment.	56.5			dB
S/Nstereo,d	Transmitted S/N for stereo for digital input	Stereo(2) (7) for digital input. A-weighted filter on RX measurement equipment.	57			dB
S/Nstereo,a	Transmitted S/N for stereo for analog input	Stereo(2) (7) for analog input. A-weighted filter on RX measurement equipment.	54			dB
	Audio spurious products	Mono(1) , F_{RF} = 76 to 108 MHz			-60	dBc

Notes:

(1) For use of the slow clock for FM, in case the accuracy of the externally applied slow clock is not sufficient, the STLC2690 provides a calibration mechanism to calibrate the slow clock versus the fast clock.

(2) With as load a loop antenna with inductance of 120 - 150 nH and a minimum Q of 30 .

(3) The integrated resonance tank and integrated RF filtering provide this transmit noise and spurious levels in cellular bands.

(4) At max output power

(5) This is at the chip output.

(6) The Host needs to set the correct gain level. For input levels other than those specified in this table and still above 58 mVp, the SNR can be up to 4 dB lower.

(7) Mono, Δf_{audio} = 22.5 kHz, fmod = 1 kHz, unless otherwise stated

(8) Stereo, Δf_{audio} = 22.5 kHz, fmod = 1 kHz, Δf_{Pilot} = 6.75 kHz, L = R, no RDS, unless otherwise stated

4.5 FM interfaces

4.5.1 Control interface

The FM subsystem can either be controlled via the I2C interface, or via the Bluetooth HCI interface. In the latter case vendor-specific HCI commands and events are used.

FM I2C interface

The FM I2C interface offers one way to control the FM subsystem of the chip. Based on the standard I2C protocol, commands can be sent over this interface to boot and control the FM subsystem, and to retrieve settings. A dedicated interrupt pin can be used to notify the host.

A host-level API has been defined along with the underlying host-level C functions. This allows the host to address the FM subsystem in a user-friendly and straightforward way and allows for a fast integration at host level. See also *Section 5.1.1: "FM external control"*. The command encoding is exactly the same when using FM I2C or BT HCI such that the host driver can be the same for both.

The physical aspects of the FM I2C interface are described in *Section 3.12.4: "FM I2C interface"*.

Bluetooth HCI interface

Alternatively the FM subsystem can be controlled from the Bluetooth chip using the Bluetooth HCI interface. For this purpose a set of vendor-proprietary HCI commands has been defined. This set allows the host to control the FM subsystem and to retrieve information on the control settings. To notify the host a vendor-specific HCI event is used.

The command encoding is exactly the same when using I2C or BT HCI such that the host driver can be the same for both.

4.5.2 Audio interface

The FM receiver output can be routed to an I2S output interface, to a PCM output interface, to a stereo analog output interface or to an on-chip interface to the Bluetooth subsystem.

Similarly the FM transmitter can be configured to receive its input from an I2S input interface, from a PCM input interface, from a stereo analog input interface or from an on-chip interface linked to the Bluetooth subsystem.

Dedicated PCM and I2S interfaces

The PCM and I2S interfaces can be configured as Master or as Slave.

When acting as a Master, the I2S interface can be configured to any arbitrary sample rate between 8 and 192 kHz. The PCM interface can be configured to sample rates between 8 and 48 kHz.

The physical aspects of the PCM and I2S interfaces are described in *Section 3.12.7: "FM PCM interface"* and *Section 3.12.8: "FM I2S interface"*.

Routing to/from Bluetooth

For specific user applications the Bluetooth voice or audio air traffic can directly be taken from or routed to the FM subsystem (for receiver or transmitter, respectively). Another possibility is to route the received FM signal directly to the Bluetooth PCM/I2S port, or to route the Bluetooth PCM/I2S port directly to the FM transmitter. See *Section 3.10: "Multimedia features"* to have an overview of all use cases.

Control of this kind of routing is only possible via dedicated HCI commands.

Stereo analog audio codec output and input

Analog audio input and output requires external AC coupling components.

5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

5.1 WLCSP package information

The device STLC2690 is in lead-free/RoHs-compliant WLCSP package, 61 pins.

Figure 23 provides the package drawing and dimensions. See *Table 34: "Package dimensions"* for more detailed information.

Figure 23: WLCSP 3.315x3.56x0.6 61 F8 (B6 C6 G7 OUT) pitch 0.4 B 0.25

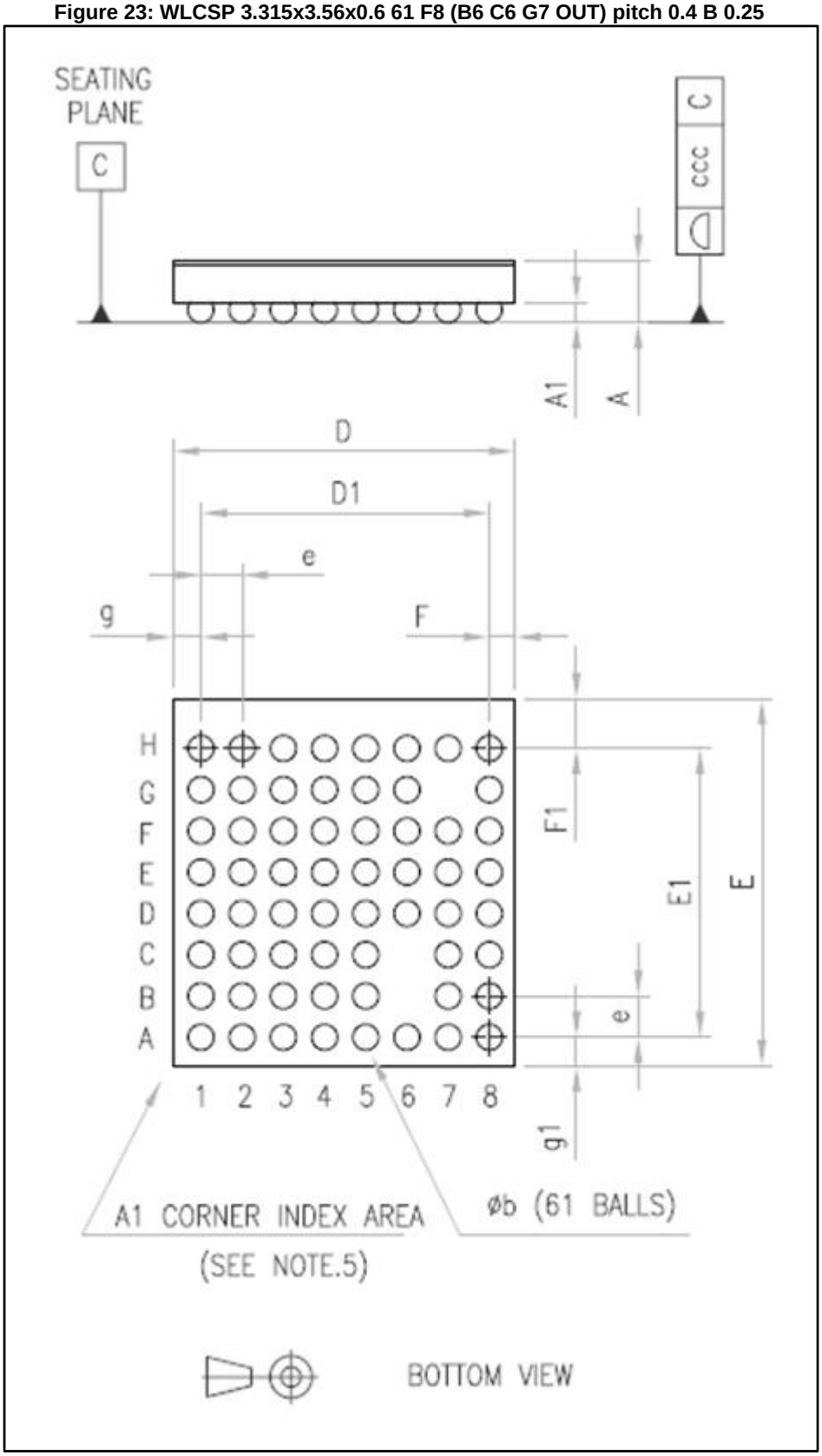


Table 34: Package dimensions

Dimensions (mm)				
Reference	**Min.**	**Typ.**	**Max.**	**Notes**
A			0.60	
A1		0.20		
b	0.24	0.27	0.30	*(2)*
D	3.275	3.315	3.355	
D1		2.80		
E	3.52	3.56	3.60	
E1		2.80		
e		0.40		
F		0.245		*(3)*
F1		0.48		*(3)*
g		0.27		*(3)*
g1		0.28		*(3)*
ccc			0.05	

1. WLCSP stands for Wafer Level Chip Scale Package.
2. The typical ball diameter before mounting is 0.25 mm.
3. The matrix ball array is not centered
4. The matrix ball array is depopulated (Balls B6 C6 G7 out)
5. The terminal A1 corner must be identified on the top surface by using a laser marking dot.

Figure 24: Package markings

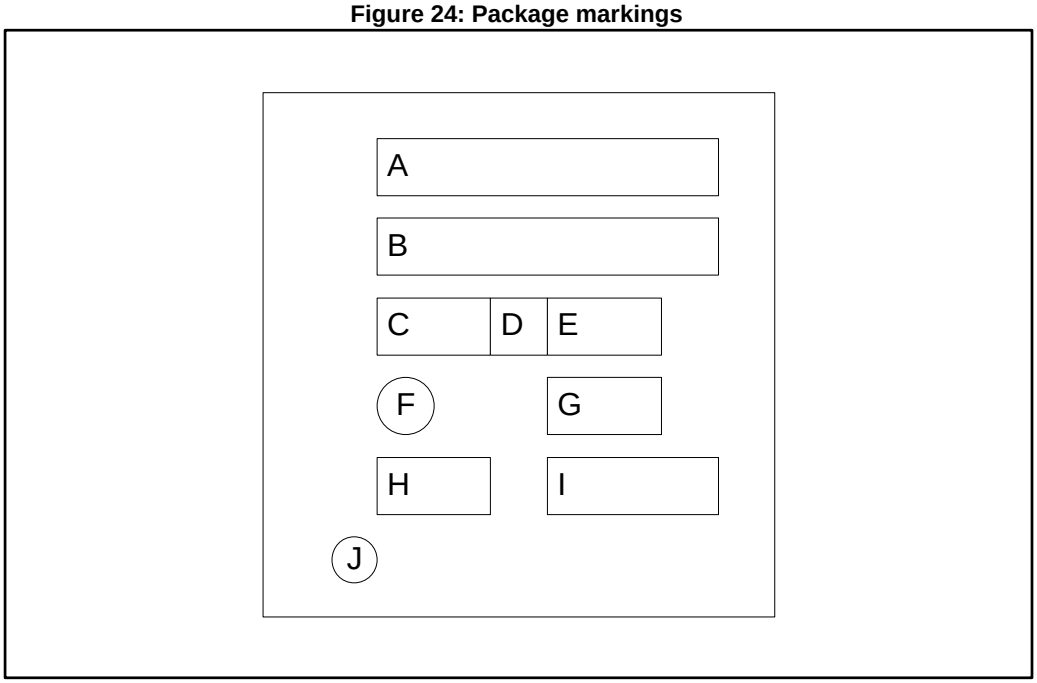


Table 35: Package markings: legend

Item	Description	Format	Value
A	Marking area	XXXXXX	2690W5
B	Operator input (diff lot)		
C	Assembly plant	PP	
D	Assembly year	Y	
E	Assembly week	WW	
F	Second lvl_intct		
G	Marking area (wafer number)		
H	Diffusion traceability plant	WX	
I	Country of origin	Max 3 char	
J	Dot (indicates pin A1)		

6 References

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8. RadioText Plus (RT+) Specification, Version 2.1, July 2006, RDS Forum
9. The I2C-bus specification, Version 2.1, January 2000, Philips Semiconductors
10. The I2S-bus specification, June 1996, Philips Semiconductors
11. AN_43_STLC2690_Layout_guideline.pdf, STE
12. AN_54_STLC2690_BT_Front_End_Recommendations.pdf, STE
13. BMDS_STLC2690_HW_Manual_FM.pdf, STE
14. AN_31_STLC2690_Enhanced_SPI_Mode.pdf, STE
15. AN_35_STLC2690_UART_Mode.pdf, STE
16. STLC2690_SW_Manual.pdf, STE
17. AN_29_STLC2690_Pin_Mapping.pdf, STE

7 Acronyms and abbreviations

Table 36: Acronyms and abbreviations

Acronym/abbreviation descriptions	
2-DH1	Bluetooth 2 Mbps ACL packet type
2-DH3	Bluetooth 2 Mbps ACL packet type
2-DH5	Bluetooth 2 Mbps ACL packet type
2-EV3	Bluetooth 2 Mbps synchronous packet type
2-EV5	Bluetooth 2 Mbps synchronous packet type
3-DH1	Bluetooth 3 Mbps ACL packet type
3-DH3	Bluetooth 3 Mbps ACL packet type
3-DH5	Bluetooth 3 Mbps ACL packet type
3-EV3	Bluetooth 3 Mbps synchronous packet type
3-EV5	Bluetooth 3 Mbps synchronous packet type
8-DPSK	8 phase differential phase shift keying
A2DP	Advanced audio distribution profile
AC	Alternating current
ACL	Asynchronous connection oriented
ADC	Analog to digital converter
AF	Alternate frequency
AHB	Advanced high-performance bus
A-law	Audio encoding standard
AMR	Absolute maximum rating
APB	Advanced peripheral bus
API	Application program interface
ARM7	Micro-processor
ARM7TDMI	Micro-processor
AWMA	Alternating wireless medium access
B-BPF	Balanced band pass filter
BER	Bit error rate
BOM	Bill of materials
BR	Basic rate
BT	Bluetooth
BW	Band width
C/I	Carrier-to-co-channel interference
CODEC	COder DECoder
CPU	Central processing unit
CQDDR	Channel quality driven data rate change

Acronym/abbreviation descriptions	
CVSD	Continuous variable slope delta modulation
DC	Direct current
DEVM	Differential error vector amplitude
DH1	Bluetooth 1 Mbps ACL packet type
DH3	Bluetooth 1 Mbps ACL packet type
DH5	Bluetooth 1 Mbps ACL packet type
DM1	Bluetooth 1 Mbps ACL packet type
DM3	Bluetooth 1 Mbps ACL packet type
DM5	Bluetooth 1 Mbps ACL packet type
DMA	Direct memory access
DSP	Digital signal processor
DUN	Dial-up networking profile
DV	Bluetooth 1 Mbps synchronous packet type
ED	Erroneous data delivery
EDR	Enhanced data rate
EIR	Extended inquiry response
EPR	Encryption pause/resume
eSCO	extended SCO
EV3	Bluetooth 1 Mbps synchronous packet type
EV4	Bluetooth 1 Mbps synchronous packet type
EV5	Bluetooth 1 Mbps synchronous packet type
FHS	Frequency hopping synchronization
FIFO	First in, first out
FLL	Frequency locked loop
FM	Frequency modulation
GFSK	Gaussian frequency shift keying
GPIO	General purpose I/O pin
GSM	Global system for mobile communications
H4	UART based HCI transport
HCI	Host controller interface
HV1	Bluetooth 1 Mbps synchronous packet type
HV3	Bluetooth 1 Mbps synchronous packet type
HW	Hardware
I/O	Input/output
I2C	Inter-integrated circuit
I2S	Inter-integrated circuit sound
IF	Intermediate frequency

Acronym/abbreviation descriptions	
ISM	Industrial, scientific and medical
JTAG	Joint test action group
L2CAP	Logical link control and adaptation protocol
LMP	Link manager protocol
LNA	Low noise amplifier
LO	Local oscillator
LSTO	Link supervision time out
MPX	MultiPleX
PA	Power amplifier
PBF	Packet boundary flag
PCB	Printed circuit board
PCM	Pulse code modulation
PD	Pull-down
PDA	Personal digital assistant
PLL	Phase locked loop
PPEC	Pitch-period error concealment
PTA	Packet traffic arbitration
PU	Pull-up
QoS	Quality of service
RAM	Random access memory
RBDS	Radio broadcast data system
RC	Resistance-capacitance
RDS	Radio data system
RF	Radio frequency
rms	Root mean squared
ROM	Read only memory
RSSI	Receive signal strength indication
RX	Receive
SBC	Sub band coding
SCO	Synchronous connection oriented
SIG	Bluetooth special interest group
SPI	Serial peripheral interface
SSP	Secure simple pairing
SSR	Sniff subrating
ST	STMicroelectronics
SW	Software
T_{eSCO}	eSCO interval

Acronym/abbreviation descriptions	
T_{SCO}	SCO interval
T_{sniff}	Sniff interval
TX	Transmit
UART	Universal asynchronous receiver/transmitter
VCO	Voltage controlled oscillator
VGA	Variable gain amplifier
WCDMA	Wideband code division multiple access
WFBGA	Very very thin profile fine pitch ball grid array
WLAN	Wireless local area network
WLCSP	Wafer-level chip scale package
µ-law	Audio encoding standard
π/4-DQPSK	π/4 rotated differential quaternary phase shift keying

8 Revision history

Table 37: Document revision history

Date	Revision	Changes
13-Nov-2014	3	Datasheet reformatted to STMicroelectronics standards following the transfer of the product from STEricsson. No technical changes.

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