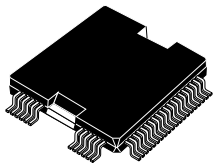
# STLC5445

## QUAD LINE FEED CONTROLLER

- BATTERY VOLTAGE UP TO 120V
- SUPPLIES POWER FOR UP TO FOUR DIGITAL TELEPHONE LINES
- PROGRAMMABLE CURRENT LIMITING
- LONGITUDINAL CURRENT CANCELLATION
- ETSI ETR80 COMPLIANT
- OUTPUT CURRENT UP TO 140 mA
- STATUS CONDITION DETECTION FOR EACH LINE
- AUTOMATIC THERMAL PROTECTION
- AUTO POWER ON SEQUENCE
- OUTPUT STAGE OPTIMIZED FOR MINIMAL OUTPUT OVERVOLTAGE PROTECTION
- TWO EXTERNAL RELAY DRIVERS PER LINE
- PARALLEL OR MPI CONTROL INTERFACE
- HI-QUAD PACKAGE 64 PIN



**HiQUAD-64**

**ORDERING NUMBER: STLC5445**

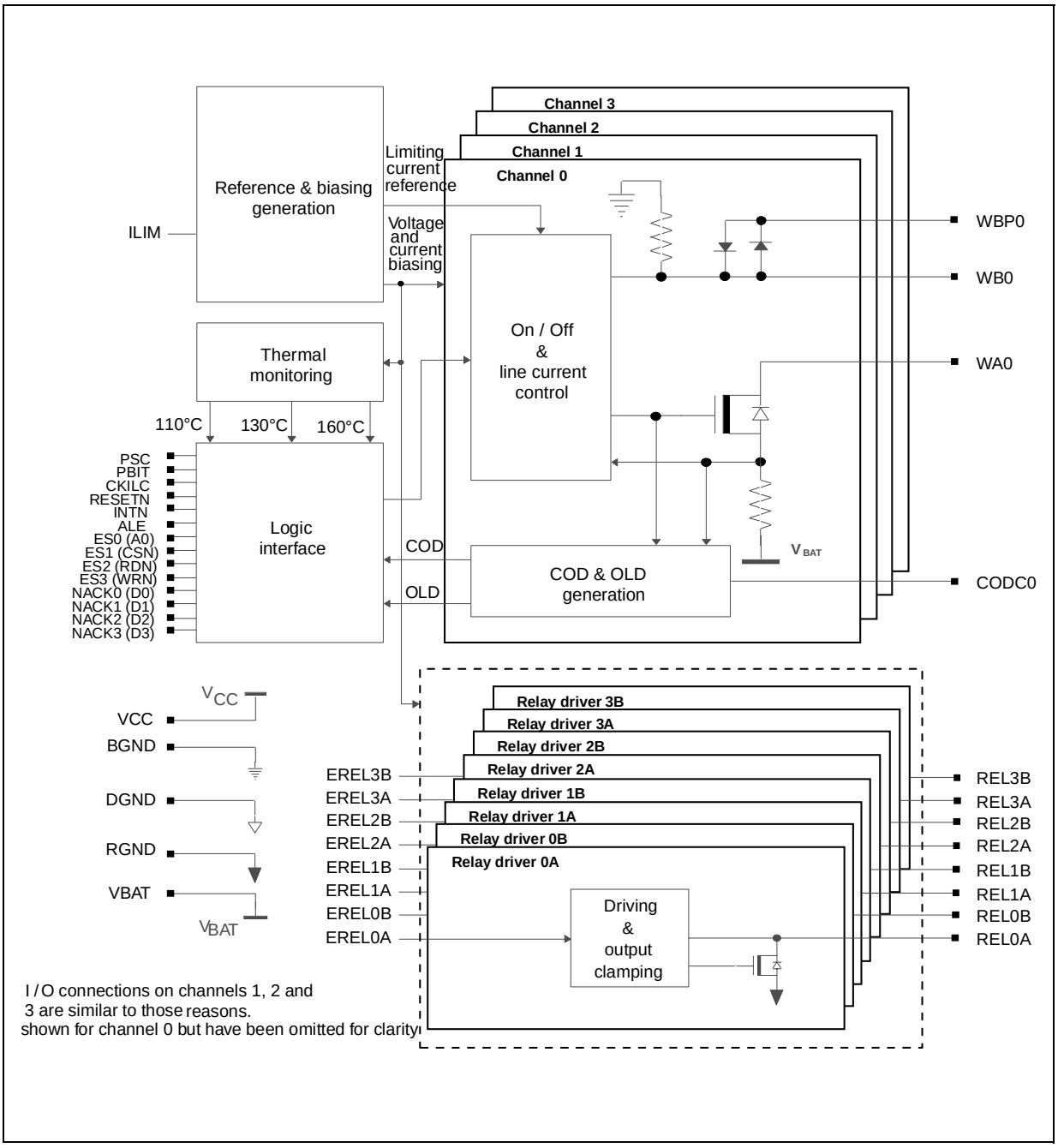
### DESCRIPTION

The QUAD LINE FEED CONTROLLER provides a power source for up to four U line interfaces. The power source to the device is a local battery or a centralized regulated power supply. Each powered line is individually controlled and monitored by the device interface.

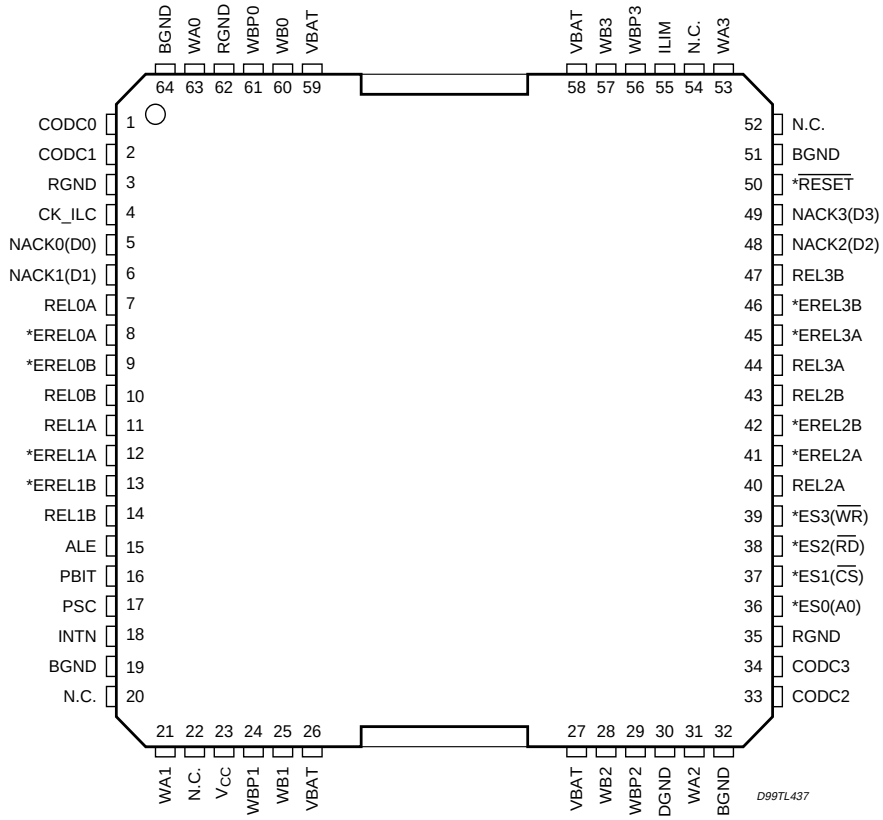
A MPI or a simple parallel interface can be selected by a pin strap.

Each line can be individually powered and monitored: therefore overload and faults can easily be detected and localized even in a large system. The status conditions detected by the device are: Current Overload, Thermal Overload, Open Loop. If activated (by means of a dedicated pin strap), a self generated power on sequence avoids the thermal over stress when a simultaneous power on has been requested for more than one channel. The current limiting value can globally be programmed for the four channels by means of an external resistor. The device has two integrated relay drivers per line to drive the test relays of the ISDN system.

## BLOCK DIAGRAM



**PIN CONNECTION** (Top view)




*INTERNAL PULL DOWN TO GROUND

**PIN FUNCTION**

| N° | Pin Name | Description |
|---|---|---|
| 1 | CODC0 | Pin for connection of the external capacitor (100nF/6.3V) to GND for COD signal filtering on channel 0. |
| 2 | CODC1 | Pin for connection of the external capacitor (100nF/6.3V) to GND for COD signal filtering on channel 1 |
| 4 | CKILC | External clock input pin for the internal power on sequencer |
| 5 | NACK0(D0) | Logic pin: with PSC = 0, Line 0 status information output<br>with PSC = 1, Line 0 I/O tristate data bus |
| 6 | NACK1(D1) | Logic pin: with PSC = 0, Line 1 status information output<br>with PSC = 1, Line 1 I/O tristate data bus |
| 7 | REL0A | Output of the 0A relay driver |
| 8 | *EREL0A | Logic input pin: relay 0A output driver's ON/OFF (high = ON) |
| 9 | *EREL0B | Logic input pin: relay 0B output driver's ON/OFF (high = ON) |
| 10 | REL0B | Output of the 0B relay driver |
| 11 | REL1A | Output of the 1A relay driver |

**PIN FUNCTION** (continued)

| N° | Pin Name | Description |
|---|---|---|
| 12 | *EREL1A | Logic input pin: relay 1A output driver's ON/OFF (high = ON) |
| 13 | *EREL1B | Logic input pin: relay 1B output driver's ON/OFF (high = ON) |
| 14 | REL1B | Output of the 1B relay driver |
| 15 | ALE | Logic input pin: with PSC = 0, Don't care<br>with PSC = 1, Address Latch Enable (active high) |
| 16 | PBIT | Power on sequencer enable: PBIT = 0: power on sequencer ON<br>PBIT = 1: power on sequencer OFF |
| 17 | PSC | Parallel or MPI mode input selection pin:<br>0 = parallel interface; 1 = MPI interface |
| 18 | INTN | Logic output pin; open drain: with PSC = 0 high impedance<br>with PSC = 1 interrupt (active low) |
| 21 | WA1 | Output feeder's switch side of line 1; negative respect to WB1 |
| 23 | VCC | Positive supply voltage. It is referred to DGND |
| 24 | WBP1 | Internal protection diodes for line 1 |
| 25 | WB1 | Output feeder's resistive side of line 1; positive respect to WA1 |
| 28 | WB2 | Output feeder's resistive side of line 2; positive respect to WA2 |
| 29 | WBP2 | Internal protection diodes for line 2 |
| 30 | DGND | Digital ground |
| 31 | WA2 | Output feeder's switch side of line 2; negative respect to WB2 |
| 33 | CODC2 | Pin for connection of the external capacitor (100nF/6.3V) to GND for COD signal filtering on channel 2 |
| 34 | CODC3 | Pin for connection of the external capacitor (100nF/6.3V) to GND for COD signal filtering on channel 3 |
| 36 | *ES0(A0) | Logic input pin: with PSC = 0, Line 0 ON/OFF request (high=ON)<br>with PSC = 1, Address bit for R/W operations |
| 37 | *ES1(CSN) | Logic input pin: with PSC = 0, Line 1 ON/OFF request (high=ON)<br>with PSC = 1, chip select (active low) |
| 38 | *ES2(RDN) | Logic input pin: with PSC = 0, Line 2 ON/OFF request (high=ON)<br>with PSC = 1, Read command (active low) |
| 39 | *ES3(WRN) | Logic input pin: with PSC = 0, Line 3 ON/OFF request (high=ON)<br>with PSC = 1, Write command (active low) |
| 40 | REL2A | Output of the 2A relay driver |
| 41 | *EREL2A | Logic input pin: relay 2A output driver's ON/OFF (high = ON) |
| 42 | *ERL2B | Logic input pin: relay 2B output driver's ON/OFF (high = ON) |
| 43 | REL2B | Output of the 2B relay driver |
| 44 | REL3A | Output of the 3A relay driver |

**PIN FUNCTION** (continued)

| N° | Pin Name | Description |
|---|---|---|
| 45 | *EREL3A | Logic input pin: relay 3A output driver's ON/OFF (high = ON) |
| 46 | *ERL3B | Logic input pin: relay 3B output driver's ON/OFF (high = ON) |
| 47 | REL3B | Output of the 3B relay driver |
| 48 | NACK2 (D2) | Logic pin: with PSC = 0, Line 2 status information output<br>with PSC = 1, Line 2 I/O tristate data bus |
| 49 | NACK3 (D3) | Logic pin: with PSC = 0 line 3 status information output<br>with PSC = 1 line 3 I/O tristate data bus |
| 50 | *RESETN | Logic input pin: reset (active low) |
| 53 | WA3 | Output feeder's switch side of line 3; negative respect toWB3 |
| 55 | ILIM | Current limit programming input |
| 56 | WBP3 | Internal protection diodes for line 3 |
| 57 | WB3 | Output feeder's resistive side of line 3; positive respect to WA3 |
| 60 | WB0 | Output feeder's resistive side of line 0; positive respect to WA0 |
| 61 | WBP0 | Internal protection diodes for line 0 |
| 0 | WA0 | Output feeder's switch side of line 0; negative respect to WB0 |
| 26<br>27<br>58<br>59 | VBAT | Negative battery supply voltage. It is referred to BGND |
| 19<br>32<br>51<br>64 | BGND | Battery ground |
| 3<br>35<br>62 | RGND | Relay ground |

* Internal pull down to ground

## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | Voltage from digital input to DGND | – 0.5 to VCC + 0.5 | V |
| $V_{CD}$ | Voltage from VCC to DGND | – 0.4 to +7 | V |
| $V_{BB}$ | Voltage from VBAT to BGND | – 143 to + 0.4 | V |
| $V_{BD}$ | Voltage from BGND to DGND | – 3 to +0.5 | V |
| $I_{WBn}$ | AC Current into the WBn outputs (WBPn not connected to GND | 250 | mA peak |
| $I_{NEG}$ | Negative current injected in the WAn outputs (-40 to +85°C) | 50 | mA |
| $T_{stg}$ | Storage temperature | – 60 to 150 | °C |

## RECOMMENDED OPERATING CONDITION

| Symbol | Parameter | Test Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | $V_{CC}$ supply voltage | | 4.75 | | 5.25 | V |
| $V_{BAT}$ | $V_{BAT}$ supply voltage | | – 120 | | – 38 | V |
| $V_{BGND}$ | BGND/DGND voltage | | – 3 | | 0.5 | V |
| $I_{LIMT}$ (1) | Programmable range of the current limiting function | | 20 | | 140 | mA |
| $I_{Relay}$ | Relay driver current | | | | 70 | mA |
| $T_{a\ normal}$ | Ambient temperature normal range | | 0 | | 70 | °C |
| $T_{a\ extended}$ | Ambient temperature extended range | | – 40 | | 85 | °C |
| $I_{loop}$ | Max operating loop current | | | | 140 | mA |
| $R_{MIN}$ | External, short circuit resistive load from WAn to WBn | | 55 | | | W |

## ELECTRICAL CHARACTERISTCS

Unless otherwise specified the below listed parameters' values are referred to the following conditions: $V_{BAT}$ = –115V, $V_{CC}$ = 5V, $R_{lim}$ = 53.6 kW, CODCn RC series = 100nF ±10% and 510Ω ±1%, normal temperature range [0°C to 70°C]. The presence of an asterisk mark (*) indicates that the marked parameter must remain within the specified tolerance in the extended temperature range [-40°C to 85°C].

| Symbol | Parameter | Test Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{Vcc}$ | $V_{CC}$ supply current | All the switches on No load | | | 2.5 | mA |
| $I_{VBAT}$ | $V_{BAT}$ supply current | All the switches on No load | | 1.5 | 1.8 | mA |
| $I_{LIMT}$ | Current limiting value with transversal line current only | $I_{long}$ = 0 | 42.5 | 50 | 57.5 | mA |
| $I_{LIMTL}$ | Current limiting value with added longitudinal line current | See Fig.1 | 37.5 | 50 | 62.5 | mA |
| $I_{LIM\%}$ | Current limiting accuracy in the range 20 to 140 mA(1) | $I_{long}$ = 0 | ±15 | | | % |
| $I_{HZ}$ | Leakage current of each WAn output to ground with output driver disabled | | | | 50* | µA |
| $R_{WA}$ | Resistance from WAn to $V_{BAT}$ | $I_{WA}$ = 30mA | 3.15 | 5.5 | 7.85 | Ω |
| $R_{WB}$ | Resistance from WBn to BGND | $I_{WB}$ = 30mA | 3.5 | 5.5 | 7.5 | Ω |
| $\Delta R_{OUT}$ | Absolute value of the difference between $R_{WAn}$ and its related $R_{WBn}$ | $I_{WA}$ = $I_{WB}$ = =30mA | | | 0.7<br>1(*) | Ω |
| $T_{j110}$ | 110°C thermal monitoring threshold | | | 110 | | °C |
| $T_{j130}$ | 130°C thermal monitoring threshold | | | 130 | | °C |
| $T_{j160}$ | 160°C thermal monitoring threshold | | | 160 | | °C |
| $T_{hyst}$ | Thermal monitoring hysteresis | | | 10 | | °C |
| $LV_{out}$(2) | Longitudinal output component of the fCKILC clock signal | See Fig. 2 | | | – 60 | dBV |
| $V_{Rel33}$ | Relay drivers' output voltage | All the relay drivers activated at a load current of 33mA.(3) | | | 0.5 | V |
| $V_{Rel70}$ | Relay drivers output voltage | All the relay drivers activated at a load current of 70mA.(3) | | | 1.2 | V |
| $I_{Rleak}$ | Relay driver leakage current | ERLn = Low | | | 100 | µA |

**ELECTRICAL CHARACTERISTICS** (continued)

| Symbol | Parameter | Test Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{SOC}$ | Open circuit detector threshold | | 1.5 | 3 | 4 | mA |
| OLDH | Open Loop detector Hysteresis | | | 0.6 | 1.6 | mA |

Notes: 1. Our characterizations show that in the range 15mA - 20mA the accuracy is ±20% over the 0°C - 70°C temperature range.
2. The longitudinal component of the signal detected by the spectrum analyzer must have an RMS voltage value, in any 4kHz equivalent bandwidth, averaged in any 1 second period, not greater of the specified value (–60dBV) over the 100Hz - 150kHz range (for details see ETSI ETR80 and ANSI 601).
3. All the output lines activated at a line current of 35mA; no current limitation condition. Rth(j-a) ≤ 20°C/W

*Please note that, in order to assure the frequency stability of the output drivers, a 1µF capacitor must always be connected between WAn and Wbn or, as shown in Fig. 6, immediately after the resistive protection elements used in the actual application.*

The $R_{LIM}$ value can be calculated starting from the value of the needed current limitation threshold $I_{LIMT}$:

$$R_{LIM} = \frac{2664}{I_{LIMIT}}$$

**SWITCHING TIMING**

| Symbol | Parameter | Test Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{ENP}$ | Output driver's enable time | Parallel interface mode | | 20 | | µs |
| $t_{DISP}$ | Output driver's disable time | Parallel interface mode | | 500 | | µs |
| $f_{CKILC}$ | Frequency of CKILC | Duty cycle 60% max<br>Pulse width 500ns min | | 8 | 200 | kHz |

**Figure 1.**

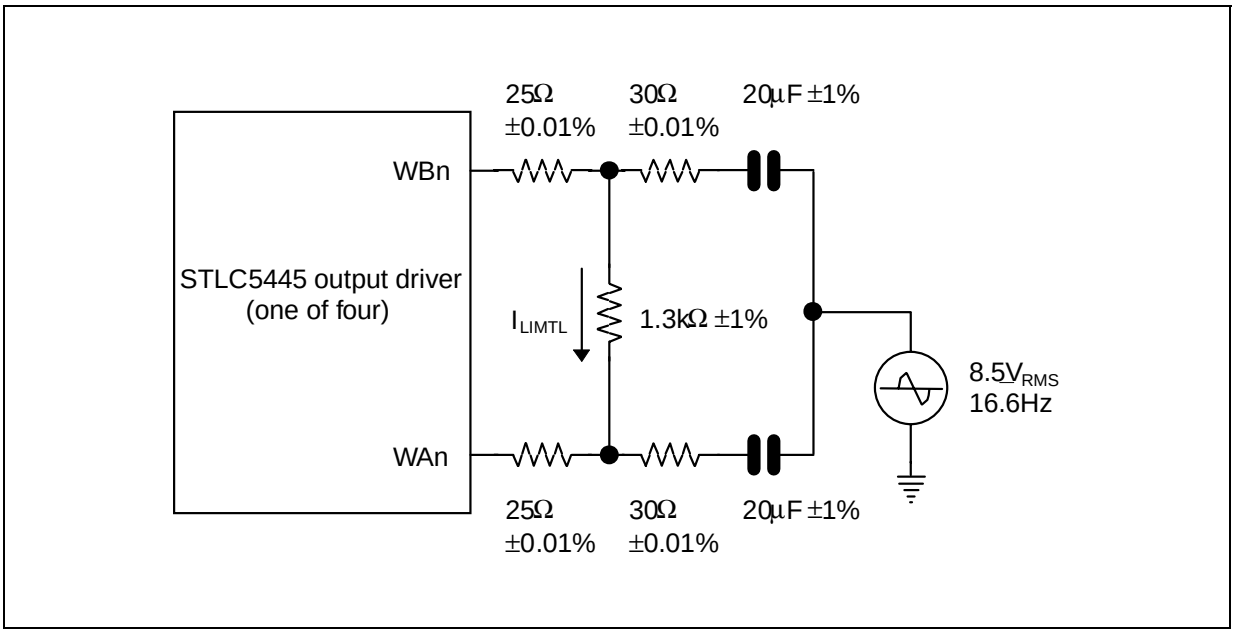
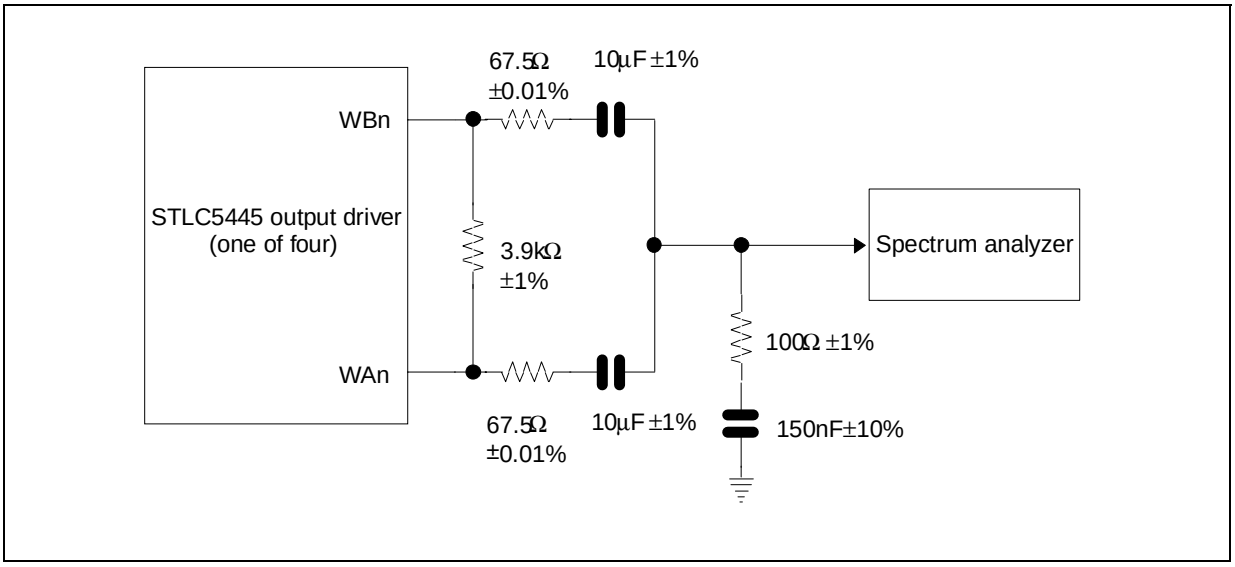


**Figure 2.**




## STATIC CHARACTERISTICS

Unless otherwise specified the below listed parameters values are referred to the following conditions: $V_{CC}$ = 5V, normal temperature range.

| Symbol | Parameter | Test Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Input low voltage | | | | 0.8 | V |
| $V_{IH}$ | Input high voltage | | 2 | | | V |
| $V_{OL}$ | Output low voltage | $I_o$ = 1mA | | | 0.4 | V |
| $V_{OH}$ | Output high voltage (Open drain with PSC = 0) | $I_o$ = –1 mA | 2.4 | | | V |
| $I_{LH}$ | Input high current | | 0 | | 10 | µA |
| $I_{LL}$ | Input low current | | -10 | | 0 | µA |
| $I_{OZ}$ | Output current in High impedance state | | -10 | | 10 | µA |

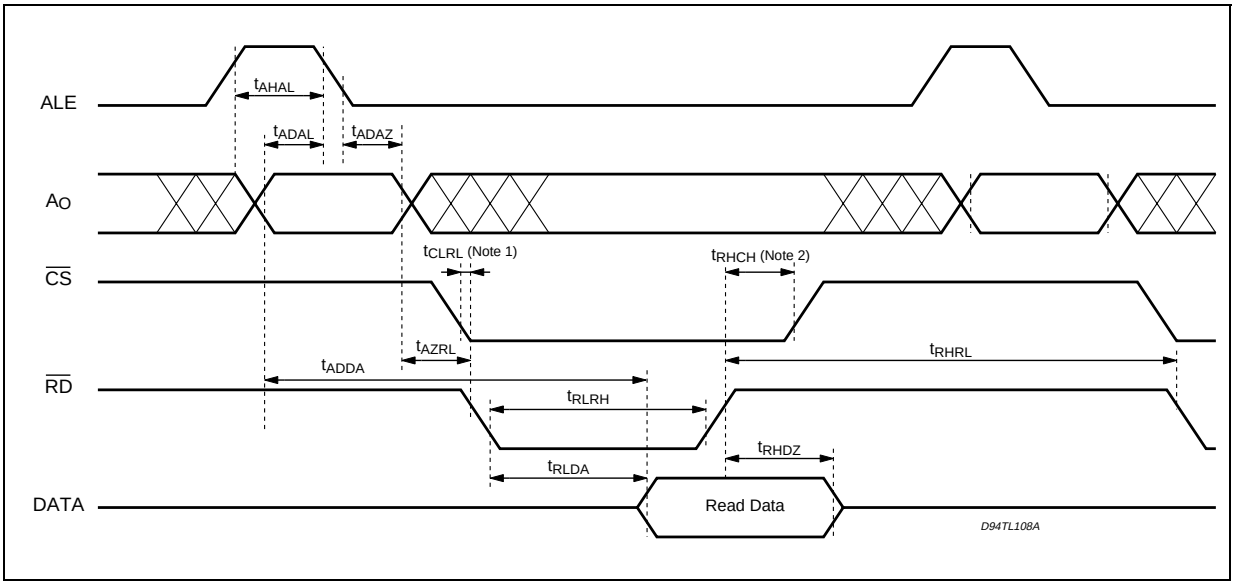
## SWITCHING CHARACTERISTICS

**MICROPROCESSOR WRITE / READ TIMING** (refers to figures 3 and 4).

Unless otherwise specified the below listed parameters' values are referred to the following conditions: VCC=5V, normal temperature range.

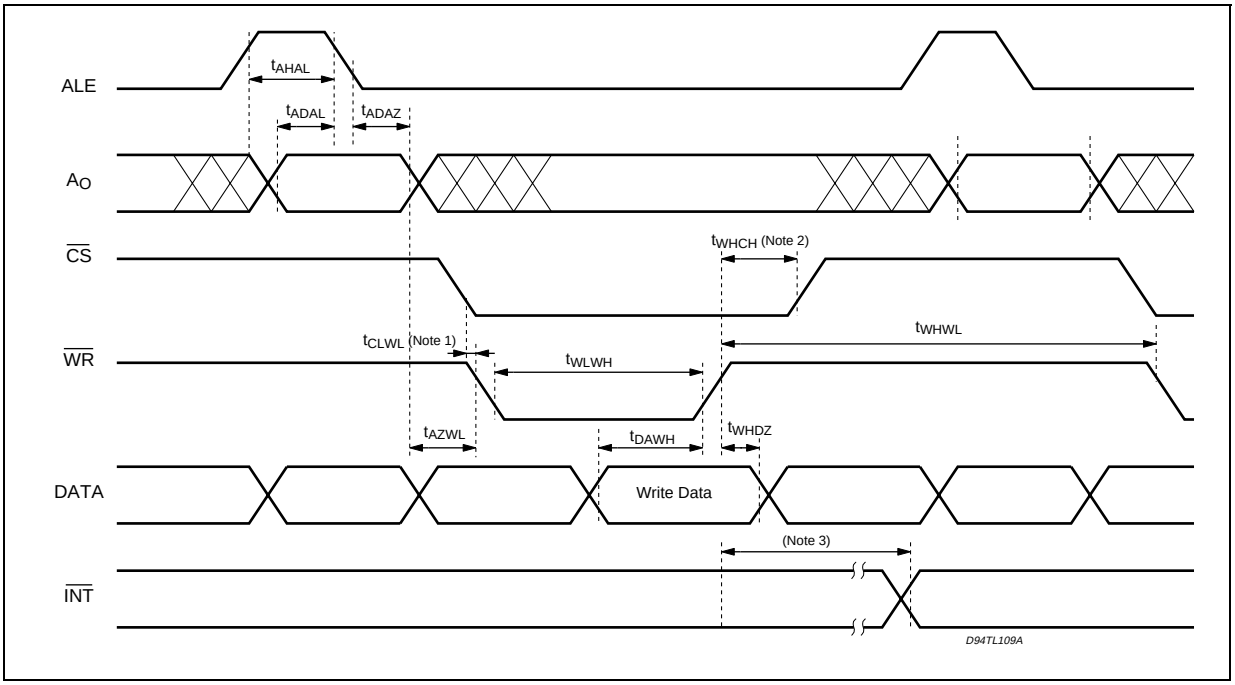
| Symbol | Parameter | Test Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{RLRH}$ | RDN, CSN pulse width | | 260 | | | ns |
| $t_{RHRL}$ | RDN, recovery time | $T_{amb}$ = – 40 to 0°C and +70°C to +85°C | 200<br>220 | | | ns |
| $t_{RLDA}$ | RDN, CSN low to data available | | | | 260 | ns |
| $t_{RHDZ}$ | RDN or CSN high to data Z | $T_{amb}$ = – 40 to 0°C and +70°C to +85°C | | | 130<br>160 | ns |
| $t_{AHAL}$ | ALE pulse width | | 100 | | | ns |
| $t_{ADAL}$ | Address setup time | | 60 | | | ns |
| $t_{ADAZ}$ | Address hold time | | 50 | | | ns |
| $t_{AZRL}$ | Address Z to RDN low | | 0 | | | ns |
| $t_{AZWL}$ | Address Z to WRN Low | | 0 | | | ns |
| $t_{ADDA}$ | Address stable to data available | $T_{amb}$ = – 40 to 0°C and +70°C to +85°C | 360<br>390 | | | ns |
| $t_{WLWH}$ | WRN or CSN pulse width | | 200 | | | ns |
| $t_{WHWL}$ | Write recovery time | | 200 | | | ns |
| $t_{DAWH}$ | Data setup time | | 100 | | | ns |
| $t_{WHDZ}$ | Data hold time | $T_{amb}$ = – 40 to 0°C and +70°C to +85°C | 20<br>40 | | | ns |
| $t_{RESN}$ | Reset Pulse with | | 200 | | | ns |

### Figure 3. Microprocessor WRITE timing



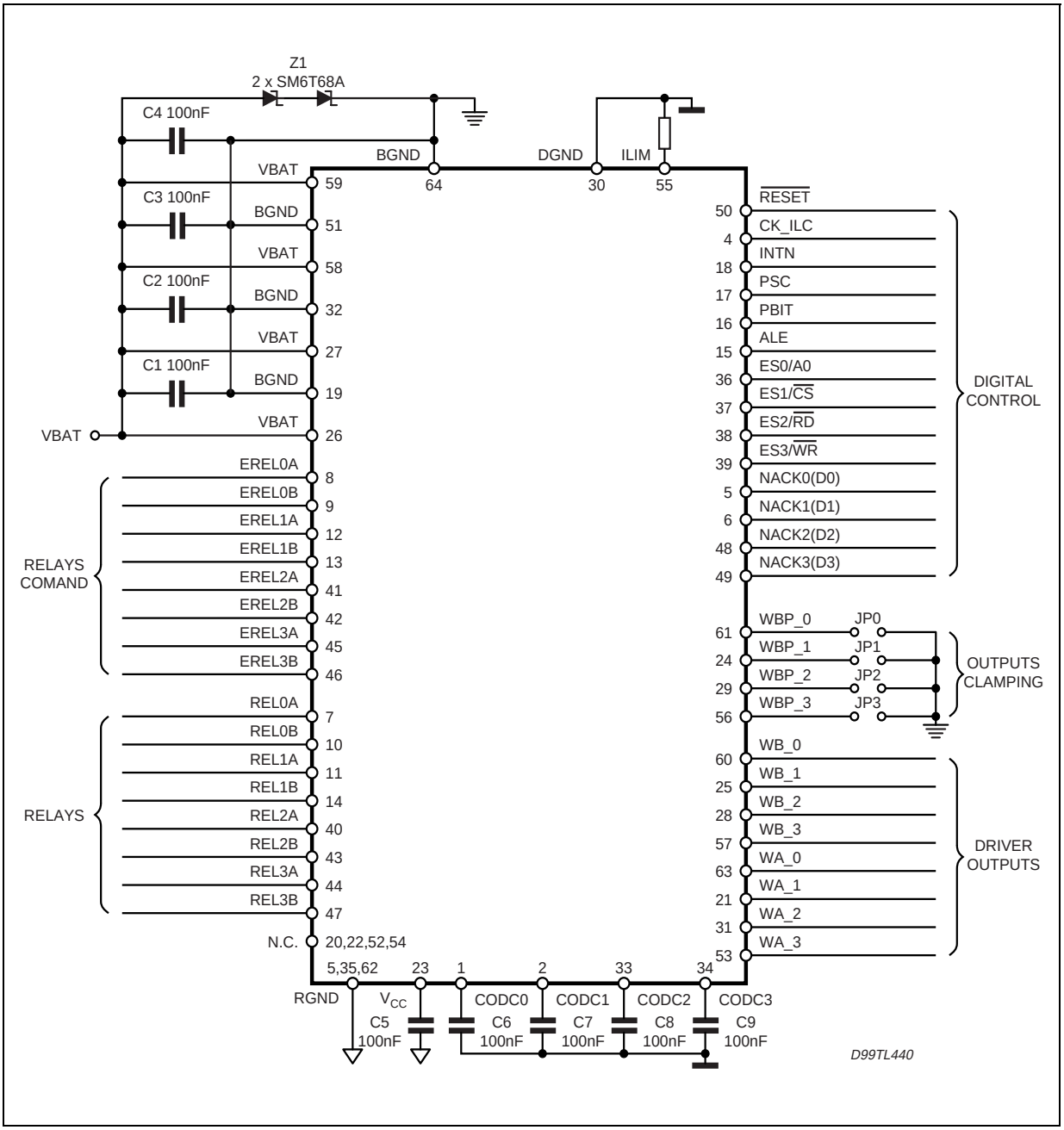

Notes: 1. If tCLWL is negative tWLWH is measured from CS_ rather than fromWR_.
2. If tWHCH is negative, tWHWL, tWLWH, tDAWH and tWHDZ are measured from CS_ rather than fromWR_.
The propagation delay from the writing of the T/I bit to the effect on the INT pin is approximately 1ms for both mask and enable operations.

### Figure 4. Microprocessor READ timing




Notes: 1. If tCLRL is negative, tRHRL, tRLRH, tAZRL, and tRLDA are measured from CS_ rather than RD_.
2. If tRHCH is negative, tRHRL, tRLRH and tRHDZ are measured from CS_ rather than RD_.
When a read from the LER immediately follows a write to the LER a minimum of 1ms is required between these operations

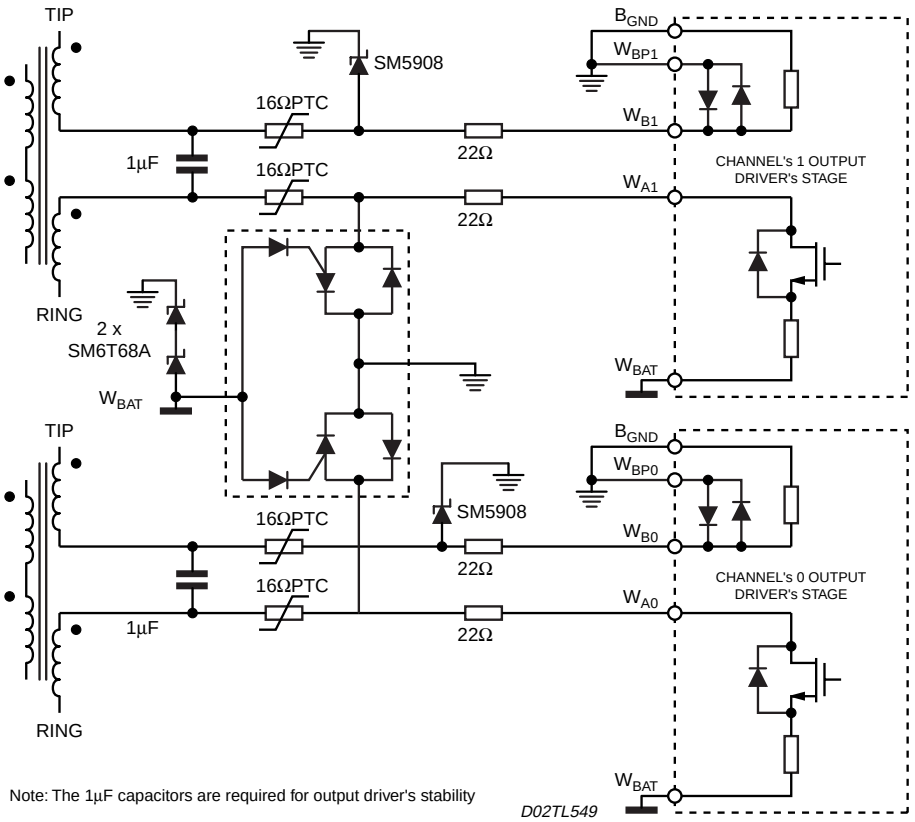
**Figure 5. Typical Application Circuit**




**External Component List**

| Coponents | Description | Value |
|---|---|---|
| C1, C2, C3, C4 & C5 | Power Supply Filter Capacitance | 100nF |
| C6, C7, C8 & C9 | Signal Filter Capacitance | 100nF |
| $R_{LIN}$ | Programmable Limiting Current Resistor | 53.6kΩ |
| $Z_1$ | Transil Clamping Protection | 136V |

**Figure 6. Typical Protection Diagram (only channel 0 and 1 shown)**




## FUNCTIONAL DESCRIPTION

**WAn** (n=0-3) Drivers (output pins).

Each WAn output can sink up to 140mA. When the ESn input is High and the activation request is approved by the internal control circuitry, the respective WAn output is internally connected to VBAT through a DMOS switch and the low side sensing resistor.

**WBn** (n=0-3) Resistor to BGND.

Each WBn output connects the wire B to ground through a 5W resistor used to perform the longitudinal balance and the high side current sensing function.

**WBPn** (n=0-3) Protection diodes connection (see the block diagram at page 3).

Each channel of the STLC5445 has two internal, back to back connected diodes, whose clamping action can be used to protect the WBn outputs during lighting and power crossing events. The diodes' clamping action is normally disabled and can be activated by connecting the WBPn pin to BGND. In this case however, if the line current exceeds 57.5mA the forward drop across the high side sensing resistor (and then across the diodes) reaches the diodes' conduction threshold, strongly degrading the current limiting action and the longitudinal balance. For line currents higher than 57.5mA external clamping elements must then be connected in place of the internal diodes or in series to them in order to increase the clamping voltage value.

**BGND** Battery ground.

**DGND** Digital ground.

**RGND** Ground connection of the relay drivers.

**CKILC** Logic input.

External clock input for the **Power On Sequencer** embedded in the **Logic interface** (see the block diagram at page 3). The Power On Sequencer controls (if activated) the power on sequence of the lines. This will limit the chip's temperature increase that occurs, at channels switch on, due to the charging current of the capacitances used by the external ISDN circuitry. If used, the Power on sequencer is the only block of the circuit that needs an external clock signal.

**ESn** (n=0-3) Logic inputs.

These pins have double names (see the block diagram at page 3) because they perform a double function: one in **Parallel mode** ( PSC = 0 ), and another in **MPI mode** ( PSC = 1).

In Parallel mode ESn acts as an activation or deactivation request for the respective line driver:

ESn = 0: Line driver deactivation request.

ESn = 1: Line driver activation request.

In MPI mode the pins perform the following functions:

**A0:** Selects the source and destination locations for read and write operations on the data bus. A0 must be valid on the falling edge of ALE or during RDN and WRN if ALE is tied High. Data transfer occurs over the D0-D3 lines.

**CSN:** This pin acts as a chip select. It must be Low to enable the read or write operations of the device.

**RDN:** Read command. The active Low read signal is conditioned by CSN and transfers internal information to the data bus. If A0 is a logical 0, the logic levels of the **I**ndirect **A**ddress **R**egister (**IAR**) and of the Thermal Shutdown Status bit will be transferred to D3-D0. If A0 is a logical 1, the data addressed by the **IAR** will be transferred to D3-D0.

**WRN:** Write command. The active Low write signal is conditioned by CSN and transfers information from the data bus to one of the two internal registers selectable by A0: if A0 is a logical 1, D3-D0 is written into the **L**ine **E**nable **R**egister (**LER**); if A0 is a logical 0, D2-D0 are written into the **I**ndirect **A**ddress **R**egister (**IAR**) and D3 is written as bit 3 and manages the generation of the interrupt signal for the external microprocessor. **LER** and **IAR** are the only two writable registers in the device.

**RESETN** Reset pin. It initializes the Power on sequencer, the TOR register and, in the MPI interface, the registers and the INTN (interrupt output pin). When applied it leaves all the line drivers switched off.

It has no effect in Parallel interface mode if the power on sequencer is not used.

When the supply voltages are applied to the circuit, an equivalent RESETN pulse (power on reset) is automatically, internally generated.

**ALE** **A**ddress **L**atch **E**nable. ALE is a logic input pin. It is used to strobe the address bit applied at the A0 pin, into the address latch. The address is latched on the High to Low transition of ALE. While ALE is High the address latch is transparent. For a non multiplexed microprocessor bus, ALE must be tied High.

**ILIM** The current limiting programming input, ILIM, is used to program the current limit of the four drivers by means of an external resistor connected between this pin and DGND. The voltage at ILIM pin is a replica of the internal bandgap voltage (1.236V).

When a line driver is in current limitation, its output current is 2155 times higher than the current flowing in the external current limiting programming resistor.

**INTN** The INTN (interrupt) open drain type output can only be used in MPI interface mode. INTN can be used to alerts an external microprocessor when a current overload condition occurs. It is not

latched and is active (Low level) when at least one of the CODn status detector bits is active (High level). When the four CODn status detector bits are Low, INTN goes inactive (High). INTN will also go inactive if (due to thermal overload) the QLFC automatically disables the output driver of the channel that caused the interrupt, or if the external microprocessor disables that line via the Line Enable Register (LER). The interrupt function can be disabled (INTN remains permanently High) via the Indirect Address Register (IAR) or a Low level on the RESETN pin.

**NACKn** (n=0-3) Logic I/O.

These pins have double names (see the block diagram at page 3) because they perform a double function: one in **Parallel mode** ( PSC = 0 ), and another in **MPI mode** ( PSC = 1).

In **Parallel mode** each NACKn acts as an open drain output and gives the channel's status information.

The NACKn bit goes in high impedance state (bit = 1 if a NACKn pull up is provided) when at least one of these conditions is verified:

The current on the relative line reaches the current limit programmed by the user.

The chip's temperature reach the thermal alarm threshold.

The line driver is in the Power on phase.

When the ESn input is set Low, the corresponding NACKn is set to zero.

In **MPI mode** the four pins become **D3 - D0** and act as a bidirectional data bus with three state capability. The four bidirectional data bus lines are used to exchange information with an external microprocessor. D0 is the least significant bit and D3 is the most significant bit. An High Level on the data bus corresponds to a logical 1. When the chip select bit (CSN) is Low, these lines act as inputs when WRN is Low and as outputs when RDN is Low. When CSN is High the D3 - D0 pins are in a high impedance state.

**PSC** Logic input.

This pin is used to select one of the two available logic interfaces.

PSC = 0: Parallel mode.

PSC = 1: MPI mode.

**ERLn** (n=0A-3B) Logic inputs.

Each ERLn pin controls directly the respective relay driver's DMOS:

ERLn = 0 : Switch off the relay driver.

ERLn = 1 : Switch on the relay driver.

**RLn** (n=0A-3B) Relay drivers' output.

Each of the eight RLn pins is connected to the drain of an internal DMOS switch (see the block diagram at page 3) which acts as a driver for an external relay to be supplied from VCC. The relay drivers' current flows to ground through the RGND pins. Each output can sink up to 70 mA. An internal clamping circuit is provided, so no external kickback diodes are required.

**CODCn**

(n=0-3) When a line over current condition exists, the output driver of the overloaded channel instantaneously limits the line current at the value programmed by means of the external RLIM resistor. In this condition the **C**urrent **O**verload **D**etector bit (COD) switches to a High logic level.

When operating in MPI mode this bit can, for each of the four channels, be red by the external microprocessor in order to check which channel (if any) is overloaded.

When in parallel mode each COD bit is internally OR combined with two other bits in order to generate the NACKn bit.

Since in the ISDN application it can happens that the sum of the DC line current and the superimposed signal peaks, easily exceeds the needed DC current limit, the COD generation circuitry has been arranged in such a way that the COD bit will be pushed High **only** if the current overload persists for at least 20ms: this eliminates any spurious High level COD / NACK. The men-

tioned delaying function requires, for each of the four channels, one Capacitor of 100nF has to be connected between each CODCn and ground.

## OPERATIVE DESCRIPTION

The device comprises three main blocks: the **Analog section** , the **Logic section** and the **Relay driver section**.

The Analog section feeds the four lines and detects their status.

The Logic section allows to exchange information and commands between the QLFC and the external digital system.

The Relay driver section is completely independent: each relay command input is related to its own driver without any conditioning.

**Analog Section** (see the Block diagram at page 3)

The ANALOG section comprises the **Channel 0-Channel 3** block, the **Reference & biasing generation** block and the **Thermal monitoring** block.

As shown in the channel's card of the block diagram, the WBn and WAn pins to which the line is connected are respectively routed to the battery ground and to the VBAT line: WBn goes to BGND through the upper side sensing resistor; WAn goes to VBAT through a power DMOS and the lower side sensing resistor. The ON/OFF control for the power DMOS comes from the outside world through the **Logic interface** block.

The implemented topology for the circuit used to cancel the longitudinal current effect is a DC coupled topology: it doesn't need external capacitors and its frequency band starts from DC.

The QLFC has a double protection provided by its **current limiting** and **thermal monitoring capabilities**.

The current limit threshold (ILIMT) of the four channels is hardware programmable by means of a single, external resistor (RLIM):

$$I_{LIMIT} = \frac{1.236 \cdot 2155}{R_{LIM}} .$$

The protection implemented by the thermal monitoring is based on a three levels control system:

A first temperature threshold controls the Power on sequencer (see the Logic Section for a detailed description of its behaviour). When activated (PBIT pin Low), the Power on sequencer manages the channels' activation requests received through the Parallel (PSC pin Low) or the MPI (PSC pin High) interface. The incoming channels' activation requests are stored in the Power on sequencer and then satisfied, one at a time, only when the previously activated channel leaves the current limiting condition that normally occurs at power on, due to the capacitive element that is part of the ISDN load. However when the chip's internal temperature reaches 110°C, only the already stored activation requests will be satisfied; the new, eventually incoming ones, will be rejected and will be processed when the internal temperature decreases down to 100°C.

A second temperature threshold is set at 130°C. When this value is reached the channels that are in current limiting condition are switched off and their reactivation will only be possible when the chip's internal temperature has decreased down to 120°C or, if the Power on sequencer is activated, down to 100°C.

The third temperature threshold is set at 160°C. When this temperature is reached the activated channels will all be switched off and their reactivation will only be possible when the chip's internal temperature has decreased down to 150°C. The user must however take into account that if (like in ISDN application) the load seen by the channel has a high capacitive component, at channel's turn on a current limiting condition will always occur and the eventually reactivated channels will almost instantaneously be switched off by the 130°C monitoring circuit, if the chip's internal temperature is still higher than 120°C. More over (as explained at the previous point) if the Power on sequencer is activated it will not be possible to switch on any channel until the chip has cooled down to 100°C.

Each of the four channels generates two status detector bits (see the block diagram at page 3): the COD bit (**C**urrent **O**verload **D**etector) and the OLD bit (**O**pen **L**oop **D**etector). The functions of the two bits are the following:

The COD bit goes in a High logic state when its channel is in current limiting condition. Since in the ISDN application it can happens that the sum of the DC line current and the superimposed signal peaks, easily exceeds the needed DC current limit, the COD generation circuitry has been arranged in such a way that the COD bit will be pushed High only if the current overload persists for at least 20ms: this eliminates any spurious High level COD. The mentioned delaying function requires, for each of the four channels, one Capacitor of 100nF has to be connected between each CODCn and ground.

The OLD bit goes in a High state logic when the current that the channel supplies to the line falls below a typical value of 3mA, indicating a probable open line condition.

As explained in the following pages, when operating in MPI mode the COD and OLD bits can, for each of the four channels, be red by an external microprocessor in order to check which channel (if any) is over or under loaded. When in Parallel mode a single status bit (the NACKn bit) is provided for each channel and is directly available on a dedicated pin. The NACKn bit is internally generated by OR combining the COD bit with two other bits (see the Logic section for a more detailed explanation).

### Logic Section

The Logic section comprises the **Parallel interface**, the **MPI interface** and the **Power on sequencer**. In the block diagram shown at page 3 the three functions have been condensed in a single entity: the **Logic interface** block.

For each of the four channels, both types of the two provided interfaces use the COD, OLD and TOR (**T**hermal **O**verload **R**egister) status detector bits:

The COD (**C**urrent **O**verload **D**etector) bit is in a High logic state when its channel is in current limiting condition since at least 20ms.

The OLD (**O**pen **L**oop **D**etector) bit is in a High logic state when the current that the channel supplies to the line falls below a typical value of 3mA (ISOC spec's parameter), indicating a possible open line condition.

Each of the four output line drivers can be switched on, **only** if their corresponding TOR bit is High.

The TOR bits are automatically set High by the internal power on reset when the chip is initially connected to its power supplies but can, however, also be globally set High by applying a reset pulse to the RESETN pin. Alternatively the TOR bits that are latched in a Low state can individually be set High by applying to the selected interface the switch off command relative to their channel.

The TOR bits will go in a Low state (determining the shut off of their relative channel's driver) in two cases:

The activated channel is in current limiting condition and the chip's temperature reaches 130°C. In this case the TOR will be latched in Low state.

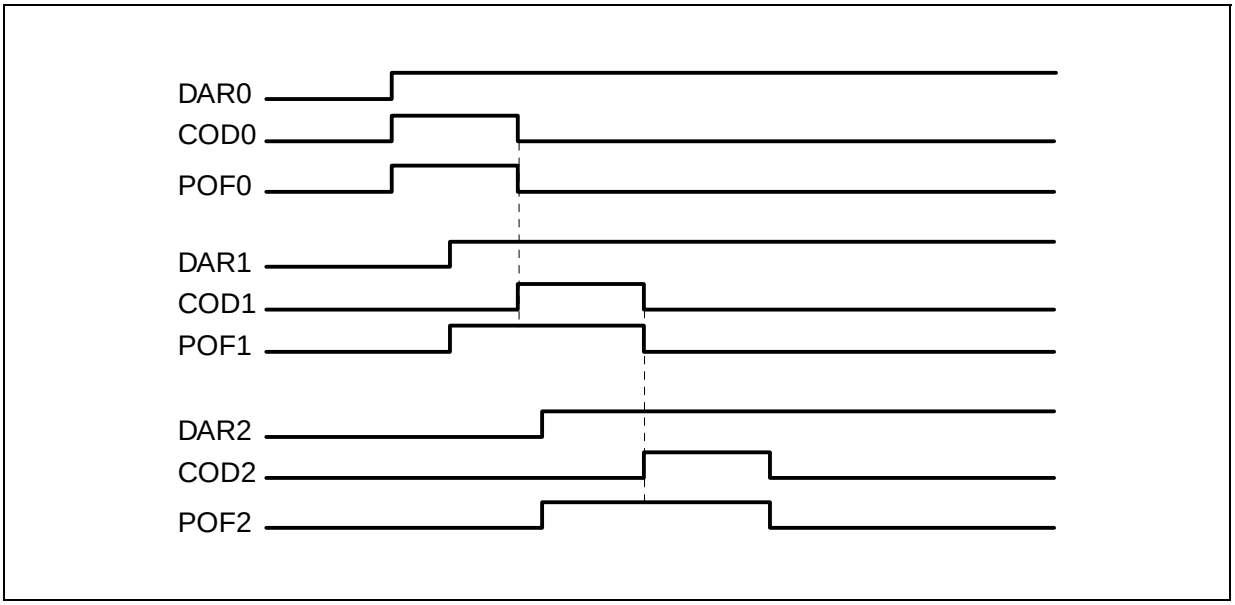
The chip's temperature reaches 160°C: in this case the TOR bits will all be set Low but only the TOR of the activated channels will be latched.

### Power on sequencer

When activated (PBIT pin Low), the Power on sequencer manages the channels' activation requests received through the Parallel (PSC pin Low) or the MPI (PSC pin High) interface. The incoming channels' activation requests are stored in the Power on sequencer and then satisfied, one at a time, only when the previously activated channel exit the current limiting condition that normally occurs at power on, due to the capacitive element that is part of the ISDN load. It must be noted that once a channel exits from the channel's turn on current limiting phase, the fact that it can for example because of a new line overload fall again in a current limiting condition

has no influence in the activation sequence of the next channels. The stored activation requests are satisfied starting from the lower index of the actually stored requests: if (for example) while channel 2 is in the activation phase, additional power on requests arrive for (in the order) channels 1, 3 and 0, when the channel's 2 activation phase will be concluded the stored activation requests will be satisfied in the order 0, 1 and 3. It must be noted that the channels' deactivation requests are not conditioned by the Power on sequencer.

**Figure 7. Power on sequence example**




Notes: DARn are the line **D**rivers' **A**ctivation **R**equest bits sent to the Power on sequencer. They are internally generated starting from the activation requests coming from the outside world through the selected interface (Parallel or MPI). POFn are the **P**ower **O**n **F**lags. Each POFn goes High with its relative DARn bit and returns to a Low state when the current limiting condition ends: a POF High state indicates that the relative channel is in the power on phase.

The figure 6 shows, for three of the four available channels, a typical power on sequence example. The CODn pulse duration represents the time needed to charge the capacitive element that is part of the ISDN load, with part of the constant current that each line driver provides with the actually programmed current limiting value. It must be realized that if (for example) has been required the activation of the lines 0, 2 and 3 but line 2 is overloaded and cannot leave the current limiting condition, the activation sequence will remain blocked at the line 2 activation step. In this case the external software has to identify and shut off the overloaded line in order to allow the activation of the line 3.

The previously mentioned RESETN pin will also influence the Power on sequencer: when RESETN is pushed Low the Power on sequencer is reset, switching off the actually activated drivers.

The Power on sequencer is the only block of the circuit that needs an external clock signal to be applied at the CKILC pin. The clock frequency is not critical and has a nominal value of 8kHz.

When PBIT=1 the power on sequencer is disabled and the incoming channels' activation requests will instantaneously be satisfied. In this case the user as to take into account the actual operative condition (VBAT, the programmed current limiting value, the load applied to the lines, the ambient temperature) and implement his own power on sequence in order to limit the chip's temperature increase induced by the channels' switch on transients.

**Parallel interface mode**

In Parallel interface mode (PSC pin Low), for each of the four output drivers a dedicated activation pin is provided (ES0-ES3):

Each driver will unconditionally be switched off when its ESn is pushed Low.

If the Power on sequencer is not used, each driver will be switched on (under the supervision of the previously described Thermal monitoring block) when its ESn is pushed High.

If the Power on sequencer is activated the drivers' activation requests coming from the ESn inputs will (under the supervision of the previously described Thermal monitoring block) be processed by the Power on sequencer block (see the previous Power on sequencer's description).

In Parallel interface mode a single status bit is provided for each of the four channels at the open drain NACK0 - NACK3 output pins. The NACKn bit is generated by OR combining the three previously described status detector bits: CODn, POFn and the complemented TOR. This means that each NACKn bit goes in high impedance state (bit=1 if a NACKn pull up is externally provided) when at least one of these conditions is verified:

The current on the relative line reaches the current limit programmed by the user (the NACKn High state in this case will not be latched).

The chip's temperature reaches 130°C and the channel is in current limiting condition (the NACKn High state will in this case be latched).

The chip's temperature reaches 160°C (in this case all the NACKn will go in High state, but only the NACKn of the activated channels will be latched).

The line driver is in the power on phase (in this case the NACKn will remain in High state only for the time during which its channel is in current limiting condition).

When the ESn input is set Low, the corresponding NACKn is always set to zero.

In Parallel interface mode the output pin INTN and the input pin ALE are not used (ALE must in this case be tied High or Low).

**MPI interface mode**

In MPI mode (PSC pin High), the ALE and INTN pins become active and the pins NACK0-NACK3 and ES0-ES3 have a function that is completely different from that performed in Parallel mode:

The four NACK0-NACK3 pins become D0 -D3 and act as a bidirectional data bus with three state capability.

The four ES0-ES3 pins become respectively A0, CSN, RDN and WRN.

In MPI mode the above mentioned four bits data bus and three internal four bits registers, LER (**L**ine **E**nable **R**egister), LEC (**L**ine **E**nable **C**ontrol) and IAR (**I**ndirect **A**ddress **R**egister) are used to perform the following operations:

Channels' output drivers switch on and switch off.

Enabling/disabling of the INTN (interrupt) signal generation.

Status detector bits reading.

T bit reading (this bit is High only when the internal chip's temperature exceeds 160°C).

The read/write operations on the data bus can only be performed when the CSN (Chip Select) pin is Low since when CSN is High the data bus is inactive (high impedance state).

The active Low RDN and WRN signals are used to perform the read and write operations on the registers selected by the logic level applied at the A0 pin:

A0=0 selects: The IAR register if a write operation is performed (status detector bits type selection and enabling/disabling of the INTN signal generation via the I bit).

The reading of the bits actually written in the IAR register if a read operation is performed.

A0=1 selects: The LER register if a write operation is performed (switch on and switch off requests programming for the output drivers).

The status detector bits reading if a read operation is performed.

A0 must be valid on the falling edge of the signal applied at the ALE (Address Latch Enable) pin or during the read and write operations if ALE is tied High.

NOTE: A delay of at least 1ms is required between a LER writing and the next LER reading. Subsequent LER reading operations do not have this constraint.

The line output drivers' switch on or switch off requests are implemented by first selecting the LER register and then by writing in its D0-D3 bits a 1 (turn on request) or a 0 (turn off request). D0 controls channel 0, D1 channel 1 and so on. If the requests are accepted by the Thermal monitoring block and (if activated) by the Power on sequencer, the bits stored in the LER register are copied in the LEC register whose status (1 = turn on; 0 = turn off) directly controls the output drivers' ON/OFF condition.

For each of the four channels, in MPI mode the following six status detector bits are available:

The COD, OLD and TOR bits whose function has already been described at the beginning of the Logic Section paragraph.

The LER and the LEC bits.

The POF (**P**ower **O**n **S**equencer) bit already described at the Power on sequencer paragraph.

The status detector bits reading is performed by first writing in the 2 - 0 bits of the IAR register (via the D2-D0 bus lines) a three bits code used to select which of the six available status detector bits type has to be red. A0 must then to be set at 1 and the reading cycle has to be performed. The status detector bits' selection codes are listed in the following table.

If (for example) a 010 code has been written in the IAR, the output on the D0 - D3 lines at the end of the reading cycle will be the COD0 - COD3 bits.

Please, note that since the red data are not latched (apart from the TOR status detector bits of the channels whose output drivers are switched on), the user should filter them (multiple samples) to ensure theirs integrity.

| IAR2 | IAR1 | IAR0 | Selected status detector bits type |
|---|---|---|---|
| 0 | 0 | 0 | POF |
| 0 | 0 | 1 | OLD |
| 0 | 1 | 0 | COD |
| 0 | 1 | 1 | LEC |
| 1 | 0 | 0 | RESERVED |
| 1 | 0 | 1 | RESERVED |
| 1 | 1 | 0 | LER |
| 1 | 1 | 1 | TOR |

As already explained the IAR is a four bits register but only three bits (D2 - D0) are required to select one of the six available status detector bits types. The fourth IAR bit (D3) is the **I bit** and is used to enable (1) or disable (0) the generation of the interrupt signal INTN that, via the INTN pin, can alerts an external microprocessor when a current overload condition occurs. INTN is active (Low level) when at least one of the CODn status detector bits is active (High level). When the four CODn status detector bits are Low, INTN goes inactive (High): this clearly means that INTN will also go inactive if (due to thermal overload) the QLFC automatically disables the output driver of the channel that caused the interrupt or if the external microprocessor disables that line via the LER register.

The interrupt function can also be disabled (INTN remains permanently High) by applying a Low level on the RESETN pin.

As previously explained, when a reading operation is performed while A0 = 0 the four bits actually written in the IAR register can be read on the D3 - D0 bus lines. We already know that the D2 - D0 bits represent the status detector bits selection code. The D3 bit is the T bit: it is High only when the internal chip's temperature exceeds 160°C.

The IAR bits' function has been summarized in the following table:

| Bit | Symbol | Bit function |
|---|---|---|
| 0 | IAR0 | Bit 0 of the status detector bits selection code |
| 1 | IAR1 | Bit 1 of the status detector bits selection code |
| 2 | IAR2 | Bit 2 of the status detector bits selection code |
| 3 | IAR3:<br>T (read)<br><br>I (write) | T bit (read only): Logical 0 when chip's temperature is below 160°C<br>Logical 1 when chip's temperature exceeds 160°C<br><br>I bit (write only): Logical 0 to disable the interrupt generation<br>Logical 1 to enable the interrupt generation |

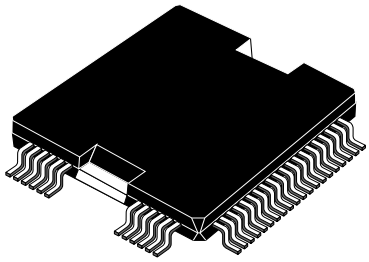
The logic behaviour of the MPI's chip select and read/write operations has been summarized in the following table:

| CSN | RDN | WRN | A0 | Performed operation |
|---|---|---|---|---|
| 0 | 1 | 0 | 0 | Write IAR |
| 0 | 0 | 1 | 0 | Read IAR |
| 0 | 1 | 0 | 1 | Write LER |
| 0 | 0 | 1 | 1 | Read the status detector bits types selected via the IAR |
| 1 | X | X | X | No access |

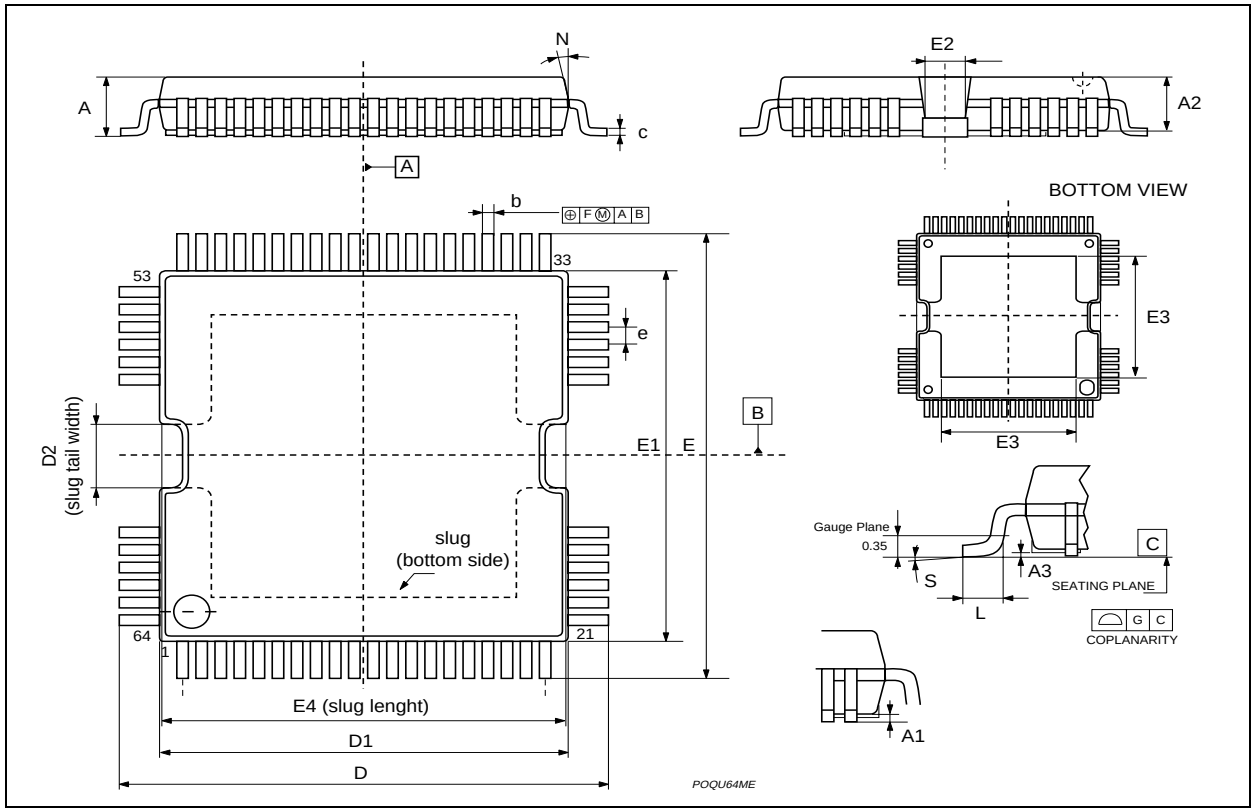
| DIM. | mm | | | inch | | |
|---|---|---|---|---|---|---|
| | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. |
| A | | | 3.15 | | | 0.124 |
| A1 | 0 | | 0.25 | 0 | | 0.010 |
| A2 | 2.50 | | 2.90 | 0.10 | | 0.114 |
| A3 | 0 | | 0.10 | 0 | | 0.004 |
| b | 0.22 | | 0.38 | 0.008 | | 0.015 |
| c | 0.23 | | 0.32 | 0.009 | | 0.012 |
| D | 17.00 | | 17.40 | 0.669 | | 0.685 |
| D1 (1) | 13.90 | 14.00 | 14.10 | 0.547 | 0.551 | 0.555 |
| D2 | 2.65 | 2.80 | 2.95 | 0.104 | 0.110 | 0.116 |
| E | 17.00 | | 17.40 | 0.669 | | 0.685 |
| E1 (1) | 13.90 | 14.00 | 14.10 | 0.547 | 0.551 | 0.555 |
| e | | 0.65 | | | 0.025 | |
| E2 | 2.35 | | 2.65 | 0.092 | | 0.104 |
| E3 | 9.30 | 9.50 | 9.70 | 0.366 | 0.374 | 0.382 |
| E4 | 13.30 | 13.50 | 13.70 | 0.523 | 0.531 | 0.539 |
| F | | 0.10 | | | 0.004 | |
| G | | 0.12 | | | 0.005 | |
| L | 0.80 | | 1.10 | 0.031 | | 0.043 |
| N | 10°(max.) | | | | | |
| S | 0°(min.), 7°(max.) | | | | | |

(1): "D1" and "E1" do not include mold flash or protusions
- Mold flash or protusions shall not exceed 0.15mm(0.006inch) per side

## OUTLINE AND MECHANICAL DATA



## HiQUAD-64



**ESD -** The STMicroelectronics Internal Quality Standards set a target of 2KV that each pin of the device should withstand in a series of tests based on the Human Body Model (MIL-STD 883 Method 3015): with C = 100pF; R = 1500Ω and performing 3 pulses for each pin versus $V_{CC}$ and GND.
Device characterization showed that, in front of the STMicroelectronics Internaly Quality Standards, all pins of STLC5445 withstand at least 1500V.
The above points are not expected to represent a pratical limit for the correct device utilization nor for its reliability in the field. Nonetheless they must be mentionned in connection with the applicability of the different SURE 8 requirements to STLC5445.