CopperWing12e

ADSL2+ Central Office (CO) Chipset: STLC61266/65 + STLC60454 + STLC60243

DATA BRIEF

www.DataSheet4U.com

1 General Description

The CopperWing12e ADSL2+ chipset targets a complete set of solution for Central Office (CO) ADSL technology integrating also processing and management capability to provide the best solution for ATM/IP DSLAM, ATM/IP mini DSLAM and "Pizza" boxes. The chipset integrates all ADSL/ADSL2+ functions from ATM/IP interfaces to the line in three devices:

- Two data pump chip options:
  - **STLC61265:** 12 channels ATM ADSL2+ Data Pump
  - **STLC61266:** 12 Channels ATM/IP ADSL2+ data Pump with embedded Cell Processor
- **STLC60454:** 4 Ch ADSL/ADSL2+ AFE with integrated receiver and LP filters
- **STLC60243:** Dual channel Line Driver

The CopperWing12e chipset is a 2nd Generation ADSL2+ CO Chipset with the following main feature upgrades versus the original CopperWing12 chipset:

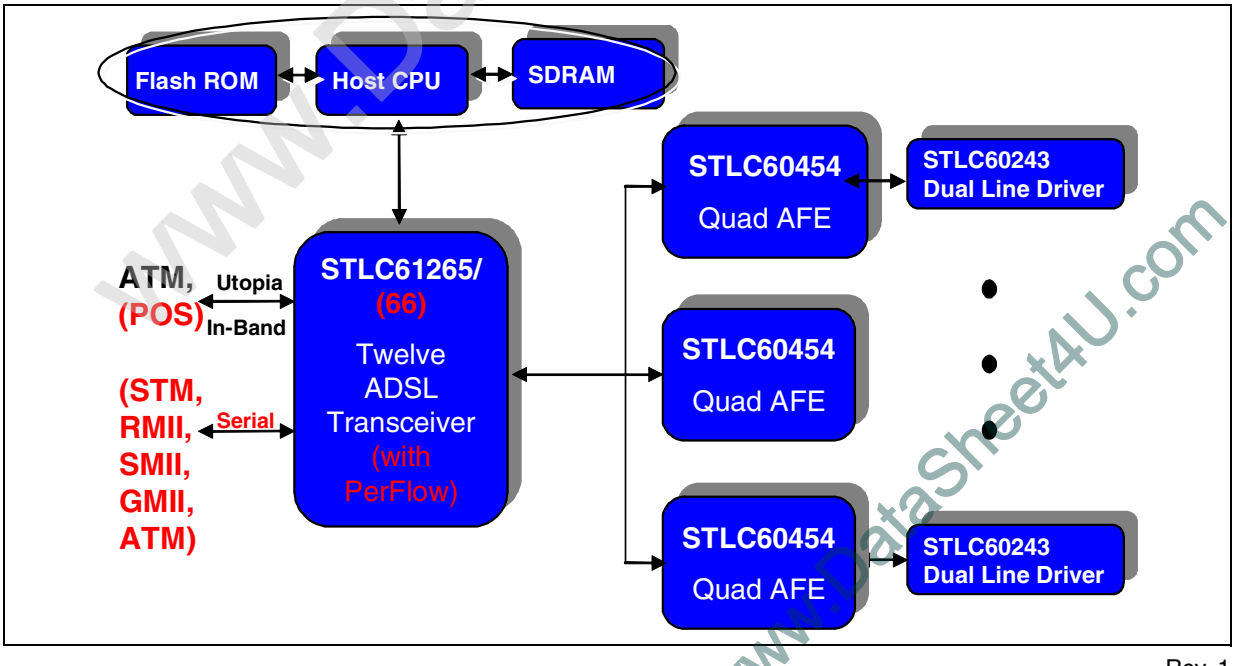
- Significantly enhanced Cell Processor throughput capability
- Dual GMII interfaces
- ATM Header compression support
- EFM PTM support (TC 64/65)

CopperWing12e chipset provides Ethernet and ATM interfaces to fit IP and ATM based Remote Unit or CO line cards.

The Modem Control Software runs entirely on the DMT Transceiver (no external memory needed for Interleave memory or modem SW): the line card host controller is in charge only of high-level management operation. The chipset is able to support not only the current ADSL standards, but also ADSL2 and ADSL2+ (12 channels).

With only 1 square inches and less than 1 Watt per channel (in ADSL mode, 1.15W/line in ADSL2+ mode), the Copperwing12e chipset is one of the most competitive solutions for CO ADSL application. The chip set supports also ADSL2+ mode to deliver higher bit rate (24Mb/s) on short loops while with Reach Extended ADSL is able to guarantee high reach performance.

Figure 1. Chipset Architecture Overview



www.DataSheet4U.com

This is preliminary information on a new product foreseen to be developed. Details are subject to change without notice.

2 ADSL supported standards

- T1.413 Issue 2
- ETSI RTS/TM 06006 - ADSL over ISDN
- ITU G.992.1 - G.dmt, Annexes A, B, C, I
  - Amendment to G.992.1 Annex C
- ITU G.994.1 - G.hs rev 2.
- ITU G.992.2 - G.lite, Annexes A, B, C.
- G.992.3 - G.dmt.bis, Annex A, B, C, I, J, L, M
- G.992.4 - G.lite.bis
- G.992.5 - G.adslplus, Annex A, B, C, I, J, M
- RE-ADSL
- Metallic loop testing

3 Perflow ATM/IP Cell Processor features

- Network processing functionality on the line card
  - First stage switching
- Cell and Packet processing
  - AAL5 and AAL2 SAR functions on chip
  - ATM line card switch
  - PTM-TC (Packet Over HDLC & Packet over 64/65B)
  - Traffic Management and Policing
- Configurable backplane interfaces
  - Utopia Level 2&3, PoS, RMII, SMII, GMII, Serial ATM, STM

12 CHANNEL DMT ADSL DATA PUMP

DATA BRIEF

4 Main Features

- Support for 12 independent ports.
- Low power consumption
- Category II Functionality: Trellis coding and Echo cancellation
- Flexible bin assignment: Supports ADSL over POTS, ADSL over ISDN, all digital loop and overlapping spectra.
- TC layer supporting: ATM TC
- No external memory needed for Interleave memory nor modem SW
- No real time requirements from the controller
- Each modem can be different phase (startup/ Showtime) independently of other modems
- Package: PBGA676 27x27mm
- 0.13um CMOS technology
- 1.2V core logic supply (3.3V for I/O)
- -40°C to +85°C operation

Figure 1. Package

PBGA676 (27 x 27mm)

Table 1. Order Codes

Part Number	Package
STLC61265	PBGA676
E-STLC61265(1)	PBGA676

(1) ECOPACK®: lead free package.

5 Description

The STLC61265 twelve channels ADSL Transceiver is the key component for Asymmetrical Digital Subscriber Line (ADSL) Central Office modem implementation. The highly integrated device supports category II ADSL functionalities, including trellis coding and echo cancellation. The device embodies 6 independent dual transceivers optimized for Central Office operation, with bit rates of up to 3.0 Mbps upstream (Annex M) and 24 Mbps downstream. This device is ideal for power and area sensitive Central Office equipment, providing highest performance and density while meeting all telecom grade equipment requirements. The STLC61265 is designed for minimal host controller intervention during runtime operation. Combining this feature with additional management interfaces such as the serial host interface and the In-band Utopia management interface provides many alternatives for designs that significantly reduce operation complexity and cost. Cost saving can be achieved by using a singe low-cost controller to support high-density line-cards, saving the need for on-board flash memory or even the entire host processor environment. The STLC61265 host interface provides a full support of the ADSL MIB, and a rich set of statistic information and programmable fault alarms.

This is preliminary information on a new product foreseen to be developed. Details are subject to change without notice.

STLC61266

12 CHANNEL DMT ADSL DATA PUMP WITH ENHANCED IP/ATM CELL PROCESSOR

DATA BRIEF

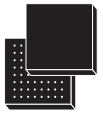
6 Main Features

- Support for 12 independent ports.
- Low power consumption.
- Category II Functionality: Trellis coding and Echo cancellation.
- Flexible bin assignment: Supports ADSL over POTS, ADSL over ISDN, all digital loop and overlapping spectra.
- TC layer supporting: STM TC, ATM TC, PTM TC as required by G.dmt.bis annex K as EFM PTM-TC (64/65).
- ATM Header Compression.
- Includes PerFlow Cell Processor
  - AAL5/2 SAR
  - Policing and Scheduling 4 priorities
  - Supports ATM and IP simultaneously per port
  - Full switching capability
- No external memory needed for Interleave memory nor modem SW (for advanced PerFlow applications external SDRAM needed).
- No real time requirements from the controller.
- Each modem can be different phase (startup/ Showtime) independently of other modems.
- Package: PBGA676 27x27mm.
- 0.13um CMOS technology.
- 1.2V core logic supply (3.3V for I/O).
- -40°C to +85°C operation.

7 Description

The STLC61266 twelve channels ADSL Transceiver is an advanced component for ADSL Central Office modem implementation. The embedded IP/ATM Cell Processor allows to simplify the design of high density CO line cards and to develop a single platform that supports IP or ATM based equipments. It allows also different line card architecture with the possibility to also have chaining of several STLC61266 devices on the same card.

Figure 1. Package



PBGA676 (27 x 27mm)

Table 1. Order Codes

Part Number	Package
STLC61266	PBGA676
E-STLC61266(1)	PBGA676

(1) ECOPACK®: lead free package.

External DRAM is required only for full PerFlow feature support (i.e. MAC or VPI/VCI switching, Hash support, large number of voice+data connections per channel). The highly integrated device supports category II ADSL functionalities, including trellis coding and echo cancellation. The device embodies 6 independent dual transceivers optimized for Central Office operation, with bit rates of up to 3.0 Mbps upstream (Annex M) and 24 Mbps downstream. This device is ideal for power and area sensitive Central Office equipment, providing highest performance and density while meeting all telecom grade equipment requirements.

The STLC61266 is designed for minimal host controller intervention during runtime operation. Combining this feature with additional management interfaces such as the serial host interface and the In-band Utopia/Ethernet management interface provides many alternatives for designs that significantly reduce operation complexity and cost. Cost saving can be achieved by using a singe low-cost controller to support high-density line-cards, saving the need for on-board flash memory or even the entire host processor environment. The STLC61266 host interface provides a full support of the ADSL MIB, and a rich set of statistic information and programmable fault alarms.

This is preliminary information on a new product foreseen to be developed. Details are subject to change without notice.

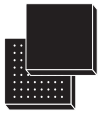
4 CHANNEL ADSL/ADSL+ AFE

DATA BRIEF

8 Main Features

- Tx Path
  - Low pass filter
  - Programmable Gain Amplifier
- Rx Path
  - Programmable filters
  - Internal Low Noise Amplifier
- ITU-T and ANSI Tone Detection per channel
- Per channel Power Down Function
- Fully Programmable through the Data Pump Interface (STLC61265/6)
- 144-pin LBGA package (13x13mm)
- Power consumption 0.9W (225mW/line)
- 0.35 um technology
- Single 3.3V supply
- Extended temperature range

Figure 1. Package



LBGA144 (13 x 13mm)

Table 1. Order Codes

Part Number	Package
STLC60454	LBGA144
E-STLC60454(1)	LBGA144

(1) ECOPACK®: lead free package.

9 Description

The STLC60454 is a 4 channel ADSL AFE. It implements four analog transceiver functions required for a central office modem. It connects the digital modem chip with the line driver and hybrid balance circuit.

This 4 channel AFE has been designed with high dynamic range in order to greatly reduce the external filter requirements. Each single channel can be put in power down mode and provides programmable filters in the receive path. No external receiver is required.

This is preliminary information on a new product foreseen to be developed. Details are subject to change without notice.

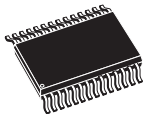
DUAL CHANNEL ADSL LINE DRIVER

DATA BRIEF

10 Main Features

- Low Noise: 3.5nV/Hz
- Class AB architecture
- High Peak Output Current: 600 mA
- Low Single Tone Distortion: -60dBc
- Thermal And Overload Protection
- BCD-SOI technology
- HTSSOP28 Package
- -40 TO +85°C Operating Range

Figure 1. Package



HTSSOP28

Table 1. Order Codes

Part Number	Package
STLC60243	HTSSOP28
E-STLC60243(1)	HTSSOP28

(1) ECOPACK®: lead free package.

11 Description

The STLC60243 is a dual channel ADSL Line Driver featuring a high slew rate and a large bandwidth optimized for XDSL applications (ADSL and ADSL+). The device is available in a HTSSOP 28 pin package (4x9 mm) with an exposed lead frame. The STLC60243 is designed optimizing bandwidth, distortion performances and power consumption.

This is preliminary information on a new product foreseen to be developed. Details are subject to change without notice.

12 Revision History

Table 1. Revision History

Date	Revision	Description of Changes
May 2005	1	First Issue.

Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

The ST logo is a registered trademark of STMicroelectronics.
All other names are the property of their respective owners

© 2005 STMicroelectronics - All rights reserved

STMicroelectronics group of companies
Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America
www.st.com