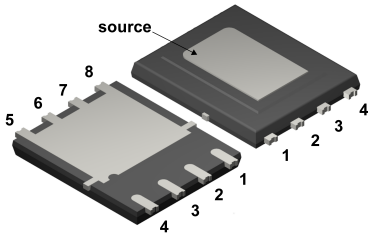
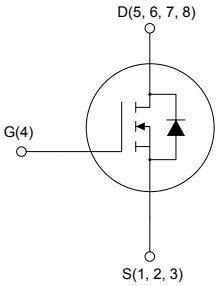
N-channel 100 V, 5 mΩ typ., 107 A STripFET™ F7 Power MOSFET in a PowerFLAT™ 5x6 dual side cooling package



PowerFLAT™ 5x6 dual side cooling



AM15540v4

Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STLD110N10F7	100 V	6 mΩ	107 A

- Among the lowest $R_{DS(on)}$ on the market
- Excellent FoM (figure of merit)
- Low C_{rss}/C_{iss} ratio for EMI immunity
- High avalanche ruggedness

Applications

- Switching applications

Description

This N-channel Power MOSFET utilizes STripFET™ F7 technology with an enhanced trench gate structure that results in very low on-state resistance, while also reducing internal capacitance and gate charge for faster and more efficient switching.

Product status link
STLD110N10F7

Product summary	
Order code	STLD110N10F7
Marking	110
Package	PowerFLAT™ 5x6 dual side cooling
Packing	Tape and reel

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	100	V
V_{GS}	Gate-source voltage	±20	V
I_D (1)	Drain current (continuous) at T_C = 25 °C	107	A
	Drain current (continuous) at T_C = 100 °C	80	A
I_{DM} (2) (1)	Drain current (pulsed)	428	A
P_{TOT} (1)	Total power dissipation at T_C = 25 °C	150	W
I_D (3) (2)	Drain current (continuous) at T_{pcb} = 25 °C	21	A
	Drain current (continuous) at T_{pcb} = 100 °C	14	A
I_{DM} (2) (3)	Drain current (pulsed)	84	A
P_{TOT} (3)	Total power dissipation at T_{pcb} = 25 °C	4.8	W
T_J	Operating junction temperature range	- 55 to 175	°C
T_{stg}	Storage temperature range		

1. *This value is rated according to $R_{thj\text{-}case}$ bottom side.*
2. *Pulse width limited by safe operating area*
3. *This value is rated according to $R_{thj\text{-}pcb}$*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}c\ top\ side}$	Thermal resistance junction-case top side	2.8	°C/W
$R_{thj\text{-}c\ bottom\ side}$	Thermal resistance junction-case bottom side	1	
$R_{thj\text{-}pcb}$ (1)	Thermal resistance junction-pcb	31.3	

1. *When mounted on 1 inch² 2 Oz. Cu board, t ≤ 10 s*

2 Electrical characteristics

(T_C= 25 °C unless otherwise specified)

Table 3. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 250 µA	100			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 100 V			1	µA
		V_{GS} = 0 V, V_{DS} = 100 V, Tj = 125 °C (1)			10	µA
I_{GSS}	Gate body leakage current	V_{DS} = 0 V, V_{GS} = 20 V			100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2.5		4.5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 10 A		5	6	mΩ

1. *Defined by design, not subject to production test.*

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS}= 50 V, f = 1 MHz, V_{GS} = 0 V	-	5117	-	pF
C_{oss}	Output capacitance		-	992	-	pF
C_{rss}	Reverse transfer capacitance		-	39	-	pF
Q_g	Total gate charge	V_{DD} = 50 V, I_D = 21 A, V_{GS} = 0 to 10 V (see Figure 13. Test circuit for gate charge behavior)	-	72	-	nC
Q_{gs}	Gate-source charge		-	30	-	nC
Q_{gd}	Gate-drain charge		-	17	-	nC

Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 50 V, I_D = 10 A, R_G = 4.7 Ω, V_{GS} = 10 V (see Figure 12. Test circuit for resistive load switching times and Figure 17. Switching time waveform)	-	25	-	ns
t_r	Rise time		-	36	-	ns
$t_{d(off)}$	Turn-off delay time		-	52	-	ns
t_f	Fall time		-	21	-	ns

Table 6. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{SD} (1)	Forward on voltage	V_{GS} = 0 V, I_{SD} = 21 A	-		1.2	V
t_{rr}	Reverse recovery time	I_{SD} = 21 A, di/dt = 100 A/µs, V_{DD} = 80 V, T_j= 150 °C (see Figure 14. Test circuit for inductive load switching and diode recovery times)	-	77		ns
Q_{rr}	Reverse recovery charge		-	150		nC
I_{RRM}	Reverse recovery current		-	4.3		A

1. *Pulse test: pulse duration = 300 µs, duty cycle 1.5%*

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

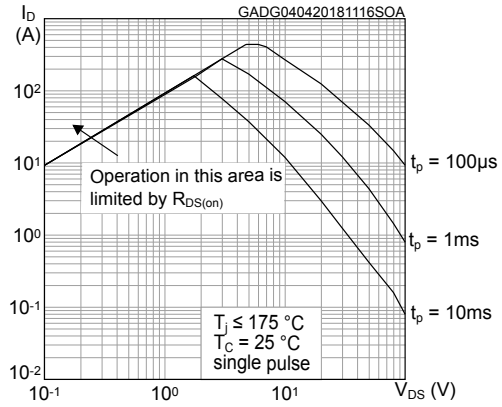


Figure 2. Thermal impedance

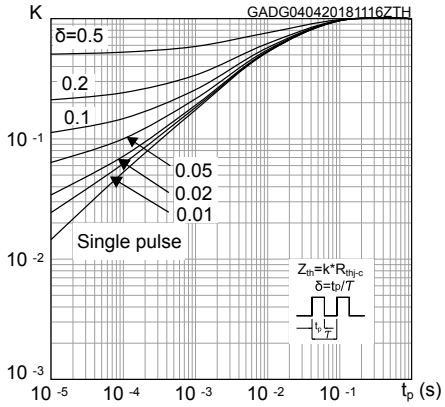


Figure 3. Output characteristics

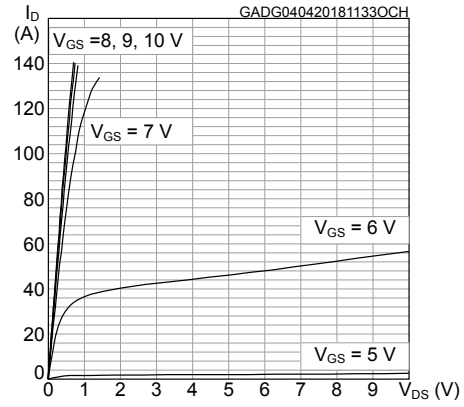


Figure 4. Transfer characteristics

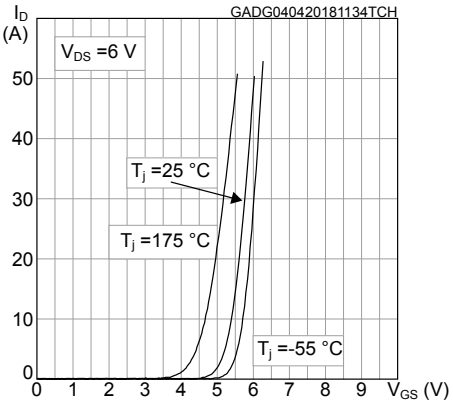


Figure 5. Gate charge vs gate-source voltage

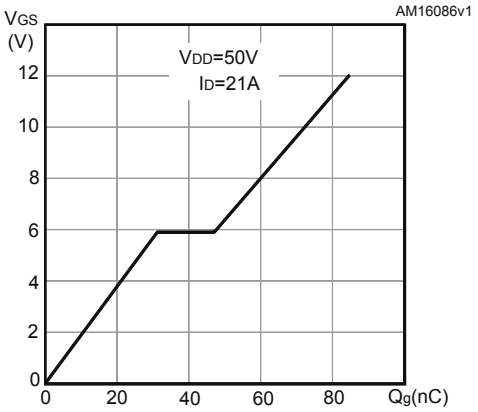


Figure 6. Static drain-source on-resistance

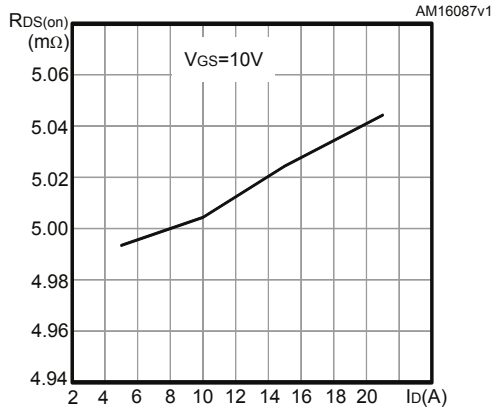


Figure 7. Capacitance variations

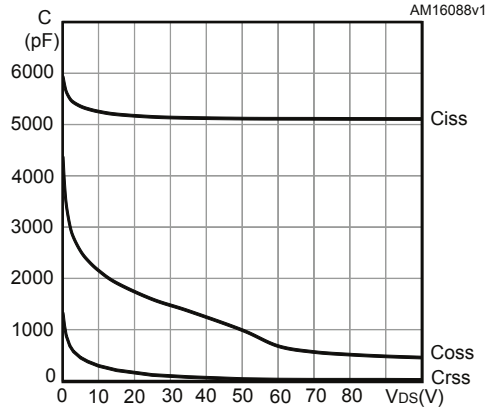


Figure 8. Normalized gate threshold voltage vs temperature

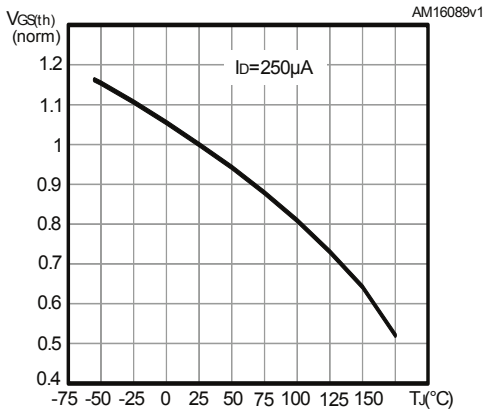


Figure 9. Normalized on-resistance vs temperature

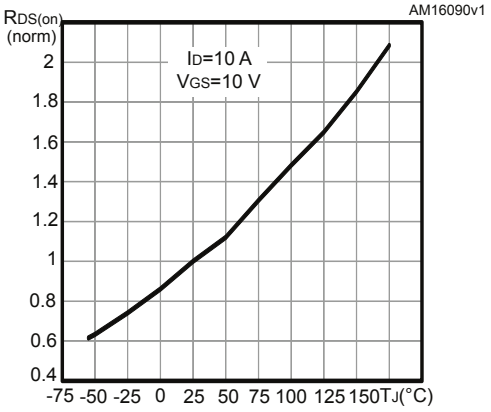


Figure 10. Normalized $V_{(BR)DSS}$ vs temperature

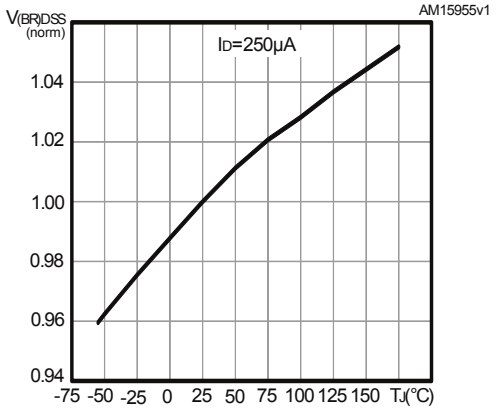
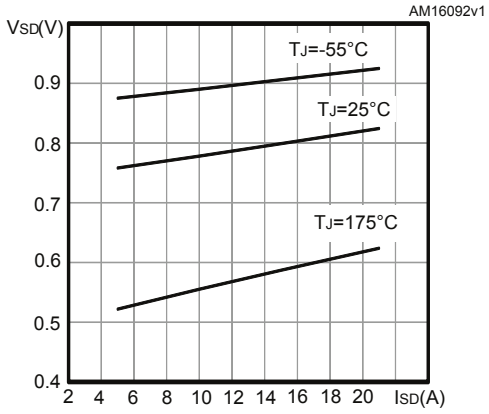


Figure 11. Source-drain diode forward characteristics



3 Test circuits

Figure 12. Test circuit for resistive load switching times

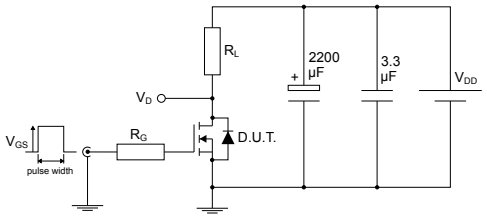


Figure 13. Test circuit for gate charge behavior

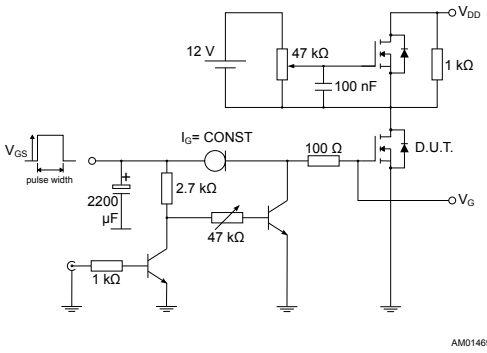


Figure 14. Test circuit for inductive load switching and diode recovery times

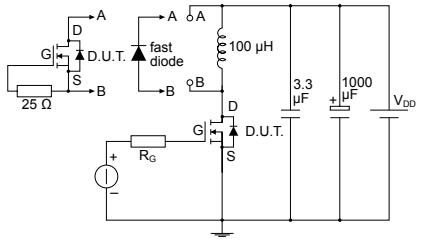


Figure 15. Unclamped inductive load test circuit

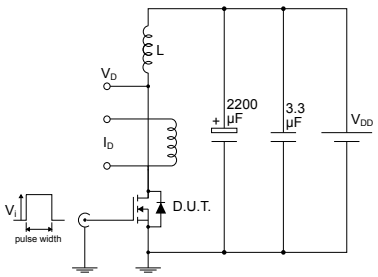


Figure 16. Unclamped inductive waveform

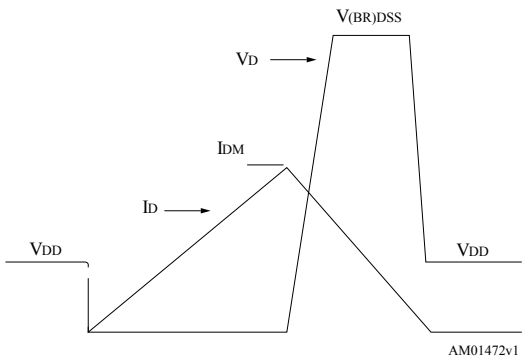
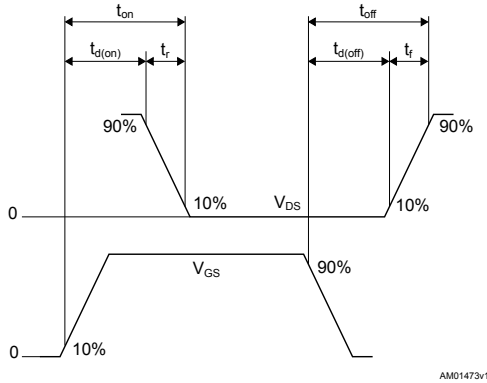


Figure 17. Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 PowerFLAT™ 5x6 dual side cooling package information

Figure 18. PowerFLAT™ 5x6 dual side cooling package outline

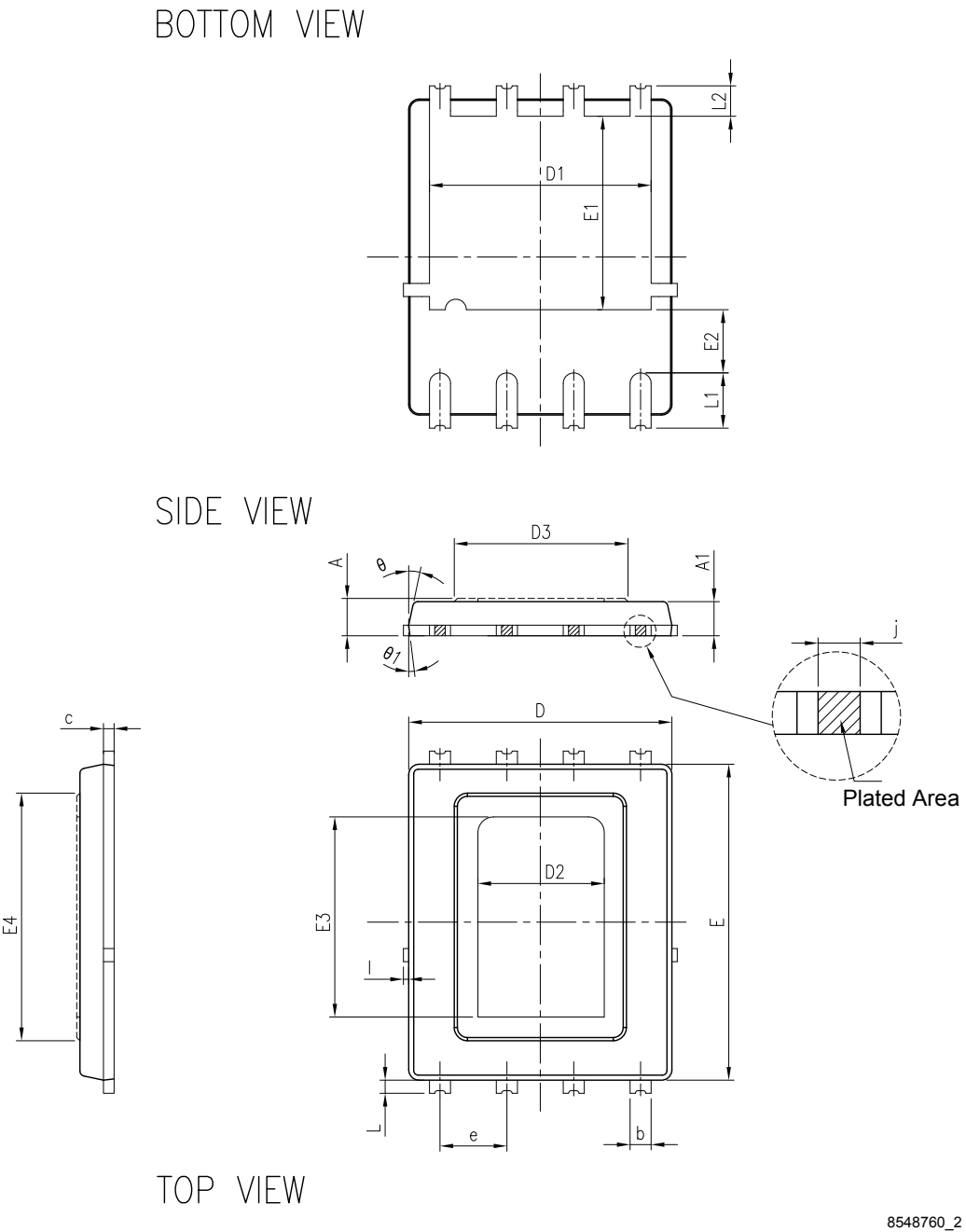
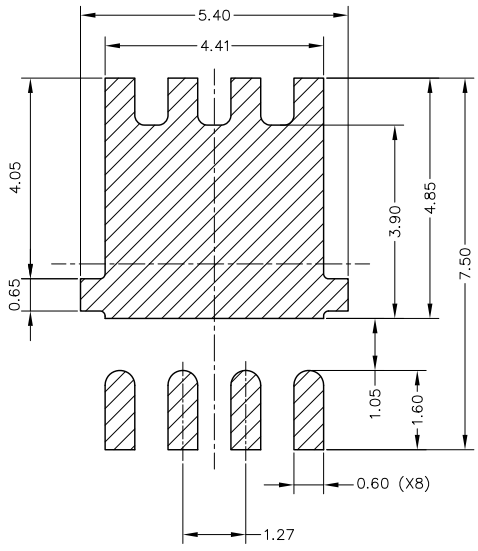


Table 7. PowerFLAT™ 5x6 dual side cooling mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.66	0.71	0.76
A1	0.60		0.75
b	0.33	0.43	0.53
c	0.15	0.203	0.30
D		5.00 BSC	
D1	4.06	4.21	4.36
D2		2.40 BSC	
D3	2.80	3.30	3.80
E		6.00 BSC	
E1	3.525	3.675	3.825
E2	1.05	1.20	1.35
E3		3.80 BSC	
E4	4.20	4.70	5.20
e		1.27 BSC	
I			0.15
L	0.15	0.25	0.35
L1	0.925	1.05	1.175
L2	0.45	0.575	0.70
ϑ		12° BSC	
ϑ1		7° BSC	
j		0.20 BSC	

Figure 19. PowerFLAT™ 5x6 dual side cooling recommended footprint (dimensions are in mm)



4.2 PowerFLAT™ 5x6 dual side cooling packing information

Figure 20. PowerFLAT™ 5x6 dual side cooling tape (dimensions are in mm)

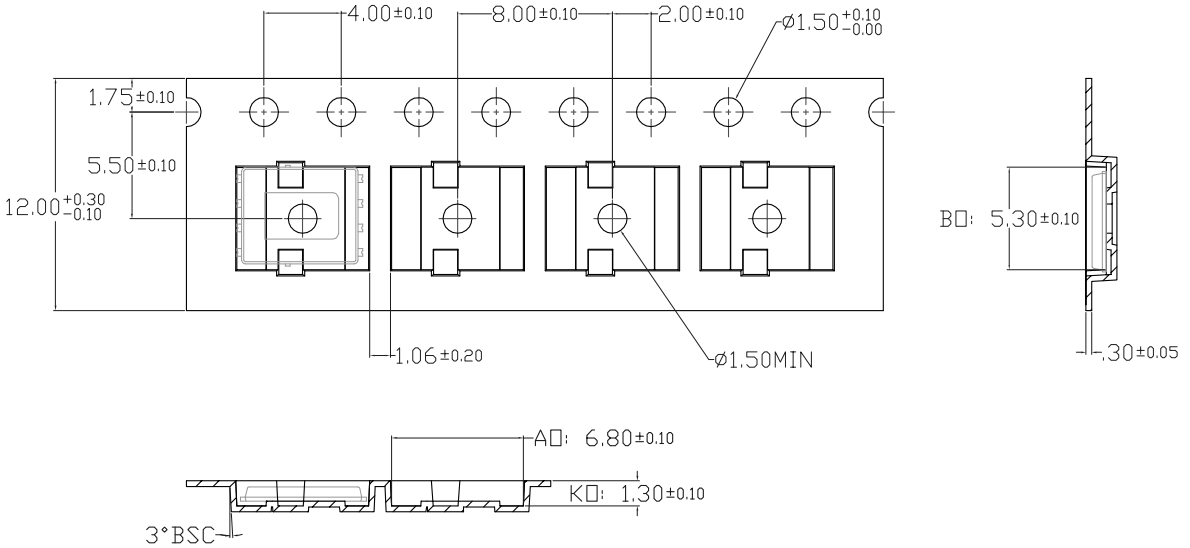


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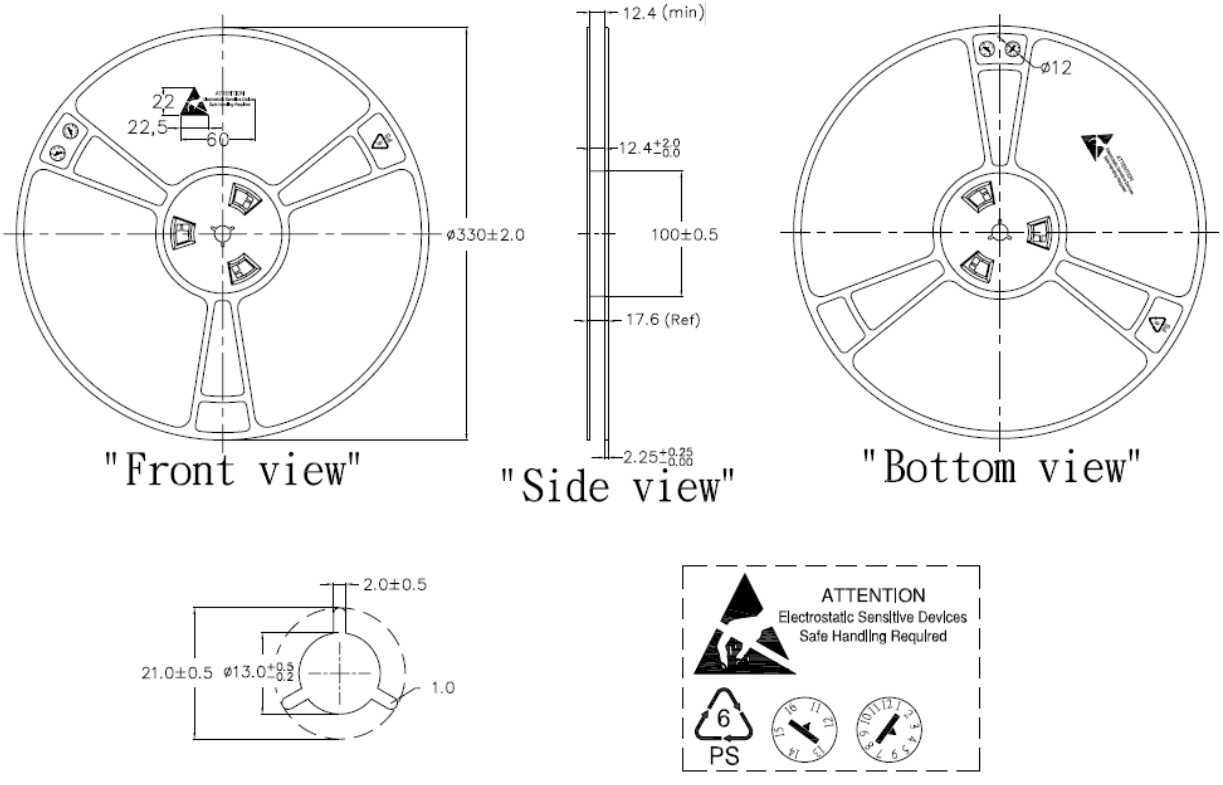
Figure 21. PowerFLAT™ 5x6 dual side cooling reel (dimensions are in mm)



Revision history

Table 8. Document revision history

Date	Revision	Changes
16-Nov-2016	1	First release
19-Dec-2016	2	Updated title and features in cover page. Minor text changes.
09-Apr-2018	3	Removed maturity status indication from cover page. The document status is preliminary data. Updated *Table 6. Source-drain diode* and *inserted Section 2.1 Electrical characteristics (curves).* Inserted *Section 4.2 PowerFLAT™ 5x6 dual side cooling packing information.*
26-Feb-2019	4	Modified Table 3. On/off states. Minor text changes.

Contents

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