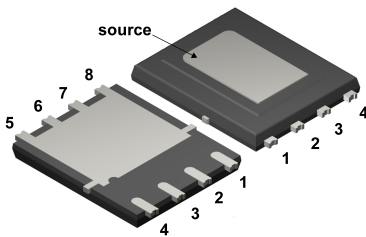
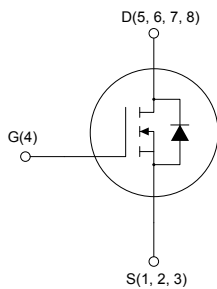


Automotive-grade N-channel 40 V, 0.82 mΩ typ., 120 A, STripFET™ F7 Power MOSFET in a PowerFLAT™ 5x6 DSC package



PowerFLAT™ 5x6 dual side cooling



AM15540v4



Product status link


[STLD257N4F7AG](#)

Product summary

Order code	STLD257N4F7AG
Marking	257
Package	PowerFLAT™ 5x6 dual side cooling
Packing	Tape and reel

Features

Order code	V _{DS}	R _{DS(on)} max.	I _D
STLD257N4F7AG	40 V	1.1 mΩ	120 A

- AEC-Q101 qualified 
- Among the lowest R_{DS(on)} on the market
- Excellent FoM (figure of merit)
- Low C_{rss}/C_{iss} ratio for EMI immunity
- High avalanche ruggedness
- Wettable flank package

Applications

- Switching applications

Description

This N-channel Power MOSFET utilizes STripFET™ F7 technology with an enhanced trench gate structure that results in very low on-state resistance, while also reducing internal capacitance and gate charge for faster and more efficient switching.

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	40	V
V_{GS}	Gate-source voltage	± 20	V
$I_D^{(1)(2)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	120	A
$I_D^{(1)(2)}$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	120	A
$I_{DM}^{(2)(3)}$	Drain current (pulsed)	480	A
$P_{TOT}^{(2)}$	Total power dissipation at $T_C = 25\text{ }^\circ\text{C}$	158	W
T_J	Operating junction temperature range	-55 to 175	$^\circ\text{C}$
T_{stg}	Storage temperature range		

1. Limited by package
2. The value is rated according to $R_{thj-case}$ bottom side.
3. Pulse width limited by safe operating area

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thj-c} top side	Thermal resistance junction-case top side	2.90	$^\circ\text{C/W}$
R_{thj-c} bottom side	Thermal resistance junction-case bottom side	0.95	
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	31.3	

1. When mounted on an 1-inch² 2 Oz, Cu board, $t \leq 10\text{ s}$

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AV}	Avalanche current, repetitive or not repetitive (pulse width limited by maximum junction temperature)	50	A
E_{AS}	Single pulse avalanche energy (starting $T_j = 25\text{ }^\circ\text{C}$, $I_D = I_{AV}$, $V_{DD} = 25\text{ V}$)	608	mJ

2 Electrical characteristics

($T_C = 25\text{ °C}$ unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$, $I_D = 1\text{ mA}$	40			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$, $V_{DS} = 40\text{ V}$			1	μA
		$V_{GS} = 0\text{ V}$, $V_{DS} = 16\text{ V}$, $T_j = 125\text{ °C}^{(1)}$			300	μA
I_{GSS}	Gate-body leakage current	$V_{DS} = 0\text{ V}$, $V_{GS} = 20\text{ V}$			100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	2.0		4.0	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 60\text{ A}$		0.82	1.1	m Ω
		$V_{GS} = 6.5\text{ V}$, $I_D = 60\text{ A}$		3.1	4.8	

1. Defined by design, not subject to production test.

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 25\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$	-	5400	-	pF
C_{oss}	Output capacitance		-	1870	-	pF
C_{rSS}	Reverse transfer capacitance		-	45	-	pF
Q_g	Total gate charge	$V_{DD} = 20\text{ V}$, $I_D = 120\text{ A}$,	-	66.5	-	nC
Q_{GS}	Gate-source charge	$V_{GS} = 0\text{ to }10\text{ V}$	-	33.5	-	nC
Q_{gd}	Gate-drain charge	(see Figure 13. Test circuit for gate charge behavior)	-	13	-	nC

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 20\text{ V}$, $I_D = 60\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$	-	28	-	ns
t_r	Rise time		-	19	-	ns
$t_{d(off)}$	Turn-off delay time	(see Figure 12. Test circuit for resistive load switching times and Figure 17. Switching time waveform)	-	58	-	ns
t_f	Fall time		-	32	-	ns

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}^{(1)}$	Source-drain current		-		120	A
$I_{SDM}^{(1)(2)}$	Source-drain current (pulsed)		-		480	A
$V_{SD}^{(3)}$	Forward on voltage	$V_{GS} = 0\text{ V}$, $I_{SD} = 90\text{ A}$	-		1.1	V
t_{rr}	Reverse recovery time	$I_{SD} = 120\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$,	-	54		ns
Q_{rr}	Reverse recovery charge	$V_{DD} = 20\text{ V}$	-	53		nC
I_{RRM}	Reverse recovery current	(see Figure 14. Test circuit for inductive load switching and diode recovery times)	-	1.9		A

1. Limited by package.
2. Pulse width is limited by safe operating area.
3. Pulse test: pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

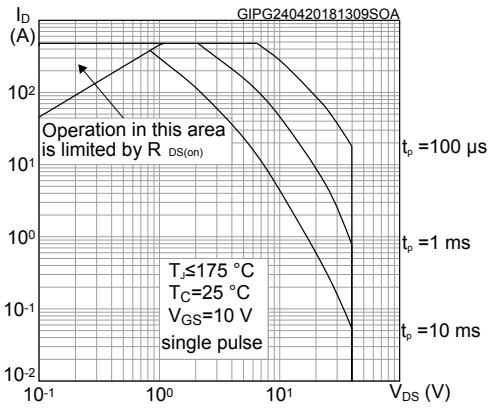


Figure 2. Thermal impedance

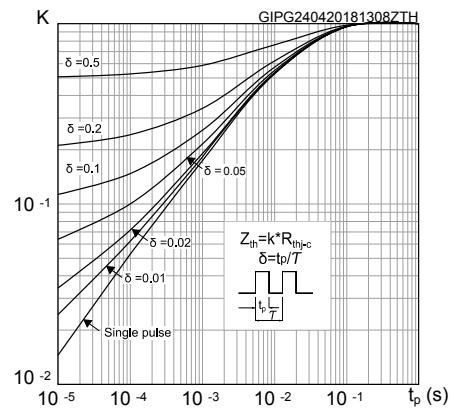


Figure 3. Output characteristics

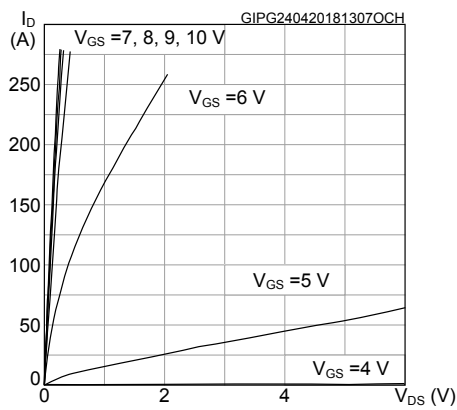


Figure 4. Transfer characteristics

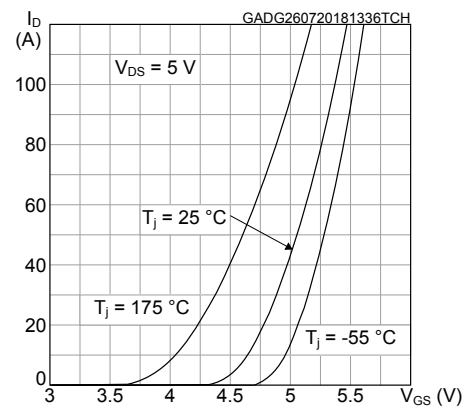


Figure 5. Gate charge vs gate-source voltage

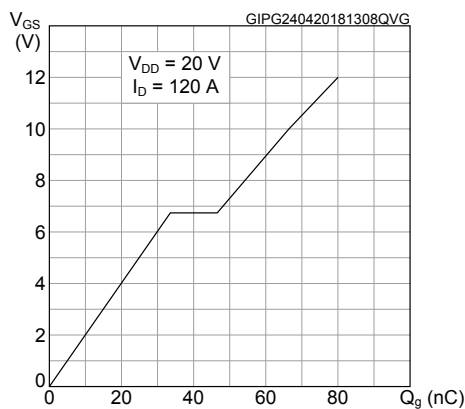


Figure 6. Static drain-source on-resistance

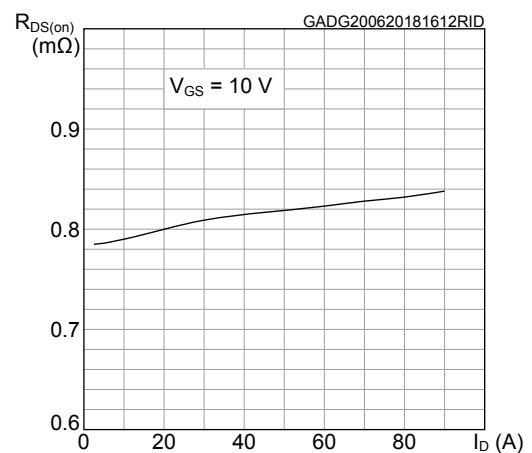


Figure 7. Capacitance variations

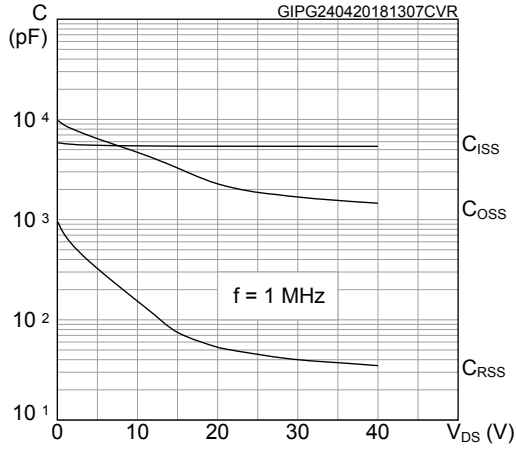


Figure 8. Normalized gate threshold voltage vs temperature

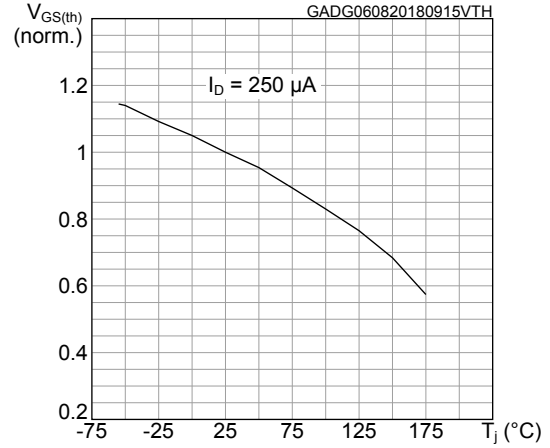


Figure 9. Normalized on-resistance vs temperature

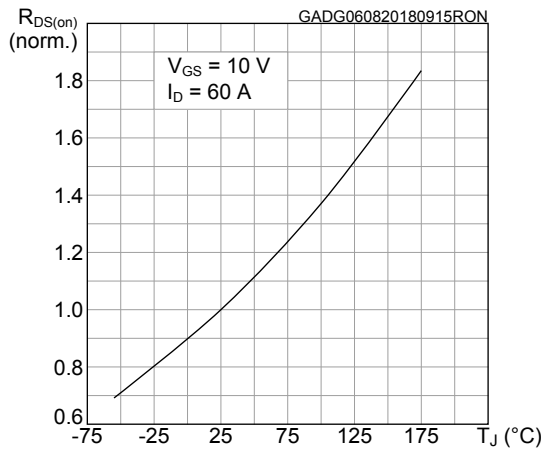


Figure 10. Normalized $V_{(BR)DSS}$ vs temperature

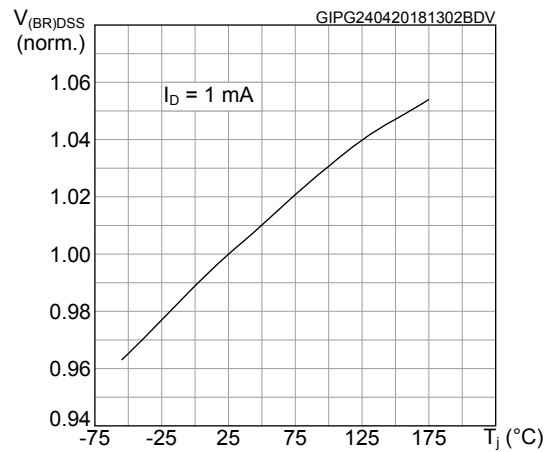
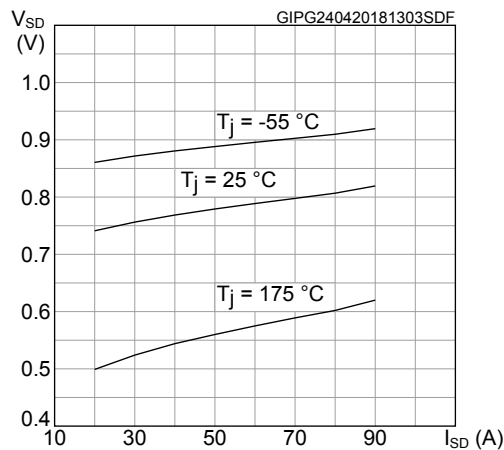


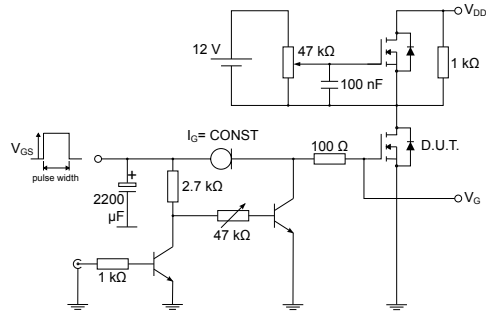
Figure 11. Source-drain diode forward characteristics



3 Test circuits

Figure 12. Test circuit for resistive load switching times


AM01468v1

Figure 13. Test circuit for gate charge behavior


AM01469v1

Figure 14. Test circuit for inductive load switching and diode recovery times


AM01470v1

Figure 15. Unclamped inductive load test circuit


AM01471v1

Figure 16. Unclamped inductive waveform


AM01472v1

Figure 17. Switching time waveform


AM01473v1

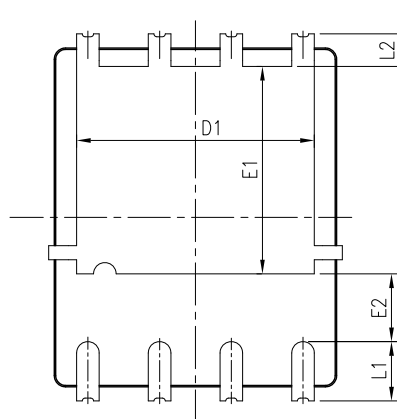
4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

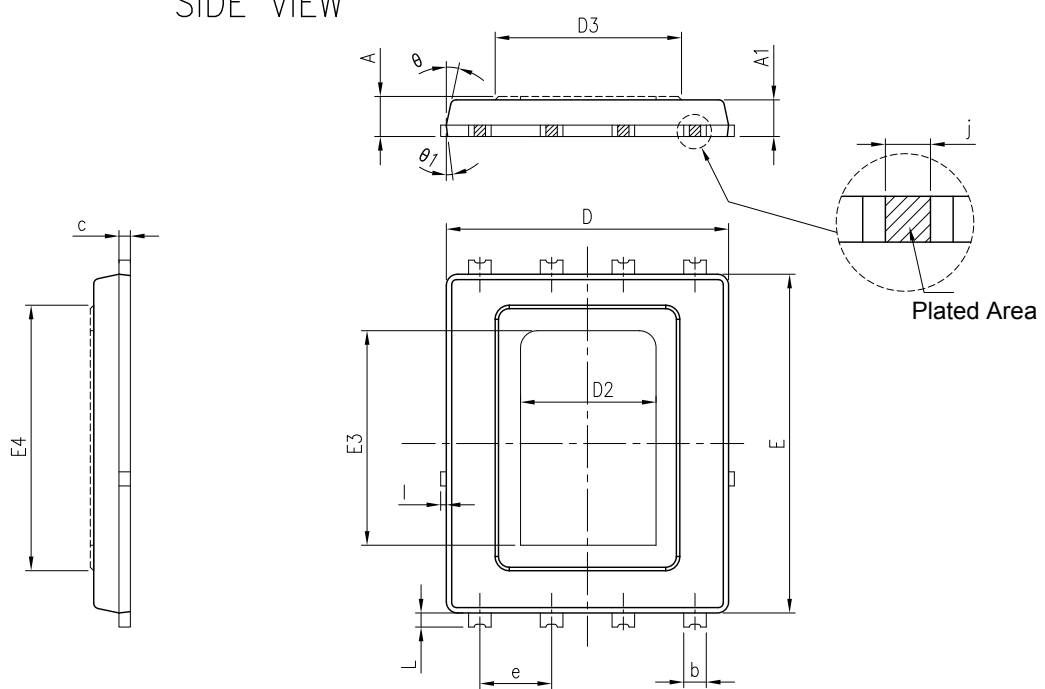
4.1 PowerFLAT™ 5x6 dual side cooling package information

Figure 18. PowerFLAT™ 5x6 dual side cooling package outline

BOTTOM VIEW



SIDE VIEW

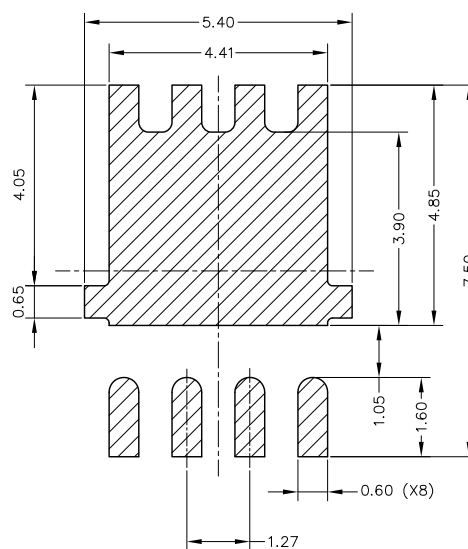


TOP VIEW

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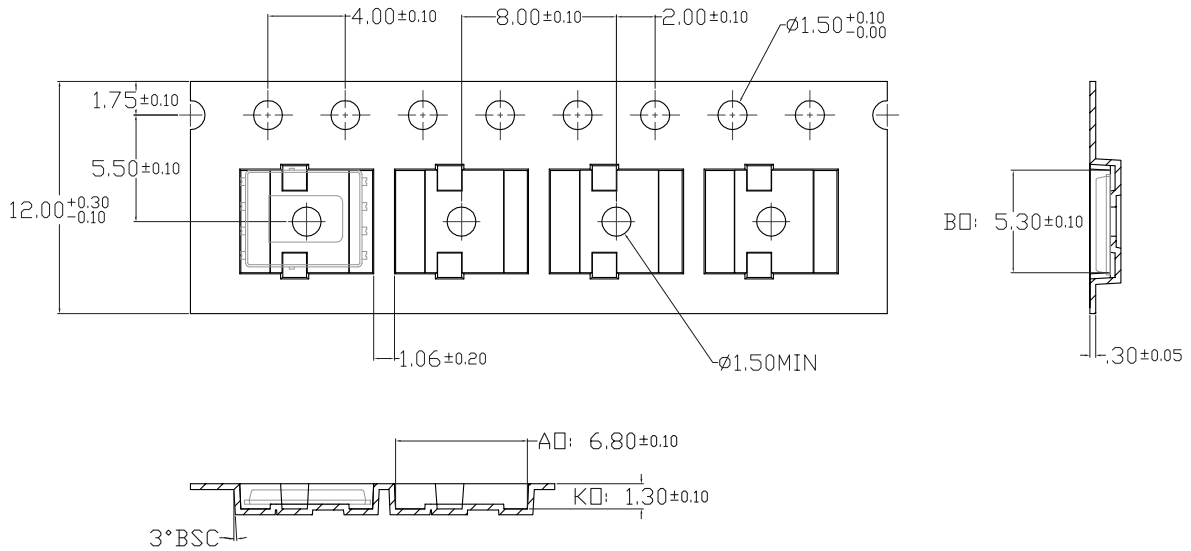
Table 8. PowerFLAT™ 5x6 dual side cooling mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.66	0.71	0.76
A1	0.60		0.75
b	0.33	0.43	0.53
c	0.15	0.203	0.30
D	5.00 BSC		
D1	4.06	4.21	4.36
D2	2.40 BSC		
D3	2.80	3.30	3.80
E	6.00 BSC		
E1	3.525	3.675	3.825
E2	1.05	1.20	1.35
E3	3.80 BSC		
E4	4.20	4.70	5.20
e	1.27 BSC		
l			0.15
L	0.15	0.25	0.35
L1	0.925	1.05	1.175
L2	0.45	0.575	0.70
ϑ	12° BSC		
ϑ1	7° BSC		
j	0.20 BSC		

Figure 19. PowerFLAT™ 5x6 dual side cooling recommended footprint (dimensions are in mm)


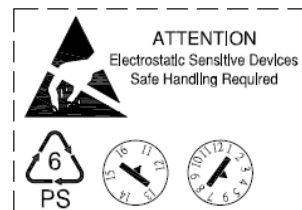
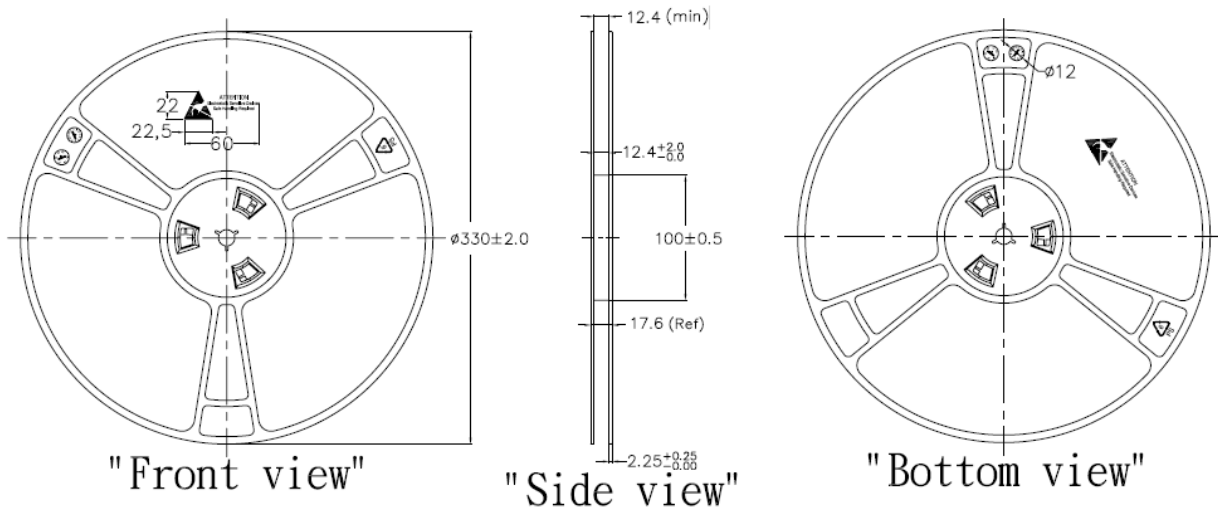
4.2 PowerFLAT™ 5x6 dual side cooling packing information

Figure 20. PowerFLAT™ 5x6 dual side cooling tape (dimensions are in mm)



8548087_REV1

Figure 21. PowerFLAT™ 5x6 dual side cooling reel (dimensions are in mm)



Revision history

Table 9. Document revision history

Date	Revision	Changes
02-May-2018	1	Initial release.
26-Jul-2018	2	Document status promoted from preliminary to production data. Updated <i>Table 4. On/off states</i> . Updated <i>Section 2.1 Electrical characteristics (curves)</i> . Minor text changes
6-Aug-2018	3	Updated <i>Table 5. Dynamic</i> . Updated <i>Section 2.1 Electrical characteristics (curves)</i> Minor text changes
21-Mar-2019	4	Modified <i>Table 4. On/off states</i> . Modified <i>Figure 1. Safe operating area</i> , <i>Figure 4. Transfer characteristics</i> , <i>Figure 6. Static drain-source on-resistance</i> and <i>Figure 9. Normalized on-resistance vs temperature</i> . Minor text changes.

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