



## N-Channel Logic Level Enhancement Mode Field Effect Transistor

PRODUCT SUMMARY		
V <sub>DSS</sub>	I <sub>D</sub>	R <sub>DS(ON)</sub> (mΩ) Max
100V	8A	19 @ V <sub>GS</sub> =10V
		27 @ V <sub>GS</sub> =4.5V

### FEATURES

- Super high dense cell design for low R<sub>DS(ON)</sub>.
- Rugged and reliable.
- Surface Mount Package.



### ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub>=25°C unless otherwise noted)

Symbol	Parameter	Limit	Units
V <sub>DS</sub>	Drain-Source Voltage	100	V
V <sub>GS</sub>	Gate-Source Voltage	±20	V
I <sub>D</sub>	Drain Current-Continuous <sup>c</sup>	T <sub>C</sub> =25°C	8
		T <sub>C</sub> =70°C	6.4
I <sub>DM</sub>	-Pulsed <sup>a c</sup>	40	A
E <sub>AS</sub>	Single Pulse Avalanche Energy <sup>d</sup>	272	mJ
P <sub>D</sub>	Maximum Power Dissipation	T <sub>C</sub> =25°C	2.5
		T <sub>C</sub> =70°C	1.6
T <sub>J</sub> , T <sub>STG</sub>	Operating Junction and Storage Temperature Range	-55 to 150	°C

### THERMAL CHARACTERISTICS

R <sub>θ JA</sub>	Thermal Resistance, Junction-to-Ambient	50	°C/W
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# STM132N

Ver 1.0

## ELECTRICAL CHARACTERISTICS (T<sub>A</sub>=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>OFF CHARACTERISTICS</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V , I <sub>D</sub> =250uA	100			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =80V , V <sub>GS</sub> =0V			1	uA
I <sub>GSS</sub>	Gate-Body Leakage Current	V <sub>GS</sub> = ±20V , V <sub>DS</sub> =0V			±100	nA
<b>ON CHARACTERISTICS</b>						
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250uA	1	2	3	V
R <sub>DS(ON)</sub>	Drain-Source On-State Resistance	V <sub>GS</sub> =10V , I <sub>D</sub> =4A		15	19	m ohm
		V <sub>GS</sub> =4.5V , I <sub>D</sub> =3A		20	27	m ohm
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> =10V , I <sub>D</sub> =4A		21		S
<b>DYNAMIC CHARACTERISTICS <sup>b</sup></b>						
C <sub>ISS</sub>	Input Capacitance	V <sub>DS</sub> =25V, V <sub>GS</sub> =0V f=1.0MHz		1823		pF
C <sub>OSS</sub>	Output Capacitance			224		pF
C <sub>RSS</sub>	Reverse Transfer Capacitance			106		pF
<b>SWITCHING CHARACTERISTICS <sup>b</sup></b>						
t <sub>D(ON)</sub>	Turn-On Delay Time	V <sub>DD</sub> =50V I <sub>D</sub> =1A V <sub>GS</sub> =10V R <sub>GEN</sub> = 6 ohm		38		ns
t <sub>r</sub>	Rise Time			39		ns
t <sub>D(OFF)</sub>	Turn-Off Delay Time			47		ns
t <sub>f</sub>	Fall Time			23		ns
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> =50V, I <sub>D</sub> =4A, V <sub>GS</sub> =10V		21		nC
		V <sub>DS</sub> =50V, I <sub>D</sub> =4A, V <sub>GS</sub> =4.5V		11		nC
Q <sub>gs</sub>	Gate-Source Charge	V <sub>DS</sub> =50V, I <sub>D</sub> =4A,		3		nC
Q <sub>gd</sub>	Gate-Drain Charge	V <sub>GS</sub> =10V		6.6		nC
<b>DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS</b>						
V <sub>SD</sub>	Diode Forward Voltage	V <sub>GS</sub> =0V, I <sub>S</sub> =5A		0.73	1.3	V

### Notes

- a. Pulse Test: Pulse Width ≤ 10us, Duty Cycle ≤ 1%.
- b. Guaranteed by design, not subject to production testing.
- c. Drain current limited by maximum junction temperature.
- d. Starting T<sub>J</sub>=25°C, L=0.5mH, V<sub>DD</sub> = 50V. (See Figure 13)
- e. Mounted on FR4 Board of 1 inch<sup>2</sup> , 2oz.

Feb,09,2015

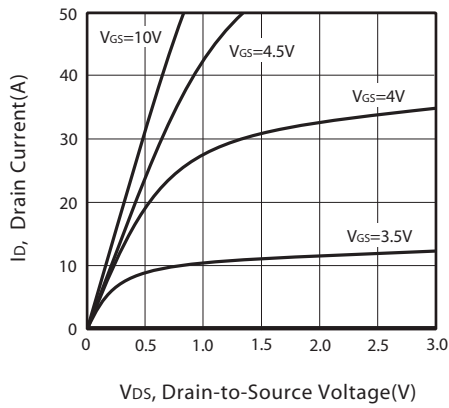


Figure 1. Output Characteristics

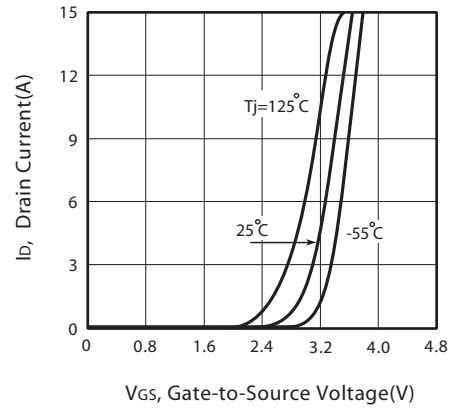


Figure 2. Transfer Characteristics

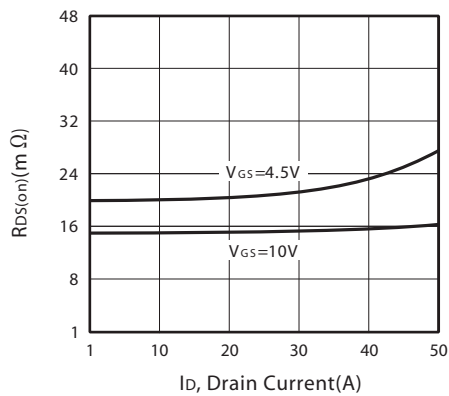


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

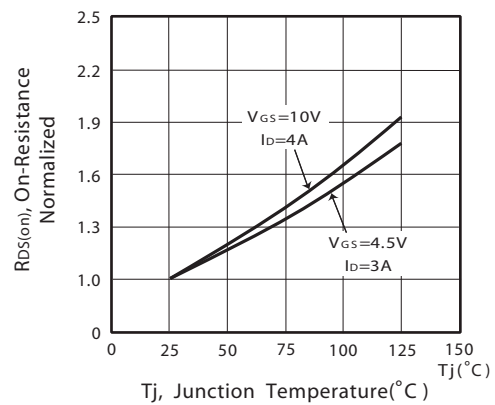


Figure 4. On-Resistance Variation with Drain Current and Temperature

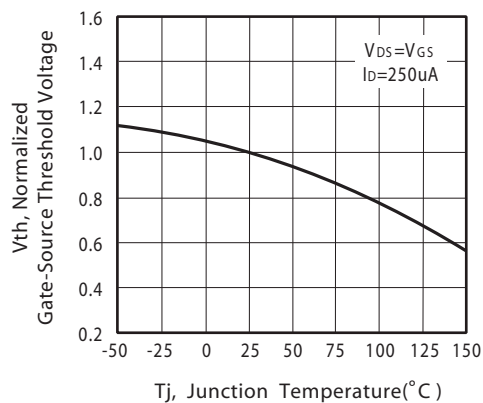


Figure 5. Gate Threshold Variation with Temperature

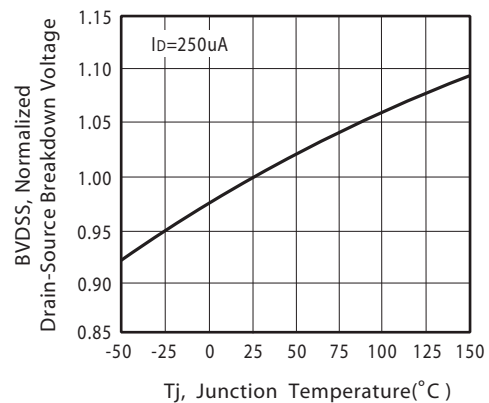


Figure 6. Breakdown Voltage Variation with Temperature

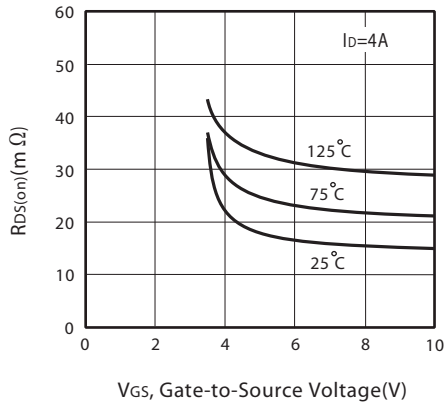


Figure 7. On-Resistance vs. Gate-Source Voltage

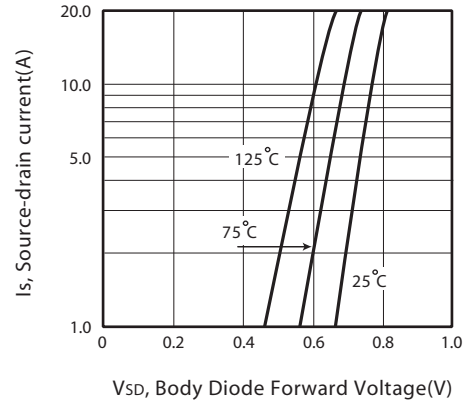


Figure 8. Body Diode Forward Voltage Variation with Source Current

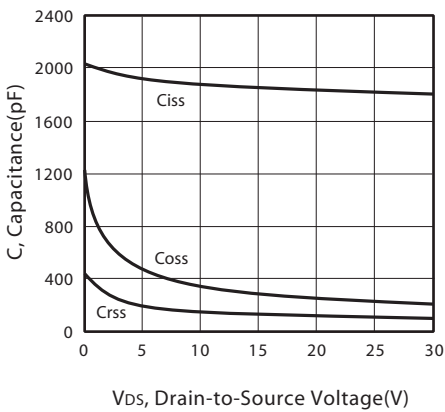


Figure 9. Capacitance

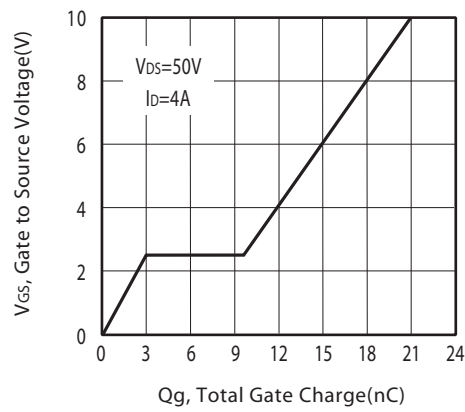


Figure 10. Gate Charge

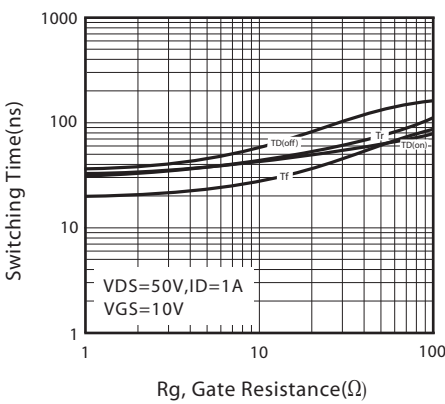


Figure 11. switching characteristics

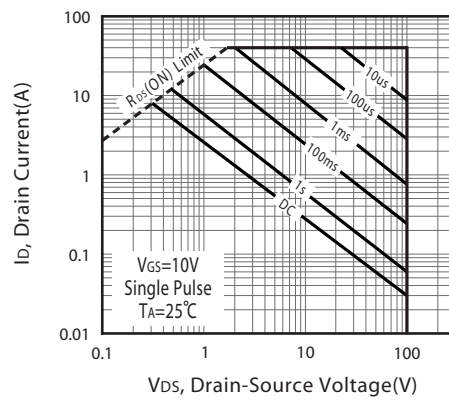
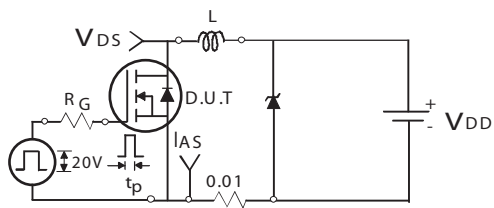
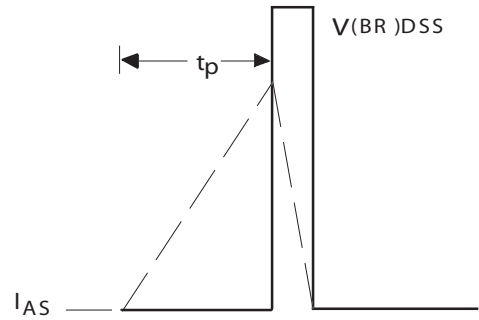


Figure 12. Maximum Safe Operating Area



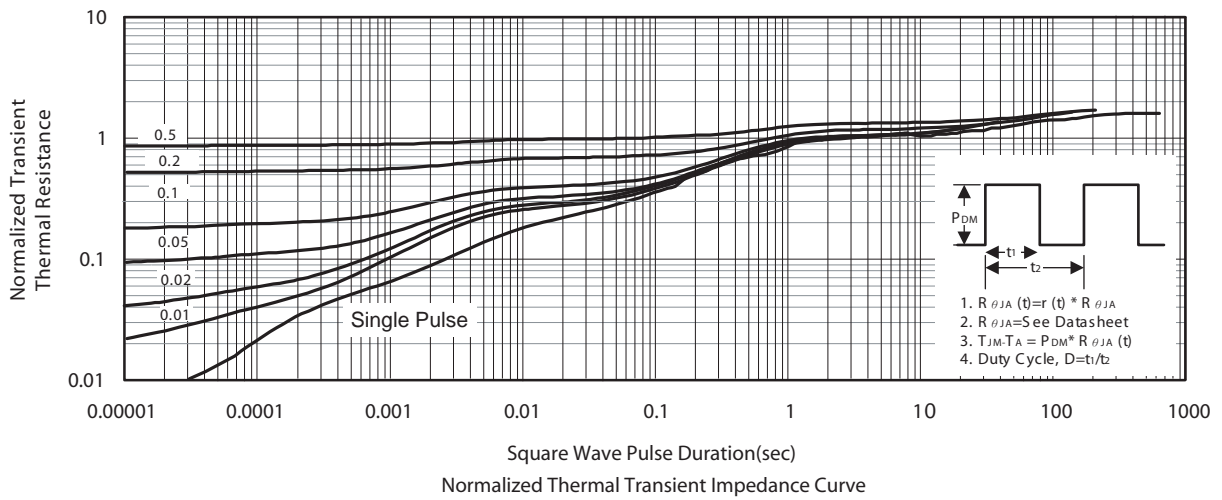
Unclamped Inductive Test Circuit

Figure 13a.



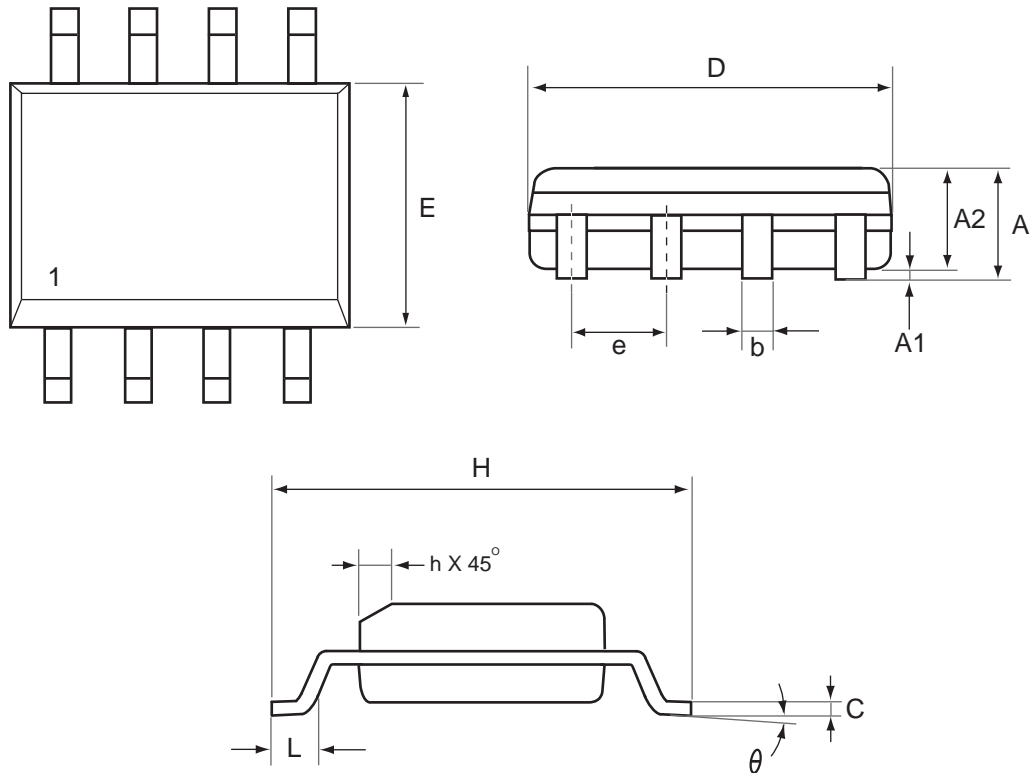
Unclamped Inductive Waveforms

Figure 13b.



## PACKAGE OUTLINE DIMENSIONS

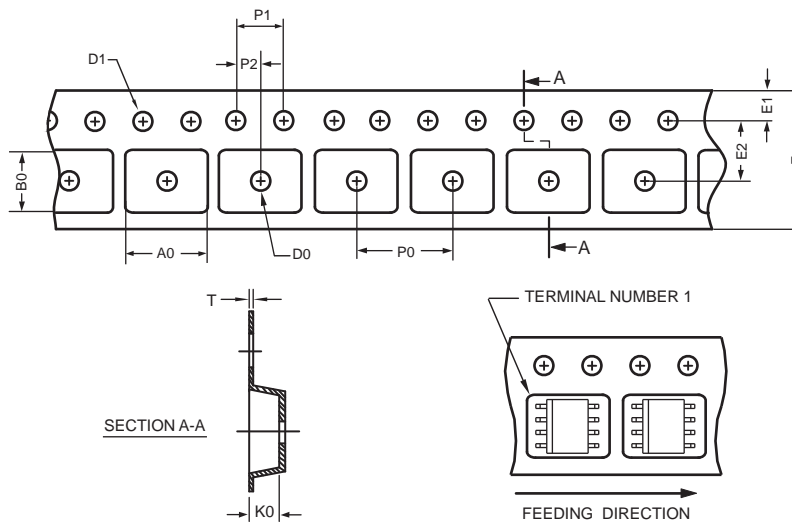
### SO-8



SYMBOLS	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
A2	1.25	1.63	0.049	0.064
b	0.31	0.51	0.012	0.020
C	0.17	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
E	3.70	4.00	0.146	0.157
e	1.27 REF.		0.050 BSC	
H	5.80	6.20	0.228	0.244
L	0.40	1.27	0.016	0.050
theta	0°	8°	0°	8°
h	0.25	0.50	0.010	0.020

## SO-8 Tape and Reel Data

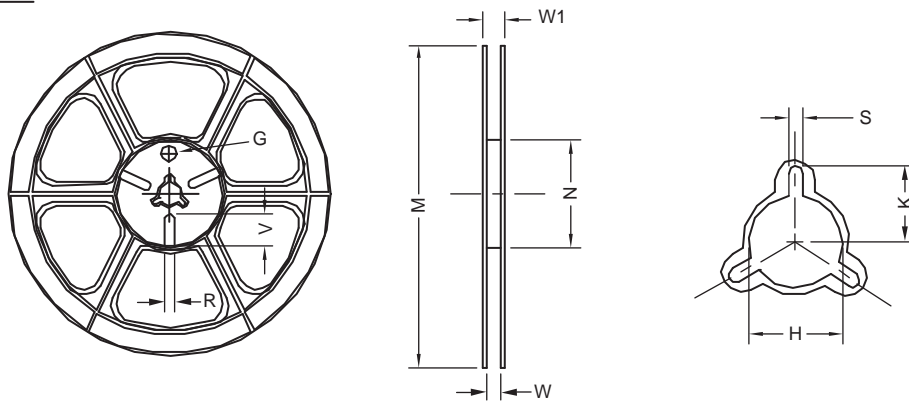
### SO-8 Carrier Tape



unit:mm

PACKAGE	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
SOP 8N 150mil	6.50 ±0.15	5.25 ±0.10	2.10 ±0.10	φ 1.5 (MIN)	φ 1.55 ±0.10	12.0 +0.3 -0.1	1.75 ±0.10	5.5 ±0.10	8.0 ±0.10	4.0 ±0.10	2.0 ±0.10	0.30 ±0.013

### SO-8 Reel



UNIT:mm

TAPE SIZE	REEL SIZE	M	N	W	W1	H	K	S	G	R	V
12 mm	φ 330	330 ± 1	62 ±1.5	12.4 + 0.2	16.8 - 0.4	φ 12.75 + 0.15	---	2.0 ±0.15	---	---	---

## TOP MARKING DEFINITION

