

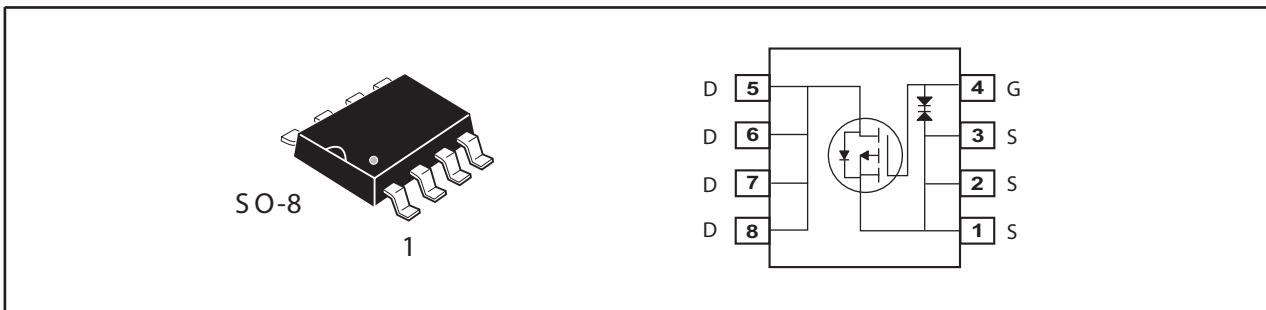


## P-Channel Enhancement Mode Field Effect Transistor

PRODUCT SUMMARY		
V <sub>DS</sub>	I <sub>D</sub>	R <sub>DS(ON)</sub> (mΩ) Max
-30V	-7.0A	33 @ V <sub>GS</sub> =-10V
		52 @ V <sub>GS</sub> =-4.5V

### FEATURES

- Super high dense cell design for low R<sub>DS(ON)</sub>.
- Rugged and reliable.
- Surface Mount Package.
- ESD Protected.



### ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub>=25°C unless otherwise noted)

Symbol	Parameter	Limit	Units
V <sub>DS</sub>	Drain-Source Voltage	-30	V
V <sub>GS</sub>	Gate-Source Voltage	±20	V
I <sub>D</sub>	Drain Current-Continuous <sup>a</sup>	T <sub>A</sub> =25°C	-7
		T <sub>A</sub> =70°C	-5.6
I <sub>DM</sub>	-Pulsed <sup>b</sup>	-40	A
E <sub>AS</sub>	Single Pulse Avalanche Energy <sup>d</sup>	20	mJ
P <sub>D</sub>	Maximum Power Dissipation <sup>a</sup>	T <sub>A</sub> =25°C	2.5
		T <sub>A</sub> =70°C	1.6
T <sub>J</sub> , T <sub>STG</sub>	Operating Junction and Storage Temperature Range	-55 to 150	°C

### THERMAL CHARACTERISTICS

R <sub>θJA</sub>	Thermal Resistance, Junction-to-Ambient <sup>a</sup>	50	°C/W
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# STM4633

Ver 1.0

## ELECTRICAL CHARACTERISTICS (TA=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>OFF CHARACTERISTICS</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V , I <sub>D</sub> =-250uA	-30			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =-24V , V <sub>GS</sub> =0V			-1	uA
I <sub>GSS</sub>	Gate-Body Leakage Current	V <sub>GS</sub> = ±20V , V <sub>DS</sub> =0V			±10	uA
<b>ON CHARACTERISTICS</b>						
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =-250uA	-1	-1.7	-3	V
R <sub>DS(ON)</sub>	Drain-Source On-State Resistance	V <sub>GS</sub> =-10V , I <sub>D</sub> =-7A		26	33	m ohm
		V <sub>GS</sub> =-4.5V , I <sub>D</sub> =-5.6A		39	52	m ohm
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> =-15V , I <sub>D</sub> =-7A		9.5		S
<b>DYNAMIC CHARACTERISTICS <sup>c</sup></b>						
C <sub>ISS</sub>	Input Capacitance	V <sub>DS</sub> =-15V, V <sub>GS</sub> =0V f=1.0MHz		811		pF
C <sub>OSS</sub>	Output Capacitance			215		pF
C <sub>RSS</sub>	Reverse Transfer Capacitance			125		pF
<b>SWITCHING CHARACTERISTICS <sup>c</sup></b>						
t <sub>D(ON)</sub>	Turn-On Delay Time	V <sub>DD</sub> =-15V I <sub>D</sub> =-1A V <sub>GS</sub> =-10V R <sub>GEN</sub> =6 ohm		12.5		ns
t <sub>r</sub>	Rise Time			18		ns
t <sub>D(OFF)</sub>	Turn-Off Delay Time			60		ns
t <sub>f</sub>	Fall Time			10.4		ns
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> =-15V, I <sub>D</sub> =-7A, V <sub>GS</sub> =-10V		15		nC
		V <sub>DS</sub> =-15V, I <sub>D</sub> =-7A, V <sub>GS</sub> =-4.5V		7.4		nC
Q <sub>gs</sub>	Gate-Source Charge	V <sub>DS</sub> =-15V, I <sub>D</sub> =-7A, V <sub>GS</sub> =-10V		1.65		nC
Q <sub>gd</sub>	Gate-Drain Charge			4.2		nC
<b>DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS</b>						
I <sub>S</sub>	Maximum Continuous Drain-Source Diode Forward Current				-1.7	A
V <sub>SD</sub>	Diode Forward Voltage <sup>b</sup>	V <sub>GS</sub> =0V, I <sub>S</sub> =-1.7A		-0.77	-1.3	V
<b>Notes</b> a. Surface Mounted on FR4 Board, t ≤ 10sec. b. Pulse Test: Pulse Width ≤ 300us, Duty Cycle ≤ 2%. c. Guaranteed by design, not subject to production testing. d. Starting T <sub>J</sub> =25°C, L=0.5mH, V <sub>DD</sub> = 20V. (See Figure13)						

Aug, 13, 2008

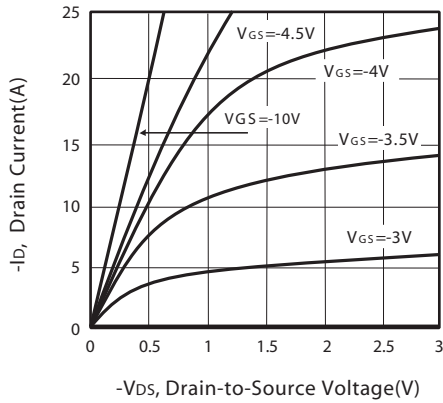


Figure 1. Output Characteristics

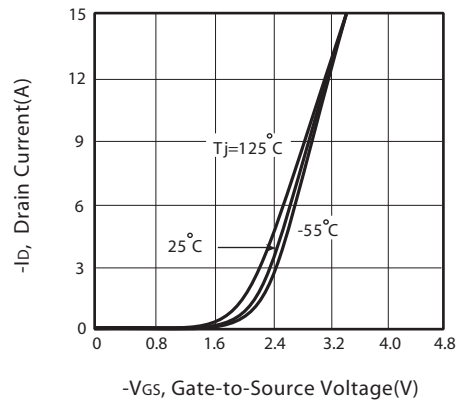


Figure 2. Transfer Characteristics

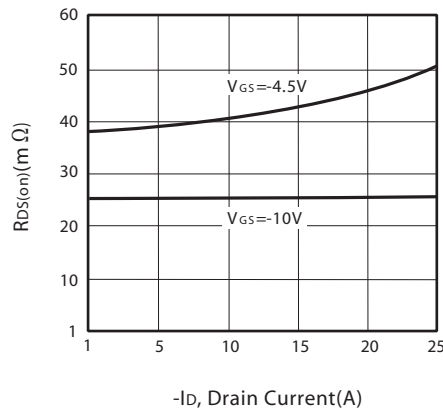


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

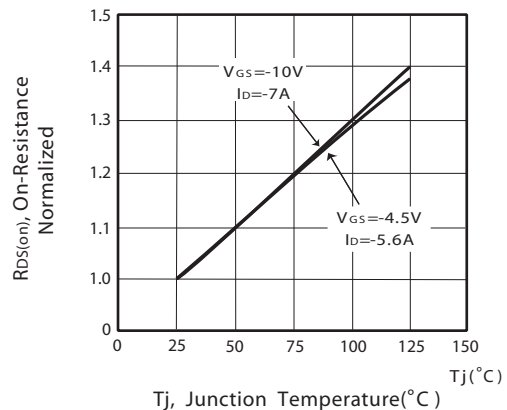


Figure 4. On-Resistance Variation with Drain Current and Temperature

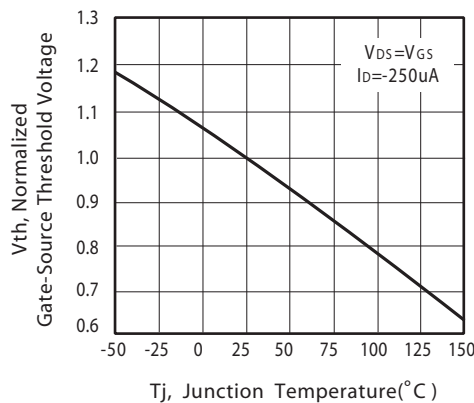


Figure 5. Gate Threshold Variation with Temperature

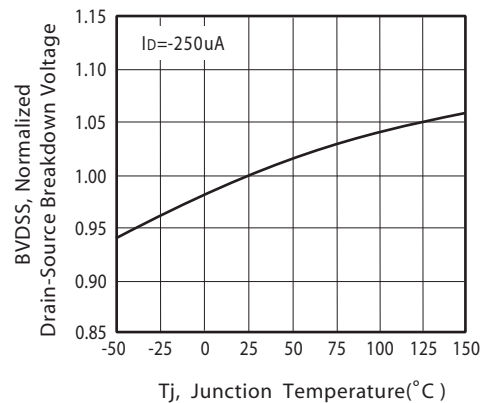


Figure 6. Breakdown Voltage Variation with Temperature

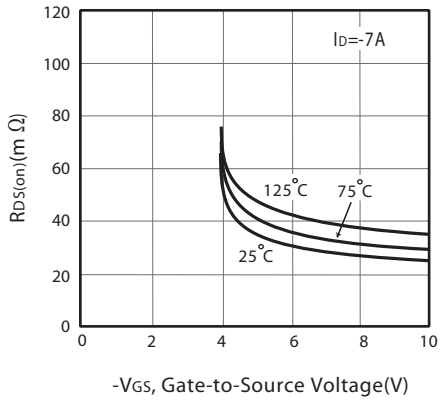


Figure 7. On-Resistance vs. Gate-Source Voltage

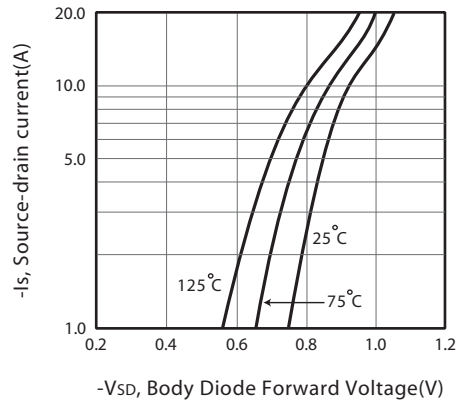


Figure 8. Body Diode Forward Voltage Variation with Source Current

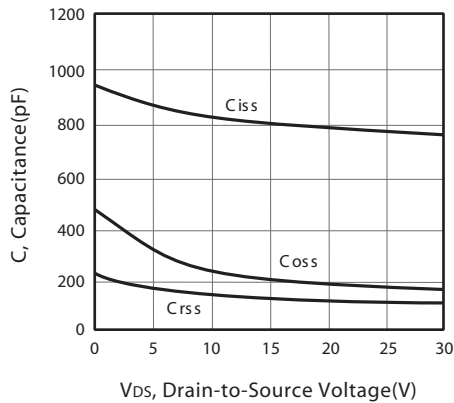


Figure 9. Capacitance

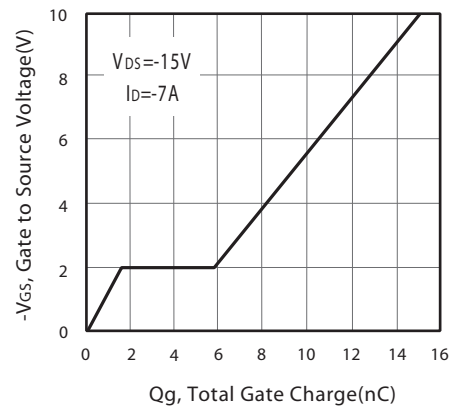


Figure 10. Gate Charge

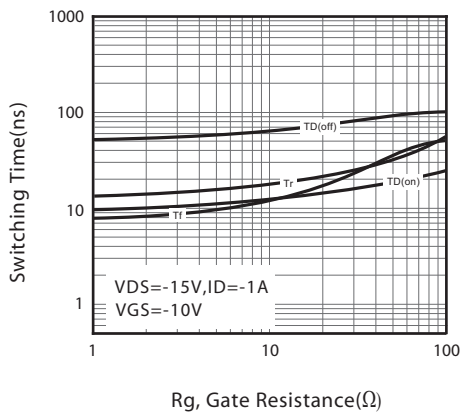


Figure 11. switching characteristics

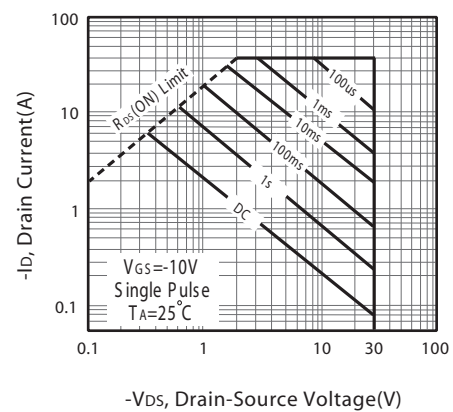
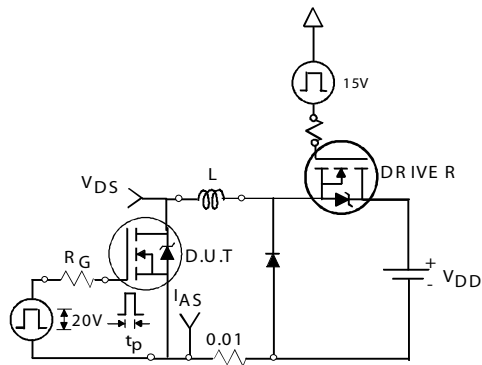
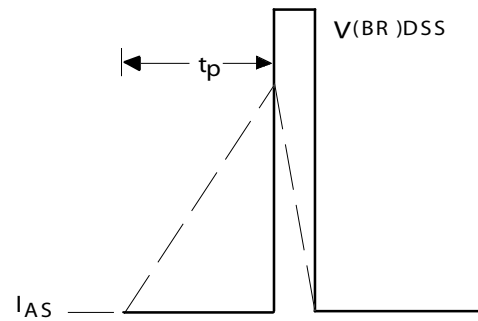


Figure 12. Maximum Safe Operating Area



Unclamped Inductive Test Circuit

Figure 13a.



Unclamped Inductive Waveforms

Figure 13b.

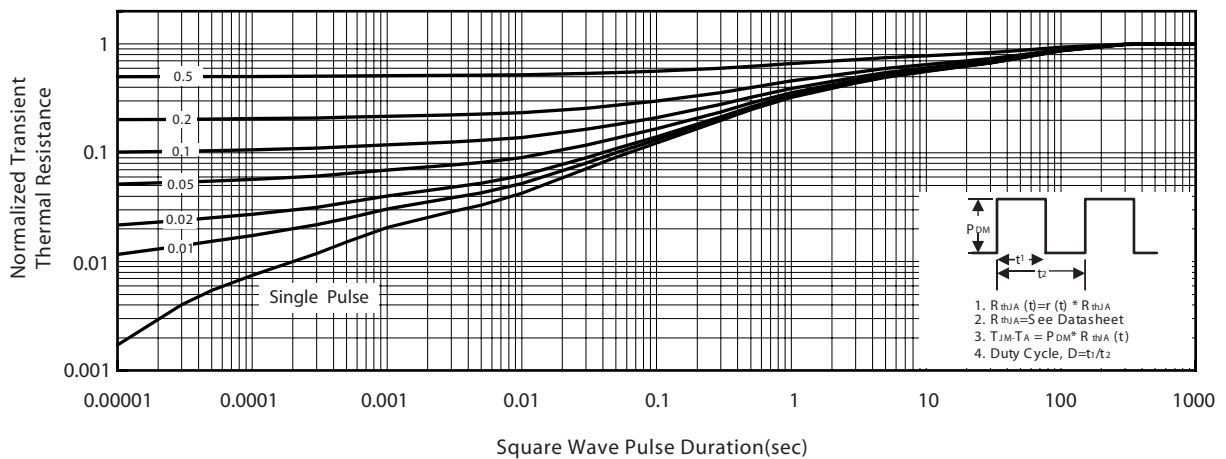
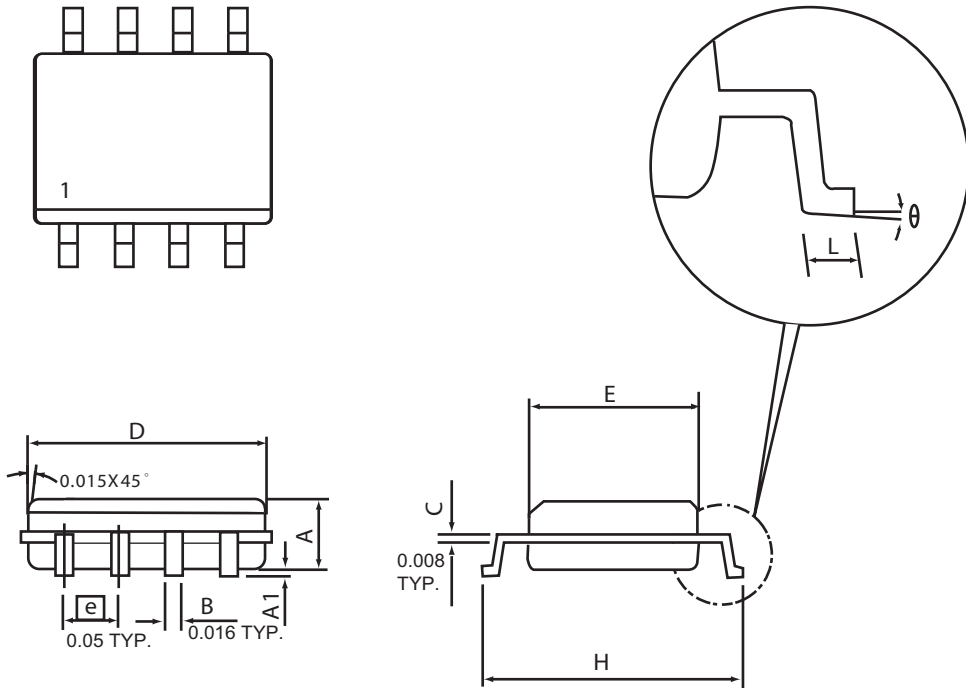


Figure 14. Normalized Thermal Transient Impedance Curve

## PACKAGE OUTLINE DIMENSIONS

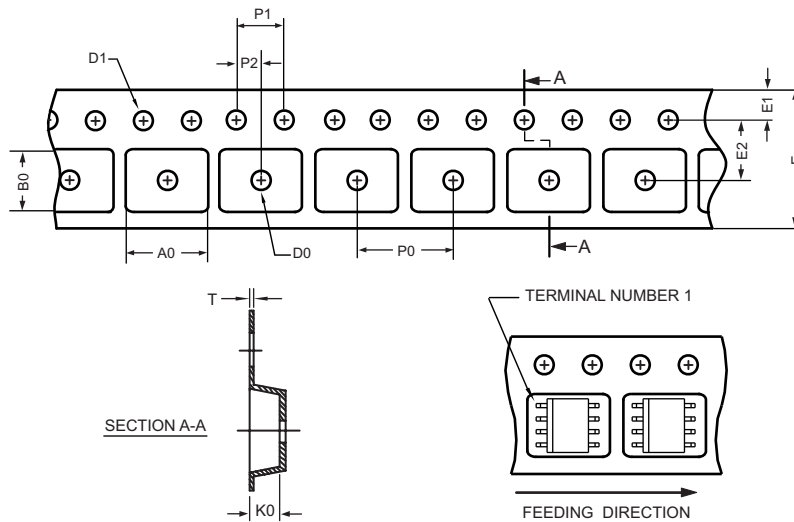
SO-8



SYMBOLS	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
D	4.80	4.98	0.189	0.196
E	3.81	3.99	0.150	0.157
H	5.79	6.20	0.228	0.244
L	0.41	1.27	0.016	0.050
$\theta$	0°	8°	0°	8°

## SO-8 Tape and Reel Data

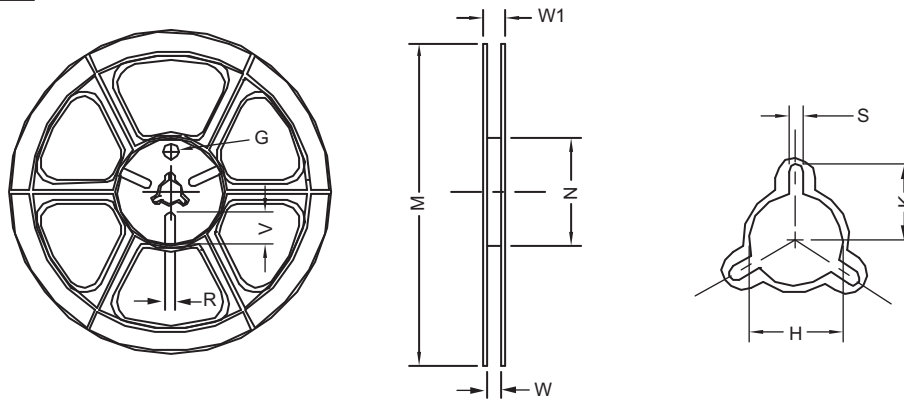
### SO-8 Carrier Tape



unit: mm

PACKAGE	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
SOP 8N 150mil	6.50 ±0.15	5.25 ±0.10	2.10 ±0.10	φ 1.5 (MIN)	φ 1.55 ±0.10	12.0 +0.3 -0.1	1.75 ±0.10	5.5 ±0.10	8.0 ±0.10	4.0 ±0.10	2.0 ±0.10	0.30 ±0.013

### SO-8 Reel



UNIT: mm

TAPE SIZE	REEL SIZE	M	N	W	W1	H	K	S	G	R	V
12 mm	φ 330	330 ± 1	62 ±1.5	12.4 + 0.2	16.8 - 0.4	φ 12.75 + 0.15	---	2.0 ±0.15	---	---	---