

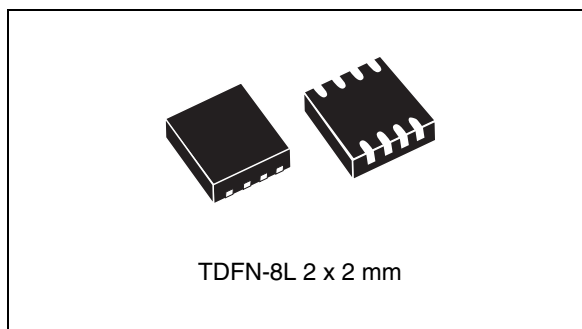


# STM6502, STM6503 STM6504, STM6505

## Dual push-button smart reset

### Features

- Operating voltage 1.0 V (active-low output valid) to 5.5 V
- Low supply current
- Factory-programmable thresholds to monitor  $V_{CC}$  in the range of 1.575 to 4.625 V typ.
- Open-drain, active-low reset output
- Dual smart reset push-button inputs with extended reset set up delay
- Adjustable smart reset setup delay ( $t_{SRC}$ ): by external capacitor or external resistor or three-state logic
- Power-on reset
- Operating temperature: industrial grade  $-40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$
- Package: TDFN-8L 2 x 2 x 0.75 mm, 0.5 mm pitch
- RoHS compliant



### Applications

- MP3 players
- Portable navigation devices
- Mobile phones

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**Table 1. Device summary**

Part number	Voltage inputs		Smart reset inputs			$t_{SRC}$ programming		Reset or Power Good outputs		Package
	$V_{CC}$	$V_{BAT}$	$\overline{SR}$ or $\overline{SR0}$	$\overline{SR1}$	SRE immediate, independent	Ext. SRC pin	Three-state input TSR	$\overline{RST}$	$\overline{BLD}$	
STM6502 <sup>(1)</sup>	✓		✓	✓		✓		✓		TDFN-8L
STM6503	✓		✓	✓			✓	✓		TDFN-8L
STM6504	✓		✓		✓		✓	✓		TDFN-8L
STM6505	✓	✓	✓	✓		✓		✓	✓	TDFN-8L

1. Contact local ST sales office for availability.

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# 1 Description

The smart reset devices provide a useful feature that ensures that inadvertent short reset push-button closures do not cause system resets as the extended smart reset delay setup periods are implemented. Hence, when valid smart reset input conditions and setup periods are met, the  $\overline{\text{RST}}$  output will generate a pulse which asserts the reset output for fixed timeout period ( $t_{\text{REC}}$ ).

The typical application hookup shows that either the single smart reset input or the dual reset inputs are also connected to the applications interrupt and control both the interrupt pin and the hard reset functions. If the push-button is closed for a short time, the processor is only interrupted. If the system still does not respond properly, holding the push-button(s) and keeping it closed for the extended setup time ( $t_{\text{SRC}}$ ) causes a hard reset of the processor. The smart reset feature helps significantly increase system stability and eliminates the need for a dedicated reset button.

The STM65xx family of smart reset devices consists of low current microprocessor reset circuits targeted for MP3 players, portable navigation, mobile phones and other portable devices. The STM65xx devices feature single or dual smart reset inputs (SRx). The delayed smart reset setup time ( $t_{\text{SRC}}$ ) options of 0 s, 2 s, 6 s and 10 s (all min.) are adjustable by an external capacitor or resistor on the SRC pin or selectable by three-state logic, see [Table 1](#). The delayed setup period ignores short switch closures shorter than  $t_{\text{SRC}}$ , thus preventing unwanted resets.

The STM65xx devices have active-low open-drain reset ( $\overline{\text{RST}}$ ) output with power-on reset function.

The reset output is also asserted when the monitored supply voltage  $V_{\text{CC}}$  drops below the specified threshold. The reset output remains asserted for the reset timeout period ( $t_{\text{REC}}$ ) after the monitored supply voltage goes above the specified threshold.

**STM6502** has two combined smart reset inputs ( $\overline{\text{SR0}}$  and  $\overline{\text{SR1}}$ ) with delayed smart reset setup time ( $t_{\text{SRC}}$ ) programmed by either an external capacitor or resistor on the SRC pin (device options).

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**STM6503** is similar to STM6502, has two combined delayed smart reset inputs ( $\overline{\text{SR0}}$ ,  $\overline{\text{SR1}}$ ) and three user-selectable delayed smart reset setup time ( $t_{\text{SRC}}$ ) options of 2 s, 6 s and 10 s through a three-state TSR input pin: when connected to ground,  $t_{\text{SRC}} = 2$  s; when left open,  $t_{\text{SRC}} = 6$  s; when connected to  $V_{\text{CC}}$ ,  $t_{\text{SRC}} = 10$  s (all the times are minimum).

**STM6504** has two independent smart reset inputs:  $\overline{\text{SR0}}$  provides the delayed smart reset setup time ( $t_{\text{SRC}}$ ) function with three user-selectable  $t_{\text{SRC}}$  options through a three-state TSR input pin: when connected to ground,  $t_{\text{SRC}} = 2$  s; when left open,  $t_{\text{SRC}} = 6$  s; when connected to  $V_{\text{CC}}$ ,  $t_{\text{SRC}} = 10$  s (all the times are minimum), SRE provides instant reset. SRE is edge trigger with a special debounce time ( $t_{\text{DEBOUNCE}} = 240$  ms min.) at the falling edge after a valid reset period.

**STM6505** has two combined delayed smart reset inputs ( $\overline{\text{SR0}}$ ,  $\overline{\text{SR1}}$ ) and provides adjustable reset delay setup time via either an external capacitor or resistor connected to the SRC pin. The  $\overline{\text{RST}}$  output depends also on the  $V_{\text{CC}}$  threshold. STM6505 also provides independent low battery detect ( $\overline{\text{BLD}}$ ) output controlled by the secondary external input voltage  $V_{\text{BAT}}$ . The  $V_{\text{BAT}}$  is monitored for low voltage and provides an indication on the battery low detect output pin ( $\overline{\text{BLD}}$ ).  $V_{\text{BAT}}$  threshold is 1.25 V, fixed, external resistor divider to be used to set the actual battery voltage threshold.  $V_{\text{BAT}}$  threshold hysteresis is 8 mV typ.

## Description

## STM6502, STM6503, STM6504, STM6505

(16 mV max.).  $V_{BAT}$  is voltage monitoring input only, the device is powered only from the  $V_{CC}$  pin;  $V_{CC}$  must be  $\geq 1.575$  V for proper operation of the  $V_{BAT}$  comparator.

For the whole STM65xx smart reset family, the reset outputs are also asserted when the monitored supply voltage  $V_{CC}$  drops below the specified threshold. The reset output remains asserted for the reset timeout period ( $t_{REC}$ ) after the monitored supply voltage goes above the specified threshold.

**Figure 1. Logic diagrams**

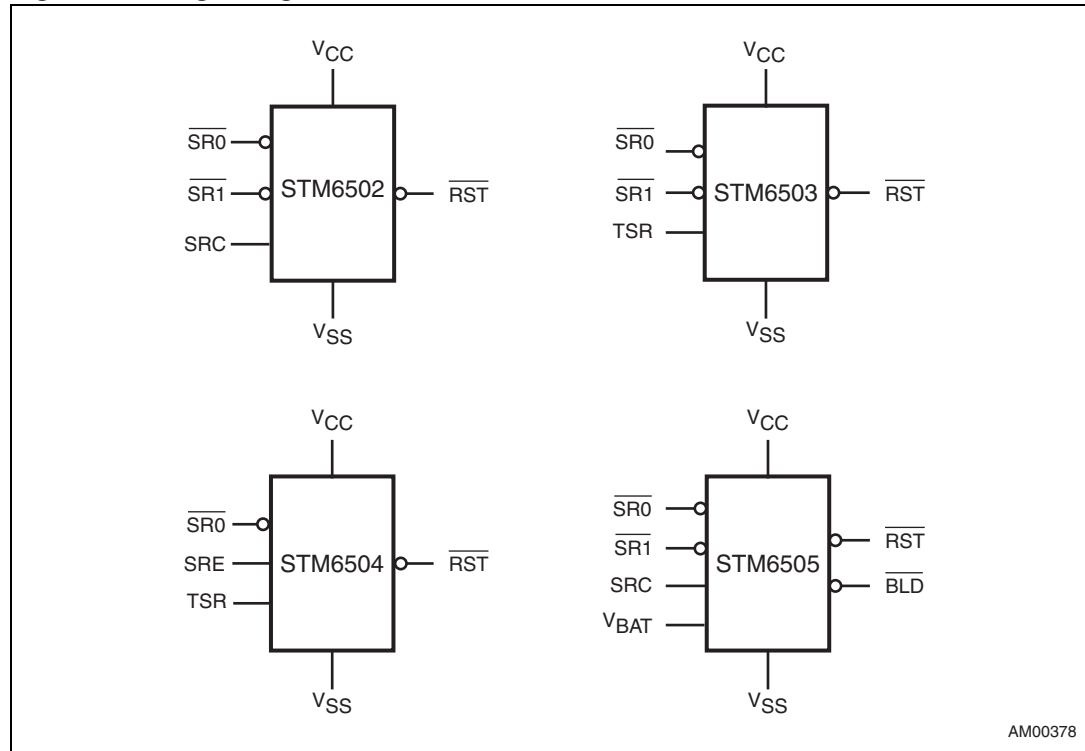
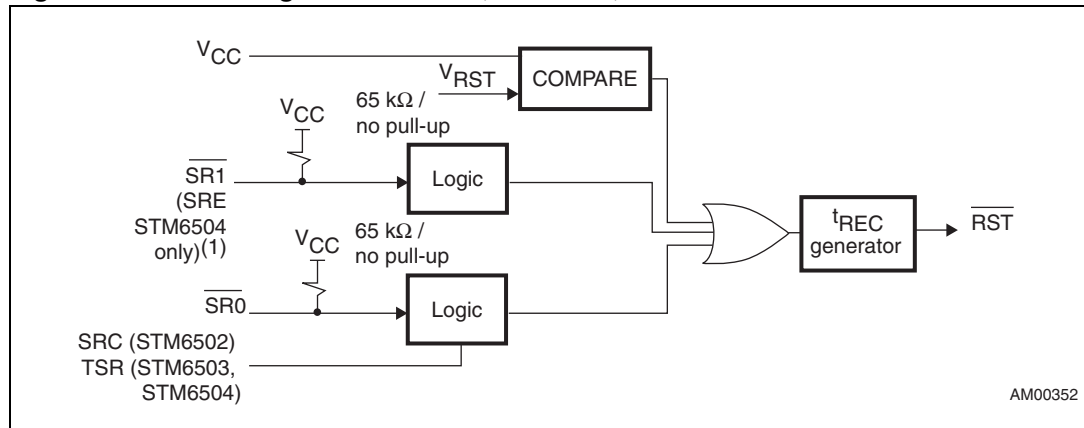


Figure 2. Block diagram - STM6502, STM6503, STM6504<sup>(1)</sup>



1. STM6504 only:  $\overline{SR0}$  and SRE are working independently: SRE is edge trigger, it has a special debounce time ( $t_{DEBOUNCE} = 240 \text{ ms min.}$ ) at the falling edge after a valid reset period.

Figure 3. Block diagram - STM6505

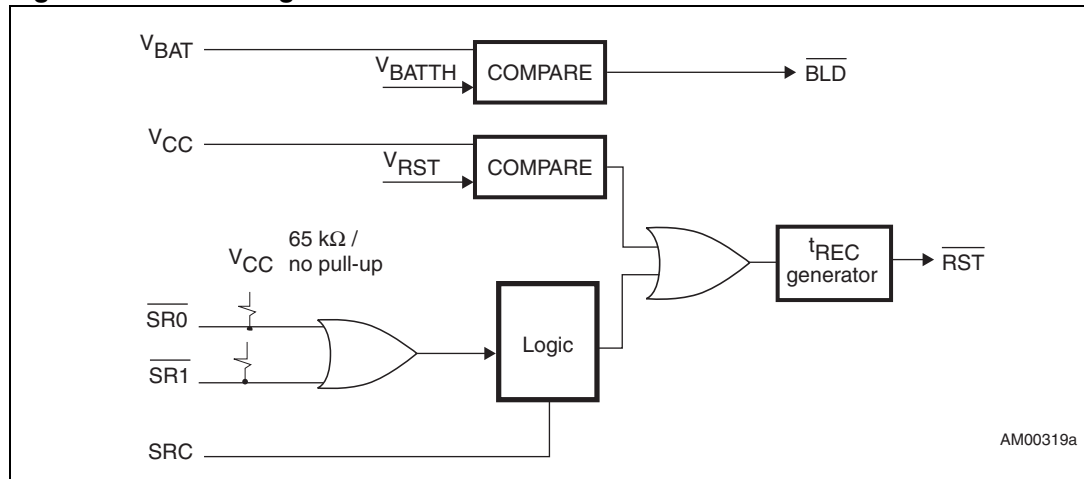


Figure 4. Single-button smart reset typical hookup

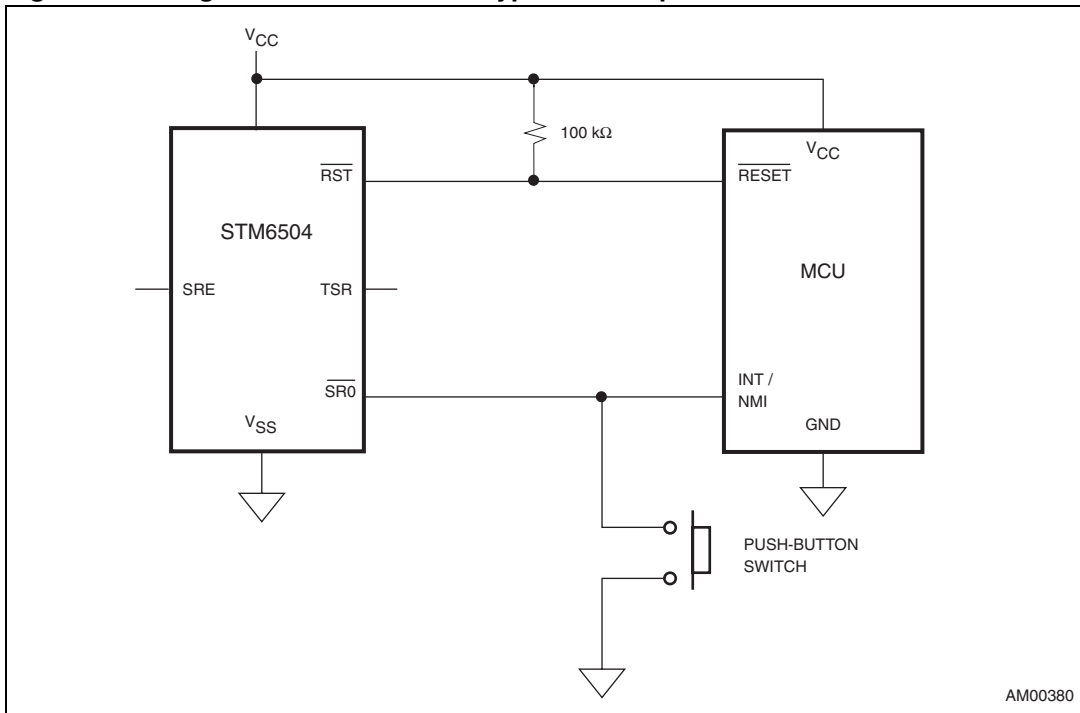
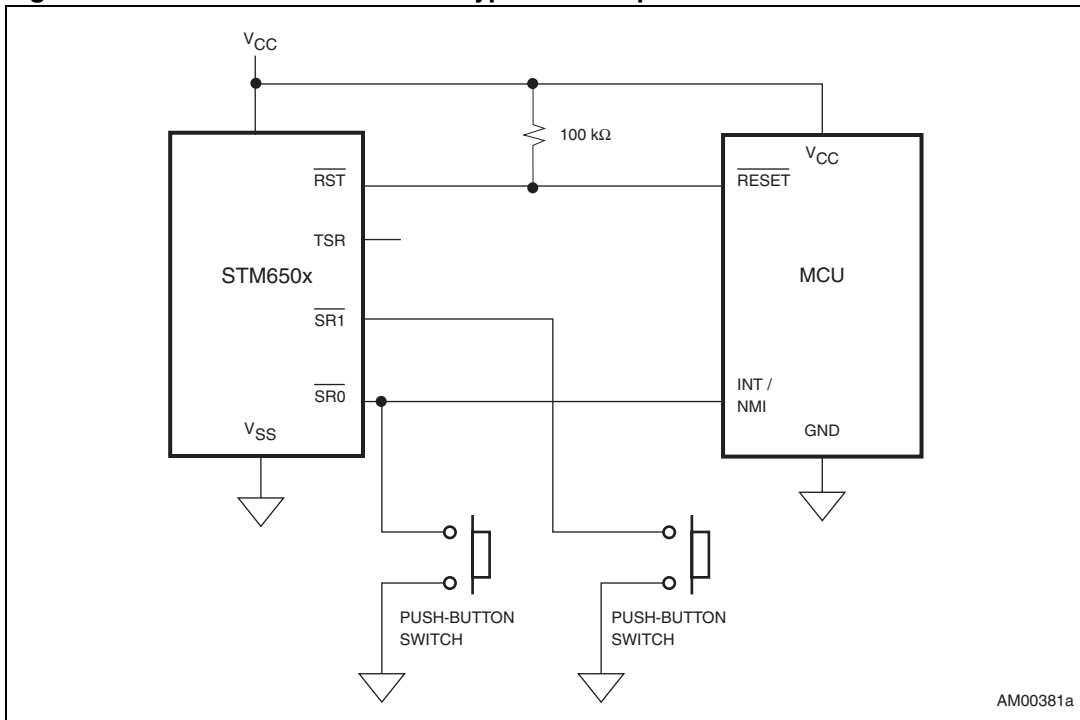


Figure 5. Dual-button smart reset typical hookup



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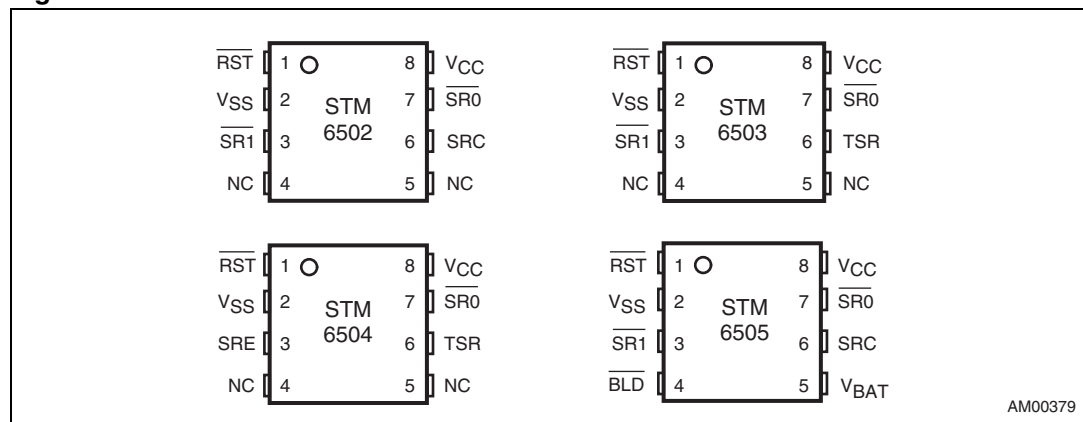
## 2 Signal names

**Table 2. Signal names**

Symbol	Input/output	Description
$\overline{\text{RST}}$	Output	Open-drain reset output, active-low.
$\overline{\text{BLD}}$	Output	Battery low detect output, active-low, open-drain. STM6505 only.
$\overline{\text{SR0}}$	Input	Primary push-button smart reset input. Active-low, internal pull-up to $V_{\text{CC}}$ (65 k $\Omega$ ), optionally without pull-up.
$\overline{\text{SR1}}$	Input	Secondary push-button smart reset input - combines with the primary push-button reset to provide set up delay time before reset. Active-low, has internal pull-up to $V_{\text{CC}}$ (65 k $\Omega$ ), optionally without pull-up.
SRE	Input	Secondary push-button smart reset input - provides instant smart reset. SRE is edge trigger with a special debounce time ( $t_{\text{DEBOUNCE}} = 240 \text{ ms min.}$ ) at the falling edge after a valid reset period. Active-high, no internal pull-up to $V_{\text{CC}}$ . STM6504 only.
SRC	Input	Smart reset input delay setup control: connect to either an external capacitor or resistor to adjust the delay setup time ( $t_{\text{SRC}}$ )
TSR	Input	A three-state smart reset input delay setup control. When connected to ground, $t_{\text{SRC}} = 2 \text{ s}$ ; when left open, $t_{\text{SRC}} = 6 \text{ s}$ ; when connected to $V_{\text{CC}}$ , $t_{\text{SRC}} = 10 \text{ s}$ (all times are minimum). TSR is a DC-type input, intended to be either permanently grounded or permanently connected to $V_{\text{CC}}$ . STM6503 and STM6504 only.
$V_{\text{CC}}$	Supply voltage	Supply voltage input. Power supply for device and an input for the monitored supply voltage.
$V_{\text{BAT}}$	Battery monitoring input	Battery voltage monitoring input. STM6505 only.
$V_{\text{SS}}$	Supply ground	Ground
NC		No connect

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**Figure 6. Pin connections**



### 3 Pin descriptions

#### 3.1 Power supply ( $V_{CC}$ )

This pin is used to provide the power to the device and to monitor the power supply.

#### 3.2 Ground ( $V_{SS}$ )

This is the power ground for the device and all supplies.

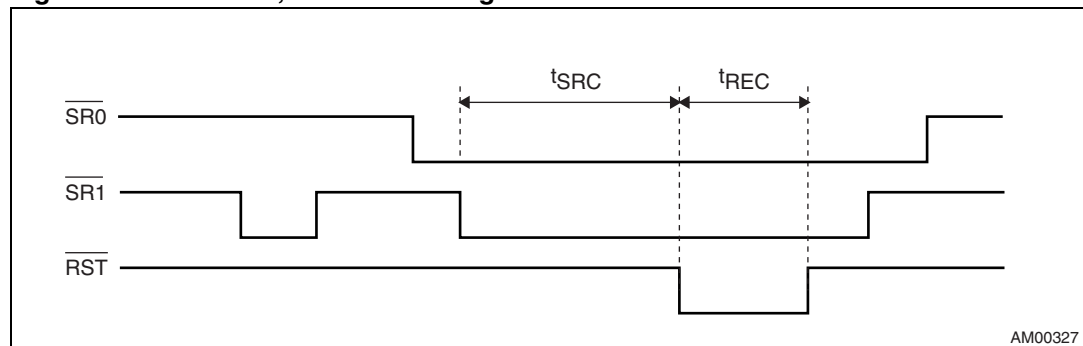
#### 3.3 Smart reset input ( $\overline{SR0}$ )

The primary push-button smart reset input, active-low pin is connected to the push-button switch.

#### 3.4 Secondary smart reset input ( $\overline{SR1}$ )

The secondary push-button smart reset input, active-low pin is connected to the second push-button switch. Keeping both smart reset inputs  $\overline{SR0}$  and  $\overline{SR1}$  active for longer than  $t_{SRC}$  will activate the reset output pulse.

**Figure 7. STM6502, STM6503 timing**

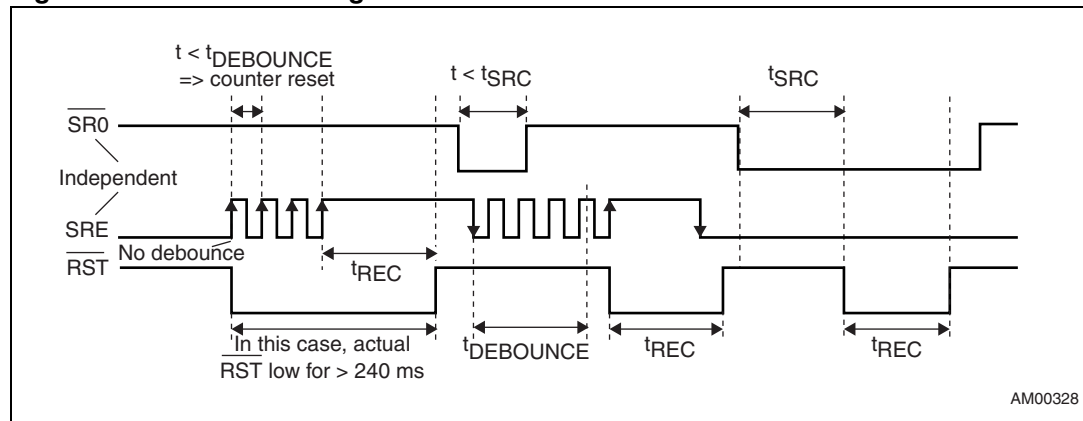


Reset will be asserted "low" right after the SRC delay time ( $t_{SRC}$ ) has been met and will be back to high after the  $t_{REC}$ .

### 3.5 Edge-triggered smart reset input (SRE) - STM6504 only

SRE is active-high, immediate and independent reset input, includes an edge trigger with debounce delay on falling edge,  $t_{\text{DEBOUNCE}} = 240 \text{ ms min.}$  See timing diagram [Figure 8](#).

**Figure 8. STM6504 timing**



### 3.6 Adjustable delay of smart reset input (SRC pin) - STM6502 and STM6505 only

This pin provides for controlling the setup time before the push-button action is validated by reset output. It is connected to an external capacitor ( $C_{\text{SRC}}$ ), optionally external resistor ( $R_{\text{SRC}}$ ), which is tied to ground for providing the desired value of setup time ( $t_{\text{SRC}}$ ).

The relation between  $t_{\text{SRC}}$  and  $C_{\text{SRC}}$  ( $R_{\text{SRC}}$ ) is given in [Section 3.6.1: Optional smart reset push-button setup delay times](#).

### 3.6.1 Optional smart reset push-button setup delay times

Table 3.  $t_{SRC}$  programmed by external capacitor

Calculated $C_{SRC}$ value [ $\mu F$ ]	Setup delay $t_{SRC}$ [s]			Closest common $C_{SRC}$ value [ $\mu F$ ]
	Min	Typ	Max	
0	0.00012 <sup>(1)</sup>	0.00015 <sup>(1)</sup>	0.00018 <sup>(1)</sup>	0
0.2	2	2.5	3.0	0.22
0.6	6	7.5	9	0.56
1	10	12.5	15	1

1. A necessary minimum to ensure debounce.

$$t_{SRC \text{ min.}} \approx 10 \times C_{SRC} \text{ [s, } \mu F]$$

*Note:* In case of quickly repeated activations of  $t_{SRC}$  counter, an interval of 10 ms min. is needed between the activations to fully discharge  $C_{SRC}$ , so that the next  $t_{SRC}$  is as specified.

Table 4.  $t_{SRC}$  programmed by external resistor

Calculated $R_{SRC}$ value [ $k\Omega$ ]	Setup delay $t_{SRC}$ [s]			Closest common $R_{SRC}$ value [ $k\Omega$ ]
	Min	Typ	Max	
0	0.00012 <sup>(1)</sup>	0.00015 <sup>(1)</sup>	0.00018 <sup>(1)</sup>	0
661	2	2.5	3.0	680
1984	6	7.5	9	2000
3307	10	12.5	15	3300

1. A necessary minimum to ensure debounce.

$$t_{SRC \text{ min.}} \approx R_{SRC} / 330.7 \text{ [s, } k\Omega]$$

*Note:* Max value of the external resistor ( $R_{SRC}$ ) is 5.688  $M\Omega$  which corresponds to  $t_{SRC} = 21.5$  s typ.

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### 3.7 Programmable smart reset input delay (TSR pin) - STM6503 and STM6504 only

Used to allow the user to program the setup time before the push-button action is validated by reset output. Controlled by different voltage levels on the three-state TSR input pin: when connected to ground,  $t_{SRC} = 2$  s; when left open,  $t_{SRC} = 6$  s; when connected to  $V_{CC}$ ,  $t_{SRC} = 10$  s (all times are minimum). TSR is a DC-type input, intended to be either permanently grounded or permanently connected to  $V_{CC}$ .

### 3.8 Reset output ( $\overline{RST}$ )

Active-low open-drain reset output in the smart reset family, no pull-up resistor.

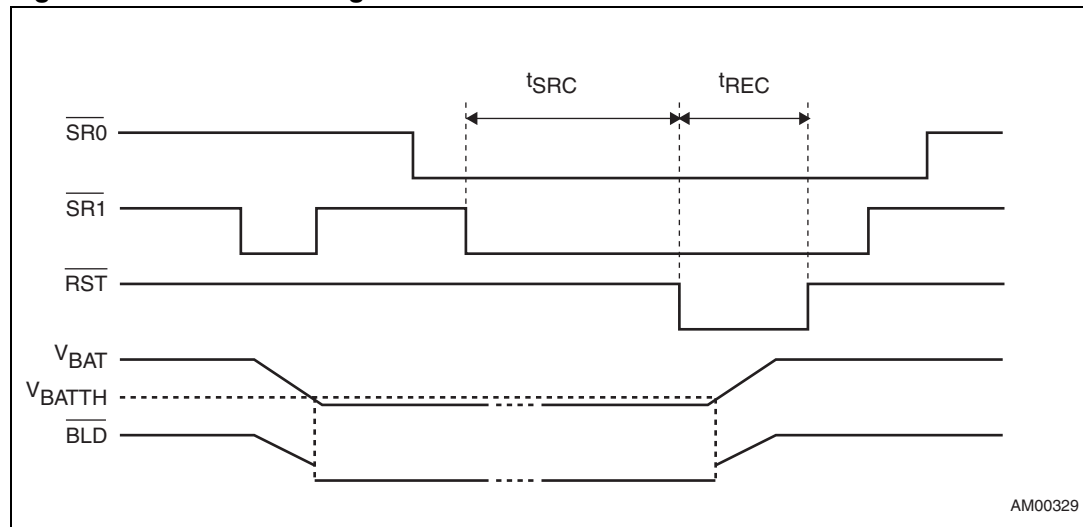
### 3.9 Battery monitor input ( $V_{BAT}$ ) - STM6505 only

An input for monitoring the battery voltage ( $V_{BAT}$ ).  $V_{BAT}$  threshold is 1.25 V, fixed, external resistor divider to be used to set the actual battery voltage threshold.  $V_{BAT}$  threshold hysteresis is 8 mV typ. (16 mV max.).

### 3.10 Battery low detect output ( $\overline{BLD}$ ) - STM6505 only

Battery low detect output controlled by the  $V_{BAT}$  voltage monitoring input, active-low, open-drain, no pull-up.

**Figure 9. STM6505 timing**



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## 4 Maximum ratings

Stressing the device above the rating listed in [Table 5: Absolute maximum ratings](#) may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

**Table 5. Absolute maximum ratings**

Symbol	Parameter		Value	Unit
$T_{STG}$	Storage temperature ( $V_{CC}$ off)		-55 to +150	°C
$T_{SLD}^{(1)}$	Lead solder temperature for 10 seconds		260	°C
$\theta_{JA}$	Thermal resistance (junction to ambient)	TDFN8	149.0	°C/W
$V_{IO}$	Input or output voltage		-0.3 to $V_{CC} + 0.3$	V
$V_{CC}$	Supply voltage		-0.3 to 7	V

1. Reflow at peak temperature of 260 °C. The time above 255 °C must not exceed 30 seconds.

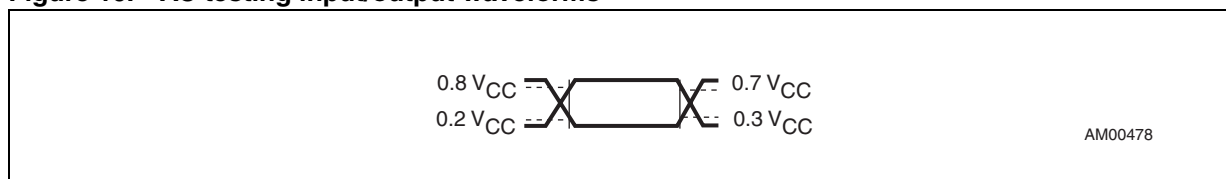
## 5 DC and AC parameters

This section summarizes the operating measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristics tables that follow, are derived from tests performed under the measurement conditions summarized in [Table 6: Operating and measurement conditions](#). Designers should check that the operating conditions in their circuit match the operating conditions when relying on the quoted parameters.

**Table 6. Operating and measurement conditions**

Parameter	Value	Unit
V <sub>CC</sub> supply voltage	1.0 to 5.5	V
Ambient operating temperature (T <sub>A</sub> )	-40 to +85	°C
Input rise and fall times	≤ 5	ns
Input pulse voltages	0.2 to 0.8 V <sub>CC</sub>	V
Input and output timing ref. voltages	0.3 to 0.7 V <sub>CC</sub>	V

**Figure 10. AC testing input/output waveforms**



**Table 7. DC and AC characteristics**

Symbol	Parameter	Test conditions <sup>(1)</sup>	Min	Typ	Max	Unit
V <sub>CC</sub>	Supply voltage range	Reset output valid - active-low	1.0		5.5	V
I <sub>CC</sub>	Supply current (V <sub>CC</sub> )	STM6502, V <sub>CC</sub> = 5.0 V		1.2	2.3	μA
		STM6503, V <sub>CC</sub> = 5.0 V		4	5.8	μA
		STM6504, V <sub>CC</sub> = 5.0 V		4	5.8	μA
		STM6505, V <sub>CC</sub> = 5.0 V		1.9	3.3	μA
V <sub>OL</sub>	Reset output voltage low (reset asserted: RST, BLD)	V <sub>CC</sub> ≥ 4.5 V, sinking 3.2 mA			0.3	V
		V <sub>CC</sub> ≥ 3.3 V, sinking 2.5 mA			0.3	V
		V <sub>CC</sub> ≥ 1.0 V, sinking 0.1 mA			0.3	V

## DC and AC parameters

## STM6502, STM6503, STM6504, STM6505

Table 7. DC and AC characteristics (continued)

Symbol	Parameter	Test conditions <sup>(1)</sup>	Min	Typ	Max	Unit
<b>Reset thresholds</b>						
$V_{RST}$	Fixed voltage trip point for $V_{CC}$ (refer to <a href="#">Table 8</a> )	-40 to +85 °C	$V_{RST}$ -2.5%	$V_{RST}$	$V_{RST}$ +2.5%	V
		25 °C	$V_{RST}$ -2.0%	$V_{RST}$	$V_{RST}$ +2.0%	V
$V_{HYST}$	Hysteresis of $V_{RST}$	L, M		0.5%		
		T, S, R, Z, Y, W, V		1%		
	$V_{CC}$ to reset delay	$V_{CC}$ falling from ( $V_{RST} + 100$ mV) to ( $V_{RST} - 100$ mV) at 10 mV/ $\mu$ s		20		$\mu$ s
$t_{REC}$	Reset timeout delay, factory-programmed	Option A	140	210	280	ms
		Option B	240	360	480	ms
$t_{DEBOUNCE}$		STM6504 only	240	360	480	ms
<b><math>V_{BAT}</math> thresholds</b>						
$V_{BATTH}$	Fixed $V_{BAT}$ monitoring threshold	STM6505 only	1.225	1.25	1.275	V
$V_{BATHYST}$	$V_{BATTH}$ hysteresis	STM6505 only		8	16	mV
<b>SR input</b>						
$V_{IL}$	$\overline{SR0}$ , $\overline{SR1}$ , SRE input voltage low				0.3 $V_{CC}$	V
$V_{IH}$	$\overline{SR0}$ , $\overline{SR1}$ , SRE input voltage high		$0.7 V_{CC}$			V
$I_{LI(SR)}$	Input leakage current, $\overline{SR}$ and SRE inputs	option without internal pull-up resistor	-1		+1	$\mu$ A
$I_{LI(TSR)}$	Input leakage current, TSR input	STM6503 and STM6504 only	-10		+10	$\mu$ A
$R_{PUI}$	Internal pull-up resistor, input (optional - refer to <a href="#">Table 12</a> )	at 3.3 V and 25 °C		65		k $\Omega$
$R_{SRC}$	Refer to <a href="#">Table 4</a>		0		5.688	M $\Omega$
$C_{SRC}$	1 $\mu$ F / 10 s (refer to <a href="#">Table 3</a> )		0			$\mu$ F
$t_{SRC}^{(2)}$	Delayed smart reset setup time, STM6503 and STM6504. For STM6502 and STM6505 please refer to <a href="#">Table 3</a> and <a href="#">Table 4</a> .	TSR = $V_{SS}$	2	2.5	3	s
		TSR = floating	6	7.5	9	s
		TSR = $V_{CC}$	10	12.5	15	s

1. Valid for ambient operating temperature:  $T_A = -40$  to +85 °C;  $V_{CC} = 1.0$  to 5.5 V (except where noted).

2. Input glitch immunity is equal to  $t_{SRC}$ .



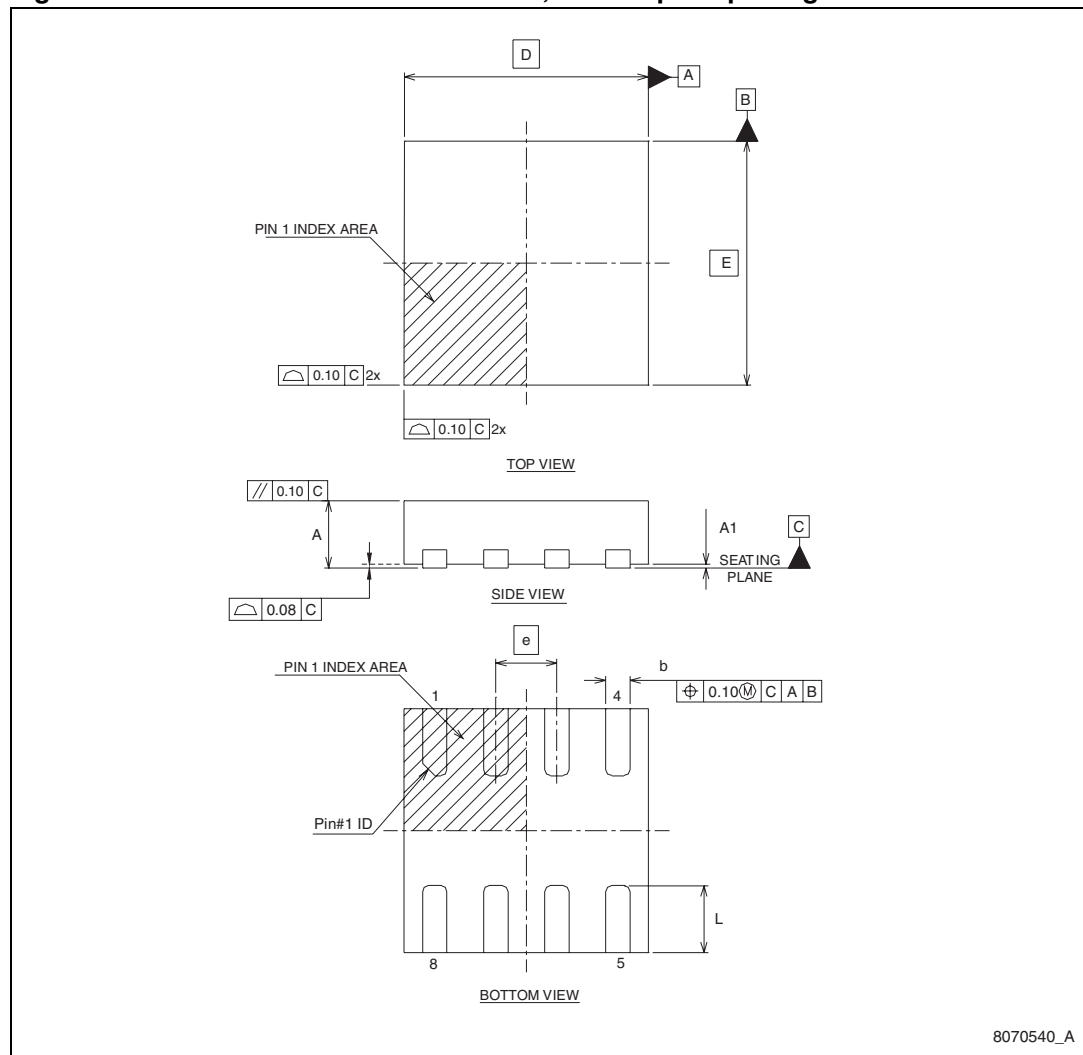
Table 8.  $V_{CC}$  voltage thresholds

$V_{CC}$ voltage threshold $V_{RST}$	Typ	$\pm 2.5\%$ ( $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ )		$\pm 2.0\%$ ( $25\text{ }^{\circ}\text{C}$ )		Unit
		Min	Max	Min	Max	
L (falling)	4.625	4.509	4.741	4.533	4.718	V
M (falling)	4.375	4.266	4.484	4.288	4.463	V
T (falling)	3.075	2.998	3.152	3.014	3.137	V
S (falling)	2.925	2.852	2.998	2.867	2.984	V
R (falling)	2.625	2.559	2.691	2.573	2.678	V
Z (falling)	2.313	2.255	2.371	2.267	2.359	V
Y (falling)	2.188	2.133	2.243	2.144	2.232	V
W (falling)	1.665	1.623	1.707	1.632	1.698	V
V (falling)	1.575	1.536	1.614	1.544	1.607	V

## 6 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

Figure 11. TDFN – 8-lead 2 x 2 x 0.75 mm, 0.5 mm pitch package outline



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Table 9. TDFN – 8-lead 2 x 2 x 0.75 mm, 0.5 mm pitch package mechanical data

Symbol	(mm)			(inches)		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00	0.02	0.05	0.000	0.001	0.002
b	0.15	0.20	0.25	0.006	0.008	0.010
D BSC		2.00			0.079	
E BSC		2.00			0.079	
e		0.50			0.020	
L	0.45	0.55	0.65	0.018	0.022	0.026

## Package mechanical data

## STM6502, STM6503, STM6504, STM6505

Figure 12. Carrier tape

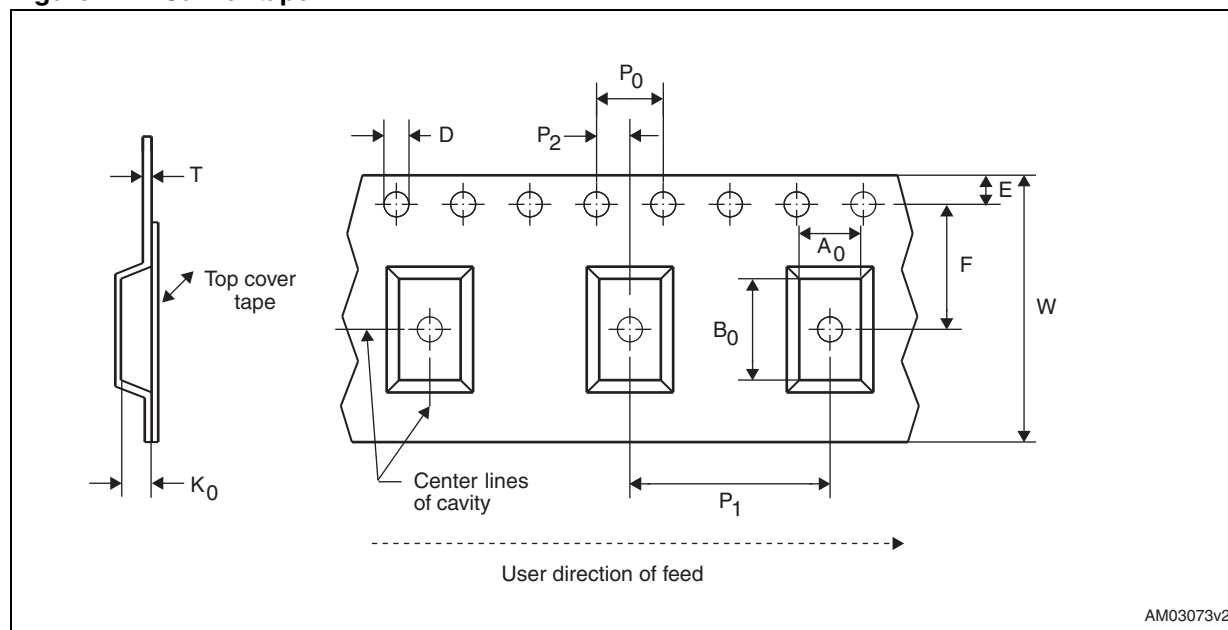


Table 10. Carrier tape dimensions

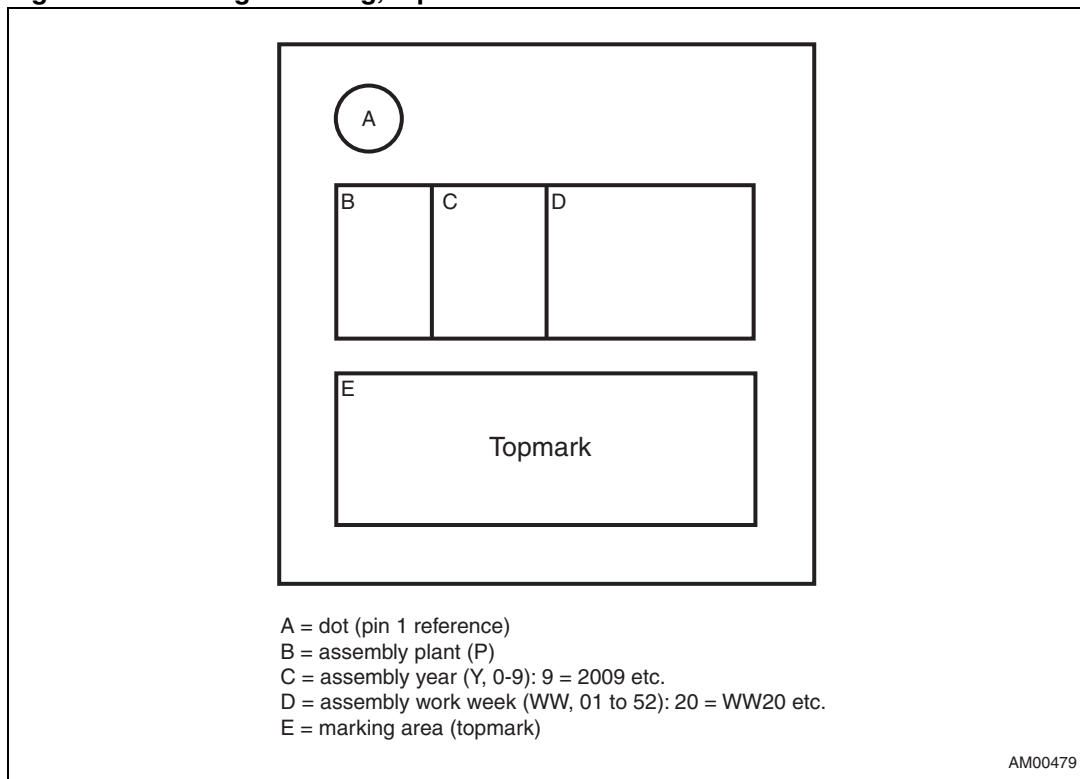
Package	W	D	E	P <sub>0</sub>	P <sub>2</sub>	F	A <sub>0</sub>	B <sub>0</sub>	K <sub>0</sub>	P <sub>1</sub>	T	Unit	Bulk Qty
TDFN8	8.00 +0.30 -0.10	1.50 +0.10/ -0.00	1.75 ±0.10	4.00 ±0.10	2.00 ±0.10	3.50 ±0.05	2.30 ±0.05	2.30 ±0.05	1.00 ±0.05	4.00 ±0.10	0.250 ±0.05	mm	3000

Table 11. Package marking

Part number	$t_{SRC}$ delay control	Smart reset inputs <sup>(1)</sup>	$V_{RST}$	RST output <sup>(1)</sup>	$t_{REC}$ option	BLD output <sup>(1)</sup>	Topmark
STM6503VEAADG6F	TSR	AL	V	AL, OD	A	-	3VG
STM6504SEABDG6F	TSR	AL	S	AL, OD	B	-	4SG
STM6505SDABDG6F	$R_{SRC}$	AL, PU	S	AL, OD	B	AL, OD	5SI
STM6505RDABDG6F	$R_{SRC}$	AL, PU	R	AL, OD	B	AL, OD	5RI
STM6505WDABDG6F	$R_{SRC}$	AL, PU	W	AL, OD	B	AL, OD	5WI

1. AL = active-low, AH = active-high, PU = with internal pull-up resistor, OD = open-drain.

Figure 13. Package marking, top view



## 7 Part numbering

**Table 12. Ordering information scheme**

Example:	STM6505	W	D	A	B	DG	6	F
<b>Device type</b>								
STM6502 <sup>(1)</sup>								
STM6503								
STM6504								
STM6505								
<b>Reset (<math>V_{CC}</math> monitoring) threshold voltage (<math>V_{RST}</math>)</b>								
L = 4.625 V (typ., falling)								
S = 2.925 V								
R = 2.625 V								
Z = 2.313 V								
W = 1.665 V								
V = 1.575 V								
<b>Smart reset setup delay (<math>t_{SRC}</math>); presence of internal input pull-up on all smart reset inputs (<math>SRx</math>, <math>SRE</math>)</b>								
B = 0 to 15 s, user-programmed (external resistor); no input pull-up								
D = 0 to 15 s, user-programmed (external resistor); 65 k $\Omega$ input pull-up								
E = 2 or 6 or 10 s min., user-programmed (three-state); no input pull-up								
F = 2 or 6 or 10 s min., user-programmed (three-state); 65 k $\Omega$ input pull-up								
<b>Output type</b>								
A = open-drain, no pull-up, active-low								
<b>Reset timeout period (<math>t_{REC}</math>)</b>								
A = 140 ms min.								
B = 240 ms min.								
<b>Package</b>								
DG = TDFN8 2 x 2 x 0.75 mm, 0.5 mm pitch								
<b>Temperature range</b>								
6 = -40 °C to +85 °C								
<b>Shipping method</b>								
F = ECOPACK <sup>®</sup> package, tape and reel								

1. Contact local ST sales office for availability.

For other options, voltage threshold values etc. or for more information on any aspect of this device, please contact the ST sales office nearest you.

## 8 Revision history

**Table 13. Document revision history**

Date	Revision	Changes
31-Aug-2009	1	Initial release.

**STM6502, STM6503, STM6504, STM6505**

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