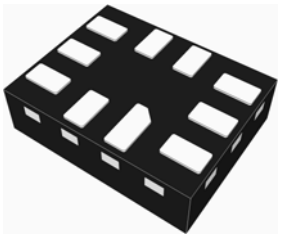
STM6620S

Smart push-button, on/off controller with Smart Reset™ discharge paths and PMOS driver

Datasheet



Features

- Operating voltage: 2.2 V to 5.5 V
- Low supply current:10 µA max.
- Deep sleep mode: 5 µA max.
- Dual Smart Reset™ push-button inputs with fixed extended setup delay (T_r)
- Power-on reset
- Two discharge paths
- Charger insertion detection
- Dual outputs: SR0 active high and nSR0 active low
- Operating temperature: -40 °C to 85 °C
- QFN10 package 1.8x1.4x0.5 mm
- Ecopack®3 (RoHS compliant, Halogen-free)

Applications

- Smartphones

Description

The Smart Reset™ devices provide a useful feature that ensures inadvertent short reset push-button closures do not cause system resets. This is done by implementing an extended Smart Reset™ input delay time (T_r) and combined push-button inputs, which together ensure a safe reset and eliminate the need for a specific dedicated reset button.

The STM6620S has two combined delayed Smart Reset™ inputs (RST0 and RST1) with a preset, delayed, Smart Reset™ setup time (T_r). The reset output is asserted after both the Smart Reset™ inputs are in a predefined state during the T_r delay time. The reset outputs then remain active during T_d. Two outputs are available, one is active low (nSR0) while the other is active high (SR0). SR0 is capable of driving en external PMOS to connect or disconnect the battery.

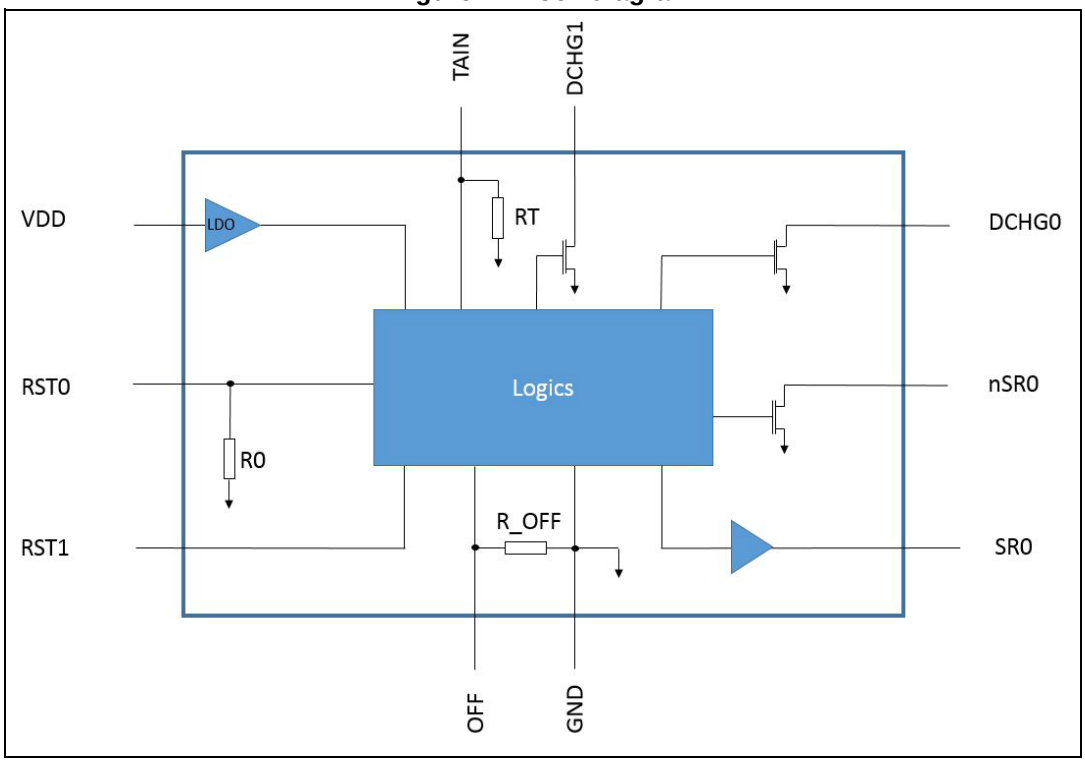
The STM6620S also offers two discharge paths to ensure a correct system setup before the complete restart of a smartphone. A dedicated pin is able to detect if a voltage is present on the USB connector, which means the charger is plugged in.

This device fully operates over the broad supply voltage range of 2.2 V to 5.5 V and over the industrial temperature range -40 °C to 85 °C.

Contents

1 Functional description

Figure 1. Block diagram



2 Pinout information

Figure 2. Pin connections (top view)

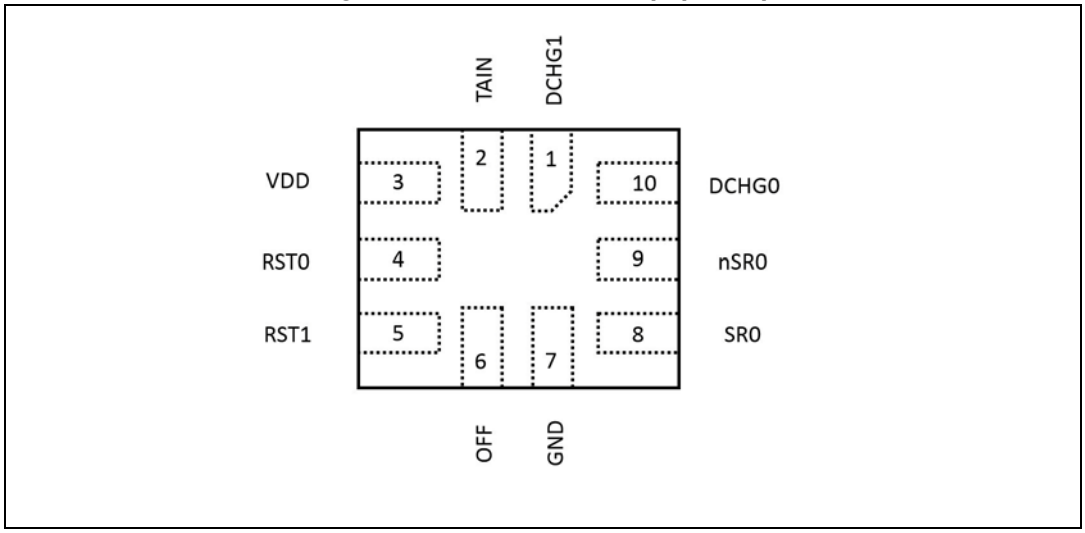


Table 1. Pin description

Pin	Name	Type	Description
1	DCHG1	Output	Discharge path 1
2	TAIN	Input	Charger insertion detection
3	VDD	Power supply	Power supply input
4	RST0	Input	Reset signal input 0
5	RST1	Input	Reset signal input 1
6	OFF	Input	Ship mode command input
7	GND	Power supply	Power supply GND
8	SR0	Output	Smart Reset™ output, active high
9	nSR0	Output	Smart Reset™ output, active low
10	DCHG0	Output	Discharge path 0

3 Absolute maximum ratings and operating conditions

Table 2. Absolute maximum ratings (AMR)

Symbol	Parameter	Value	Unit
V_{DD}	Supply voltage (1)	-0.3 to 12	V
RST0, SR0	Reset signal input Smart Reset™ output	-0.3 to 12	
RST1	Reset signal input	-0.3 to 6	
OFF	Ship mode command input	-0.3 to 6	
nSR0	Smart Reset™ output	-0.3 to 6	
DCHG0, DCHG1	Discharge input pins	-0.3 to 12	
TAIN	Charger insert detection pin (2)	-0.3 to 6	
T_{Lead}	Lead temperature for 10s (3)	260	°C
T_{stg}	Storage temperature	-65 to 150	
T_j	Maximum junction temperature	150	
R_{thja}	Thermal resistance junction-to-ambient (4) (5)	124	°C/W
ESD	HBM: human body model (6)	2000	V
	MM: machine model (7)	200	
	CDM: charged device model (8)	1300	
	Latch-up immunity	200	mA

1. All voltage values, except the differential voltage, are with respect to the network ground terminal.
2. An external 100 kOhms serial resistor is required to withstand the 30 V DC voltage on the USB port. See the application section for more details.
3. Reflow at peak temperature of 260 °C. Time above 255 °C must not exceed 30 s.
4. Short-circuits can cause excessive heating and destructive dissipation.
5. R_{th} are typical values.
6. According to JEDEC standard JESD22-A114F
7. According to JEDEC JESD22-A115C Nov.2010
8. According to ANSI/ESD STM5.3.1

Table 3. Operating conditions

Symbol	Parameter	Value	Unit
V_{DD}	Supply voltage	2.2 to 5.5	V
T_{oper}	Operating free-air temperature range	-40 to +85	°C

4 Electrical characteristics

Table 4. Electrical characteristics at V_{DD} = 4 V, T_{oper} = 25 °C, (unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Power supply						
I_Q	Quiescent supply current				1	µA
I_{OFF}	Current in active ship mode				5	
I_{DD}	Operating current	$T_{min.} < T_{oper} < T_{max.}$			10	
T_W	Wakeup time			1	3	ms
Digital IO						
V_{IL}	Logical low-level input	RST0, RST1, OFF			0.4	V
V_{IH}	Logical high-level input	RST0, RST1, OFF	1			
I_L	Input leakage current	RST0, RST1			1	µA
R0	Pull-down resistor	RST0		8		MΩ
T_{ta}	Debounce time	RST0, RST1, TAIN		10		ms
V_{OL}	Logical low-level output	SR0, V_{DD}>2.2V, I = 1mA			0.3	V
V_{OH}	Logical high-level output	SR0, V_{DD}>2.2V, I = 1 mA	0.85 x V_{DD}			V
		SR0, V_{DD}>2.2V, I = 0.1 mA	0.95 x V_{DD}			
V_{nSR0_OL}	Output drive voltage	nSR0, I_{PU} = 2 mA and V_{DD} > 2.5 V, $T_{min.} < T_{oper} < T_{max.}$			0.3	V
V_{IL_TAIN}	TAIN logical low-level input				0.16	V
V_{IH_TAIN}	TAIN logical high-level input		0.4			
RT	Pull-down resistor on TAIN		12	15	18	kΩ
Reset						
T_r	Smart Reset™ delay	STM6620SAx		8		s
		STM6620SBx		10		
		STM6620SCx		12		
		STM6620SDx		16		
	Accuracy		-10		10	%
T_d	Discharge time	STM6620SxA		200		ms
		STM6620SxB		300		
		STM6620SxC		400		
		STM6620SxD		600		
	Accuracy		-10		10	%
T_{dd}	Discharge delay time		4	5	6	ms
I_d	Discharge current	Vout = 4 V	50	60	70	mA

Table 4. Electrical characteristics at V_{DD} = 4 V, T_{oper} = 25 °C, (unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Ship mode						
R_OFF	Pull-down resistor	OFF pin		1		MΩ
T_S	Ship mode enter delay		12	15	18	s
	Ship mode command enter			5		Cycle
T1	High and low hold time	(1)	0.5		1	ms
T2	Total 5 pulse time		80		100	
T3	Time to keep RST0 low to exit ship mode			2		s
	Accuracy		-20		20	%

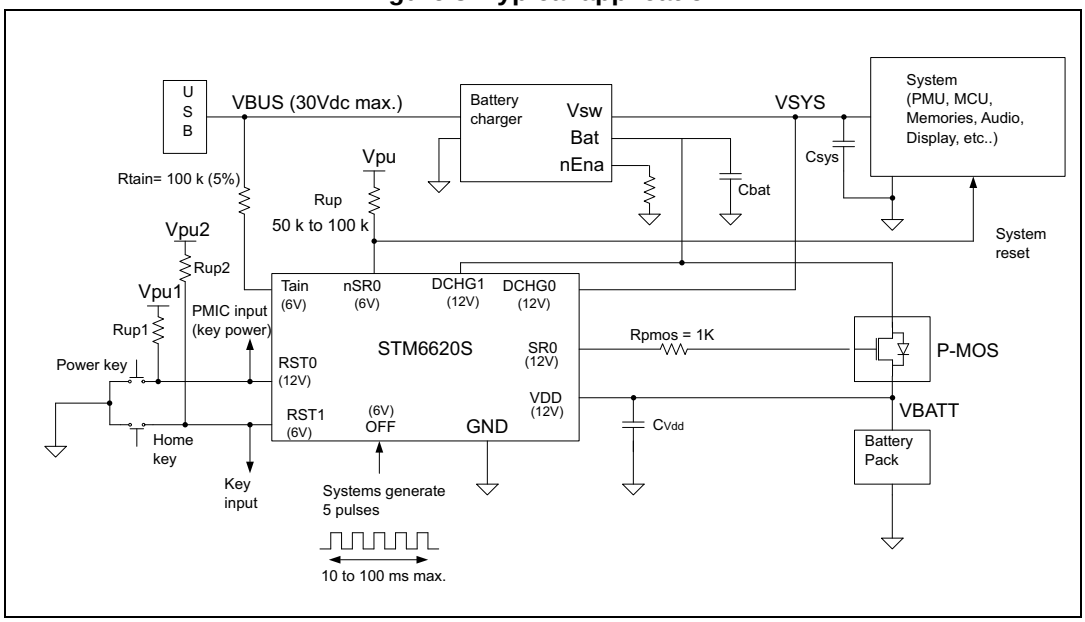
1. Pulse high or low time < T1 min., invalid pulse.
Pulse high or low time > T1 max., valid pulse.
Entering ship mode: mandatory to provide 5 pulses with width > T1 max.

5 Application information

5.1 Typical application

Figure 3 represents the STM6620S in a typical smartphone platform. This figure gives the different connections of the device inputs/outputs.

Figure 3. Typical application



The device is supplied by the battery voltage through the VDD and GND pins. When the device is not supplied, in the case of a dead or disconnected battery, the PMOS is not controlled but the charger can start to charge the battery thanks to the intrinsic PMOS diode. The current flowing to the battery is then the “trickle low current” due to the low battery voltage. When the battery voltage is above the battery protection voltage cut-off, the STM6620S is able to control the PMOS itself. A reset operation or a ship mode request can then be performed.

The RST0 and RST1 input keys are used to request a reset of the application and allow the capacitors to discharge. RST0 has a pull-down resistor (R0) with a high value (see *Table 4*) for 12 V protection as specified in *Table 2*.

The TAIN input is directly connected to the external power supply line through a resistor of 100 kΩ. In most cases, this power line will be the VBUS line coming from the USB connector used to charge the battery.

The digital OFF input is used to force the system into ship mode, a low current consumption mode (see *Section 5.3* for more details).

SR0 and nSR0 are digital outputs. SR0 is able to control an external PMOS transistor and nSR0 asks the processor to reset.

DCHG0 and DCHG1 are discharge inputs that can pull the system capacitors down to ground.

5.2 Truth table

Figure 4 presents a truth table describing the STM6620S behavior in various situations.

Figure 4. Truth table description

	Event0					State 0			Event0 For (in s)	State 1			Time between State 1 and State 2	State 2			OSC ON or Idd=10uA max
	AVDD	RST0	RST1	TAIN	OFF	SR0	nSR0	DCHGx		SR0	nSR0	DCHGx		SR0	nSR0	DCHGx	
POR	VDD ↑	X	X	X	X	L	open	open	0.5m	H	X	X		L	open	open	ON during Tta
RESET	VDD	H	X	X	L	L	open	open	-	L	open	open		L	open	open	OFF
	VDD	X	H	X	L	L	open	open	-	L	open	open		L	open	open	OFF
	VDD	L	L	X	X	L	open	open	Tr	↑	↓	↓	Td+2Tdd	↓	↑	↑	ON during Tr+Td +2Tdd
ENTER SHIP	VDD	X (H if RST1= L)	X (H if RST0 =L)	X	5 pul ses	L	open	open	Ts	↑	open	open	0	H	open	open	ON during Ts (and OFF in ship mode)
	VDD	H	H	L	L	L	open	open	X	L	open	open		L	open	open	OFF
EXIT SHIP	VDD	X	X	H	X	H	open	open	10m	↓	open	open	0	L	open	open	ON during Tta
	VDD	L	X	X	X	H	open	open	T3	↓	open	open	0	L	open	open	ON during T3

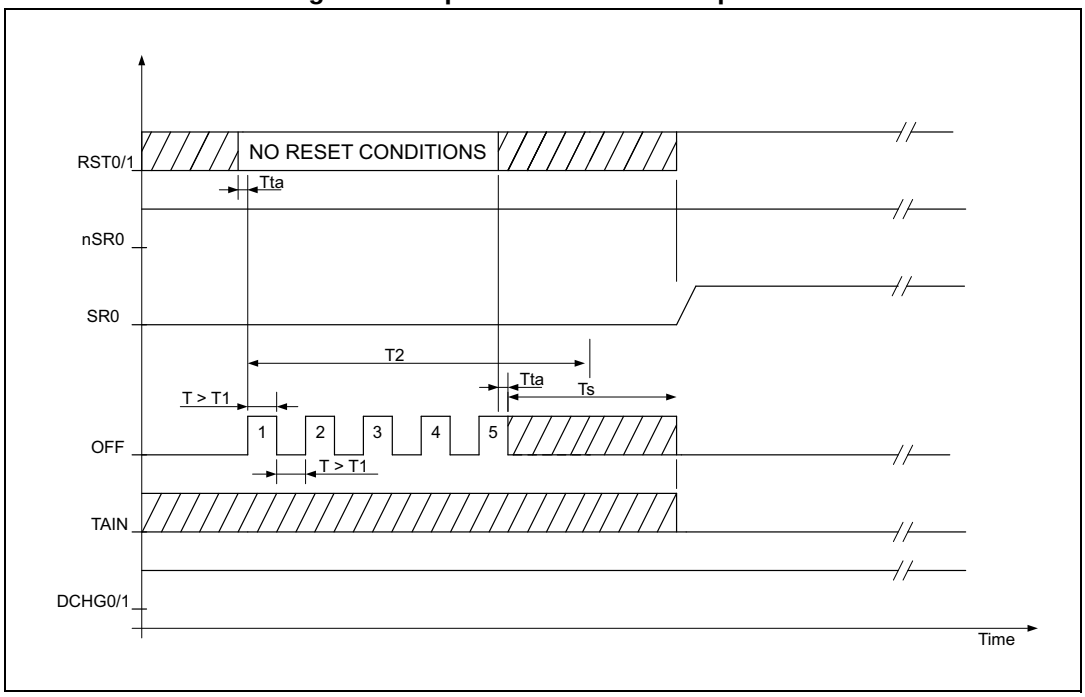
5.3 Ship mode (OFF pin)

The digital OFF input is used to force the system into ship mode. The main purpose of this mode is to disconnect the battery from the rest of the hardware application. Thus, the battery only supplies the STM6620S during the time the smartphone is off the shelf and waiting for its final customer to open the box.

Ship mode ensures the lowest power consumption on the smartphone from production factory output to system startup. The OFF input is directly connected to a digital output of the platform, generally the application processor. To enter ship mode, the STM6620S must detect five pulses with the correct format on the OFF pin during a fixed duration (T2).

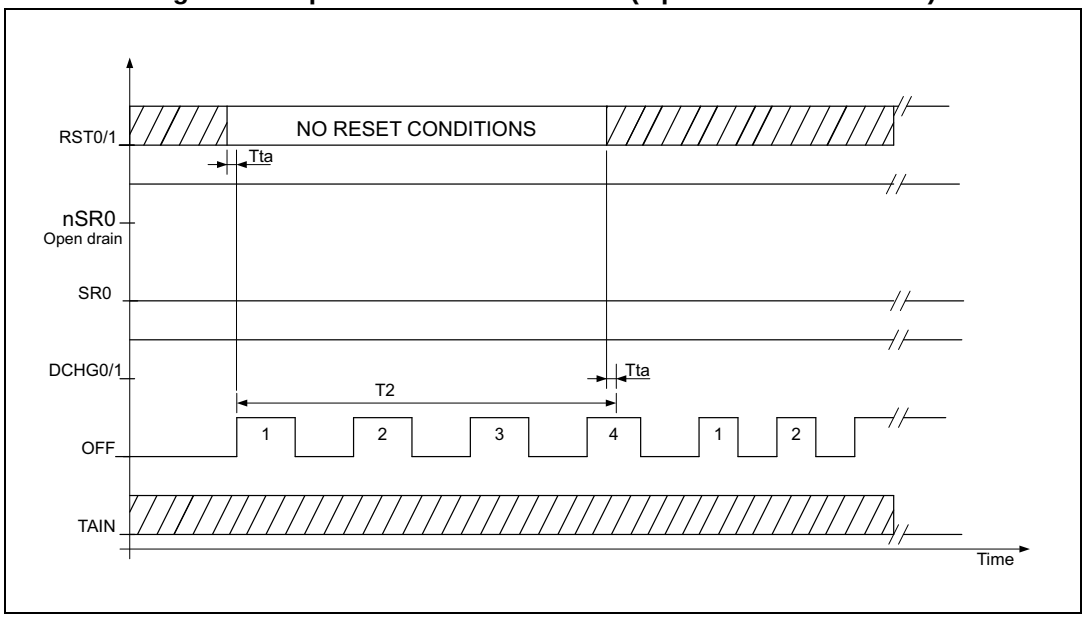
Details of the ship mode activation sequence are given in *Figure 5*.

Figure 5. Ship mode activation sequence



During the ship mode activation sequence, the capacitors on the platform must not be discharged. If the five pulses expected on the OFF pin (to enter ship mode) are not provided during T2, ship mode will not be active as shown in *Figure 6*.

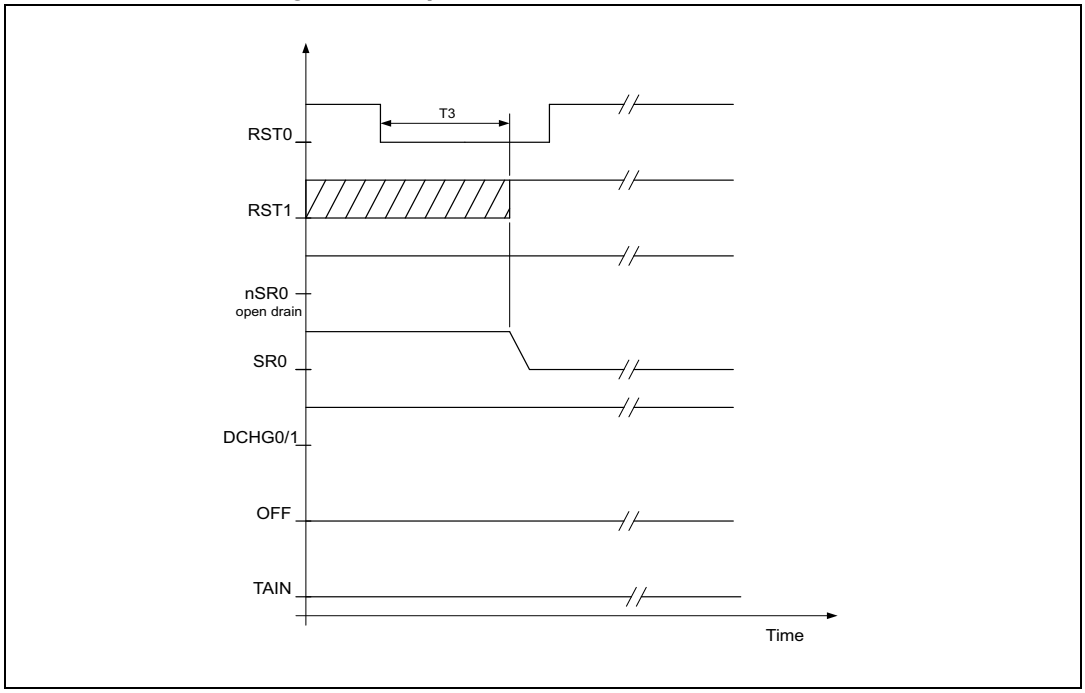
Figure 6. Ship mode activation failure (5 pulses out of time T2)



Note: Reset conditions are those defined in Section 5.5. A reset is only taken into account after a debouncing delay of Tta. So, if a reset appears when the ship pulses are set on the OFF pin, the reset occurs only if the debouncing time has elapsed. In all other cases, ship mode is activated.

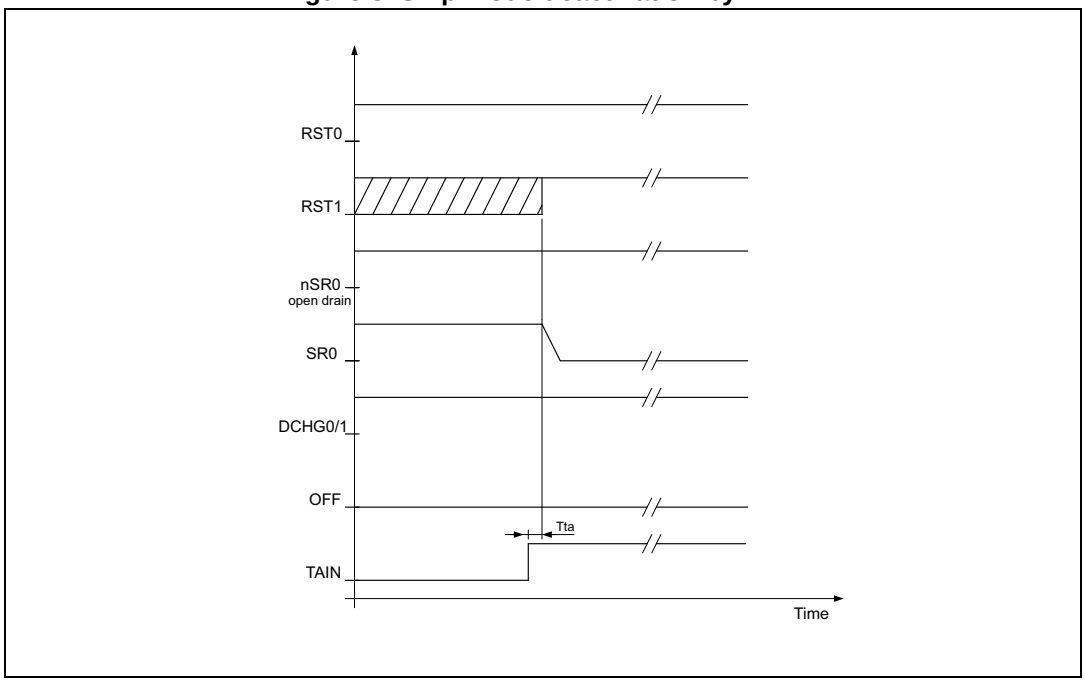
To exit ship mode, a different process has been put in place. RST0 must be pulled down during T3 to generate a ship mode exit signal. Details are provided in *Figure 7*.

Figure 7. Ship mode deactivation with RST0



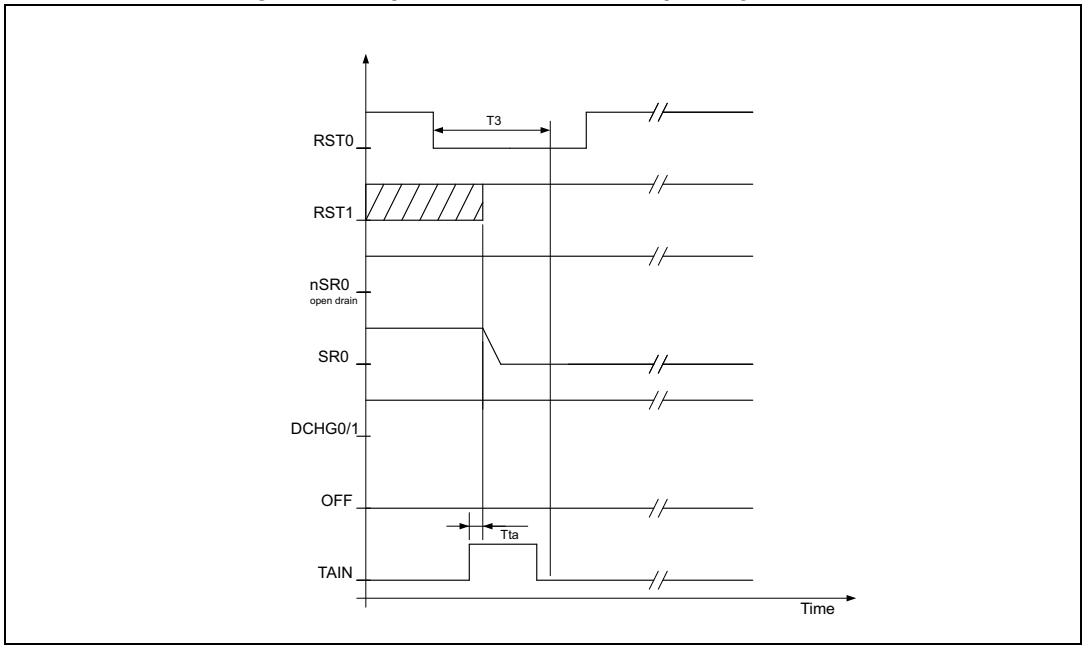
Ship mode can also be disabled by inserting a charger as shown in *Figure 8*.

Figure 8. Ship mode deactivation by TAIN



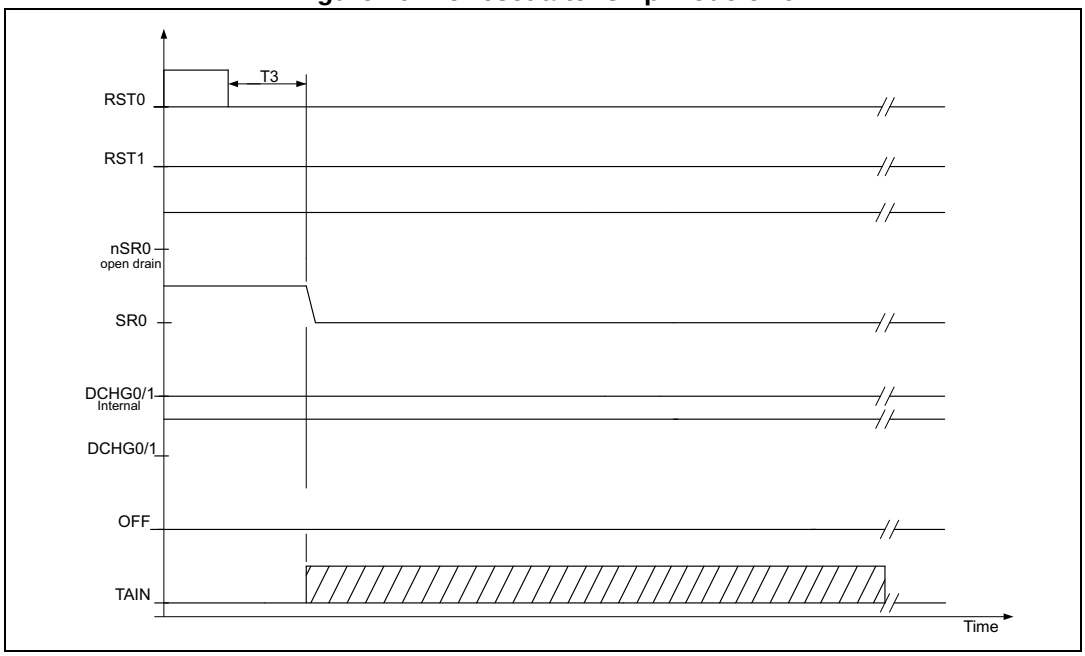
If RST0 is at a low level (the condition to exit ship mode) and the charger is inserted (TAIN rising) during T3, the charger detection (TAIN) has a higher priority as shown in *Figure 9*.

Figure 9. Ship mode deactivation, priority to TAIN



If reset conditions are present after a ship mode exit, no reset occurs as described in *Figure 10*. A reset can occur only if RST0 or RST1 are released and pressed again.

Figure 10. No reset after ship mode exit



In case the charger is detected on the Tain pin during the ship mode process (Ts), Tain is ignored and the STM6620S enters ship mode. However, if the Tain pin is high at the end of Ts, STM6620S enters ship mode then exits it as shown in *Figure 11* and *Figure 12*.

Figure 11. Ship mode behavior if charger is present at the end of Ts

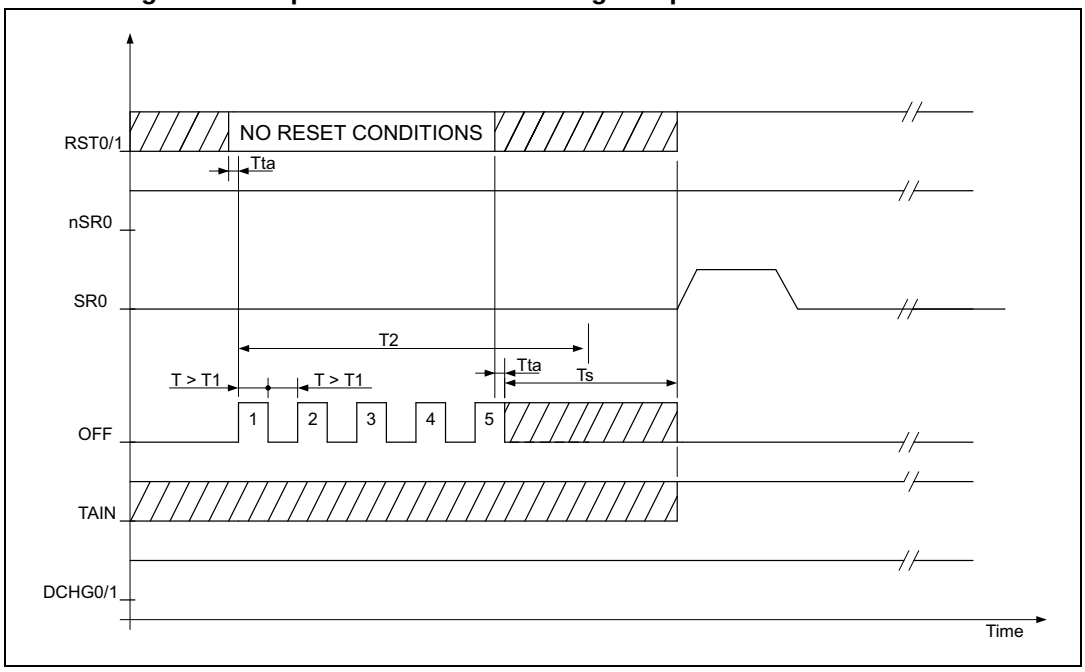
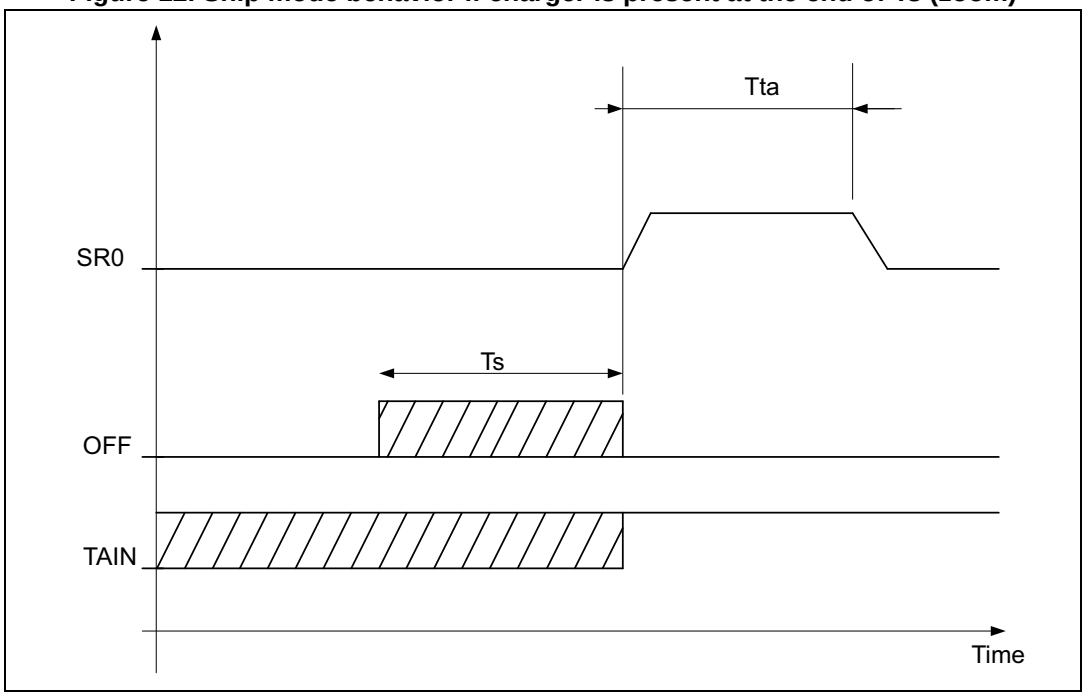


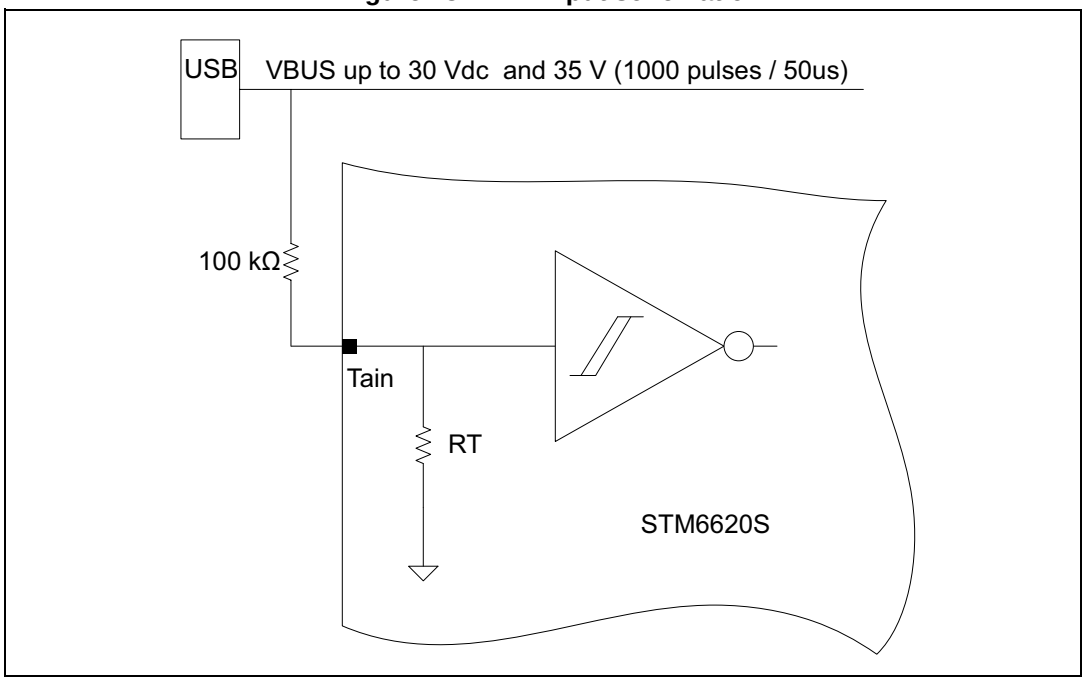
Figure 12. Ship mode behavior if charger is present at the end of Ts (zoom)



5.4 Charger insertion detection pin (TAIN)

The TAIN input is directly connected to the power supply line of the USB port (VBUS) through an external serial resistor of 100 kΩ (see *Figure 13*). The 100 kΩ external resistor creates a resistor divider with the internal resistor (R_T) to ensure the voltage on the TAIN pin respects the AMR value in *Table 2*. With the upcoming, new USB power delivery standard, the VBUS voltage is expected to vary and may require higher voltage values. So, TAIN must be protected with an external serial resistor.

Figure 13. TAIN input schematic



5.5 Reset description

The RST0 and RST1 input keys are used to request a system reset and capacitor discharge. To enter reset mode, the following conditions must be present:

- Both RST0 and RST1 must be at a low level during Tr
- When RST0 or RST1 is pressed during Ts, the action is ignored

When a reset occurs, STM6620S first turns off the external PMOS by rising SR0 to a high level. Then the device discharges the system capacitors by pulling down the DCHG0 and DCHG1 outputs. The combination of the RST0 and RST1 actions and their effects is shown in *Figure 14*, *Figure 15*, and *Figure 16*.

Figure 14. Normal reset operation with RST0 acting

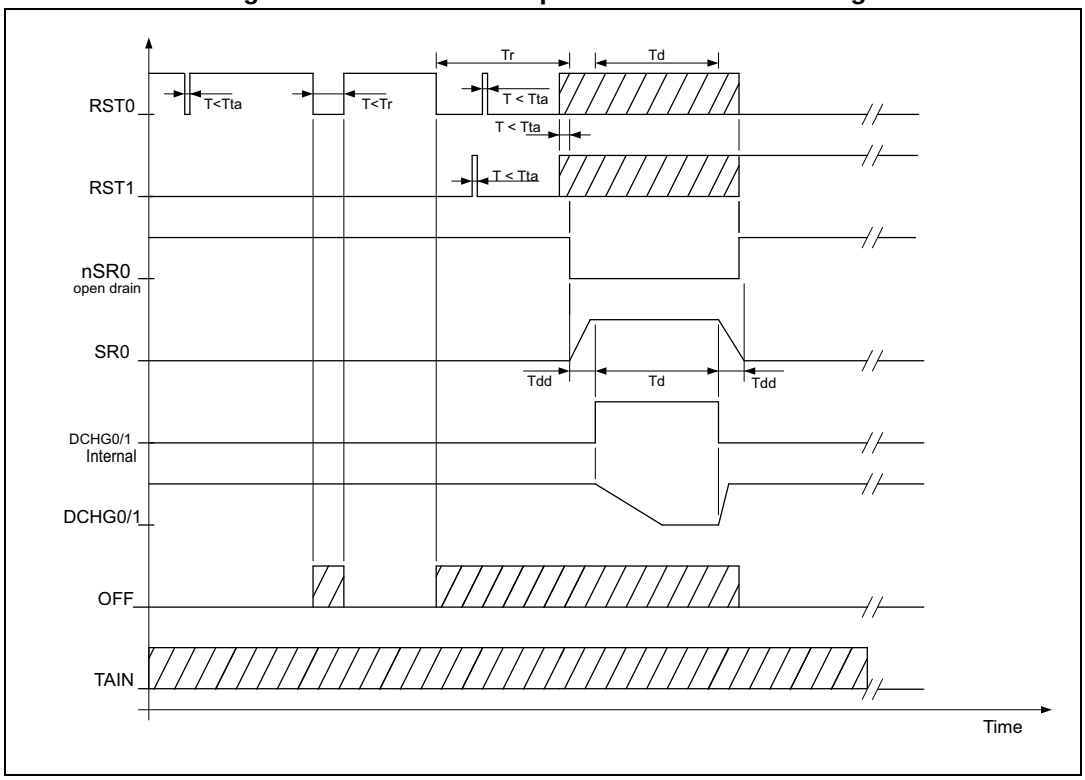


Figure 15. Normal reset operation with RST0 acting (zoom)

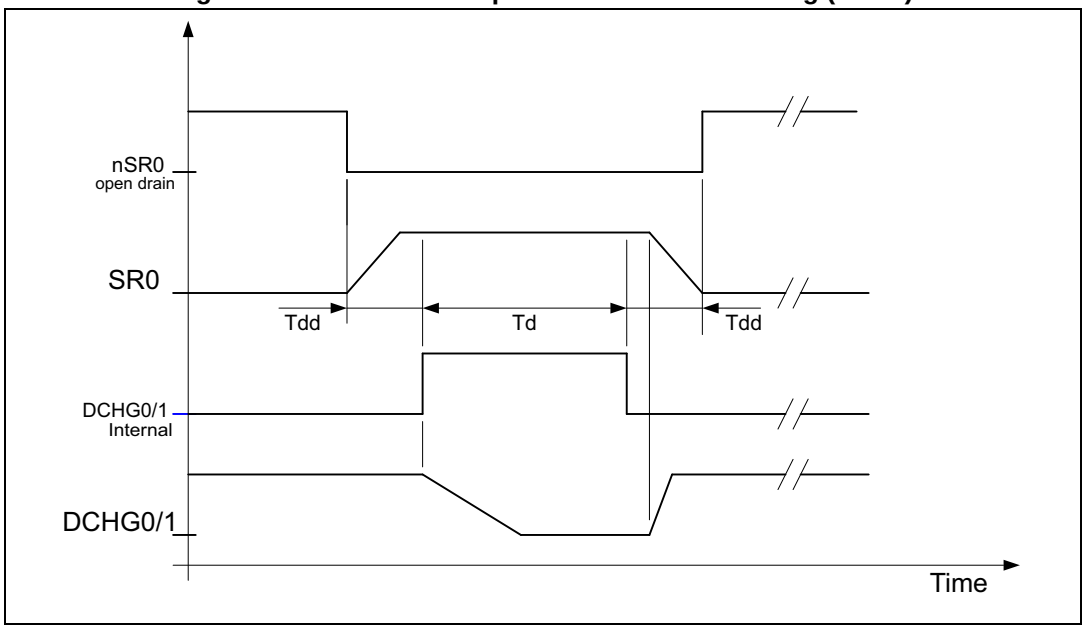
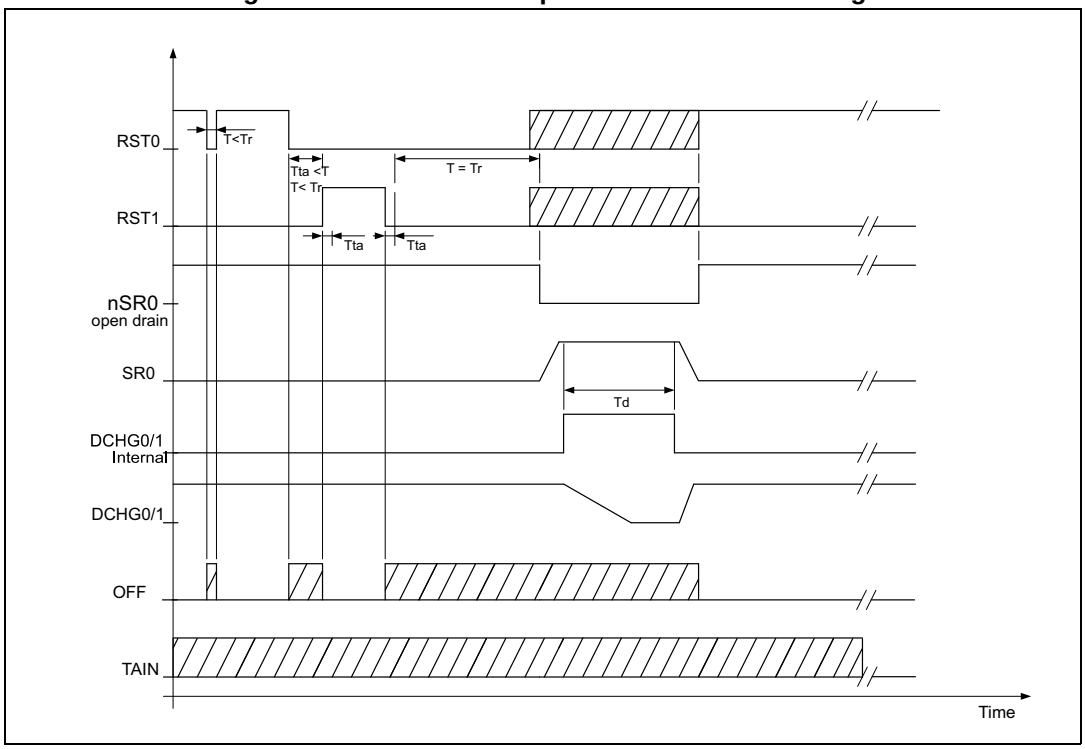
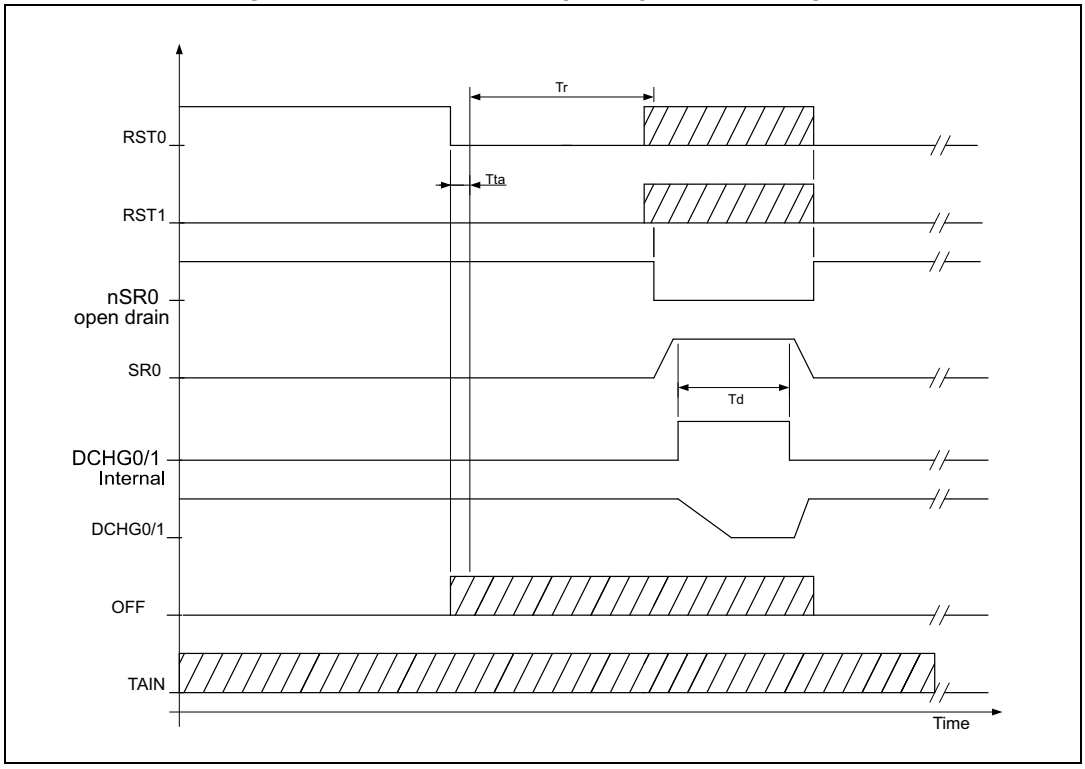


Figure 16. Normal reset operation with RST1 acting



A debounce function is designed on the RST0 and RST1 input keys to avoid false switching. The debounce time is specified with the T_{ta} parameter (see *Table 4*). Once RST0 and RST1 are simultaneously at a low level, all other inputs are ignored. If RST0/1 are at a low level during Tr, a reset occurs and it cannot be interrupted by any other inputs. If a signal is detected on the OFF pin during Tr, it has no effect as both RST0 and RST1 at a low level have the highest priority (see *Figure 17*).

Figure 17. RST0 and RST1 priority over OFF signal



If RST0 and RST1 stay in the appropriate conditions for a reset for a long time, multiple resets are not allowed except if RST0 or RST1 is released. This behavior is described in *Figure 18* and *Figure 19*.

Figure 18. Multiple reset behavior with RST0

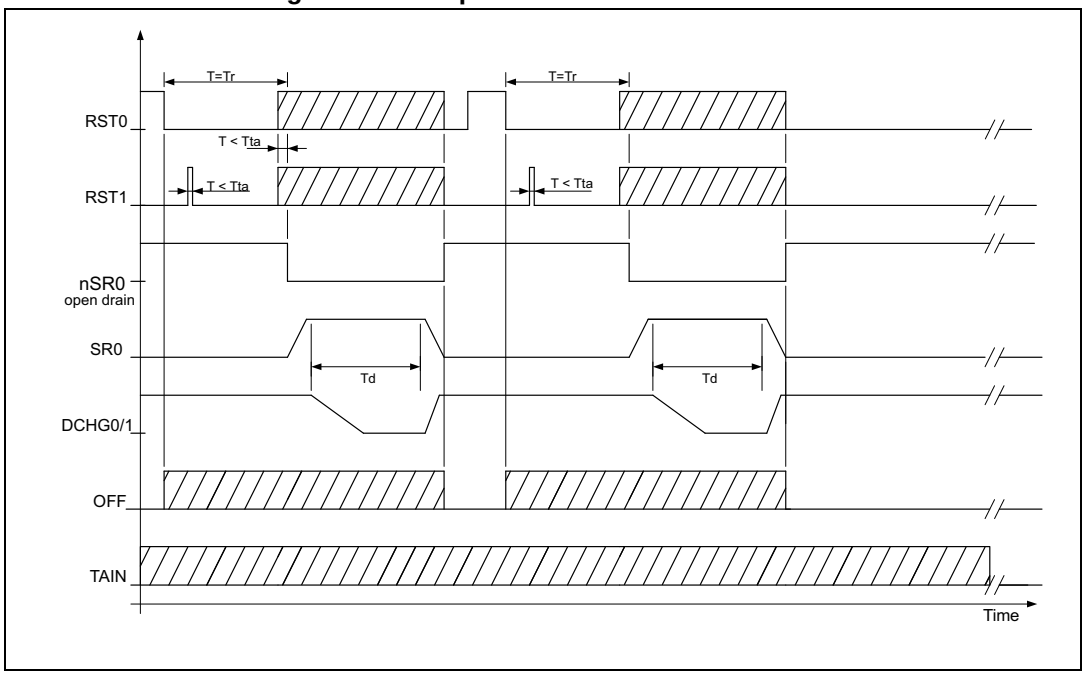
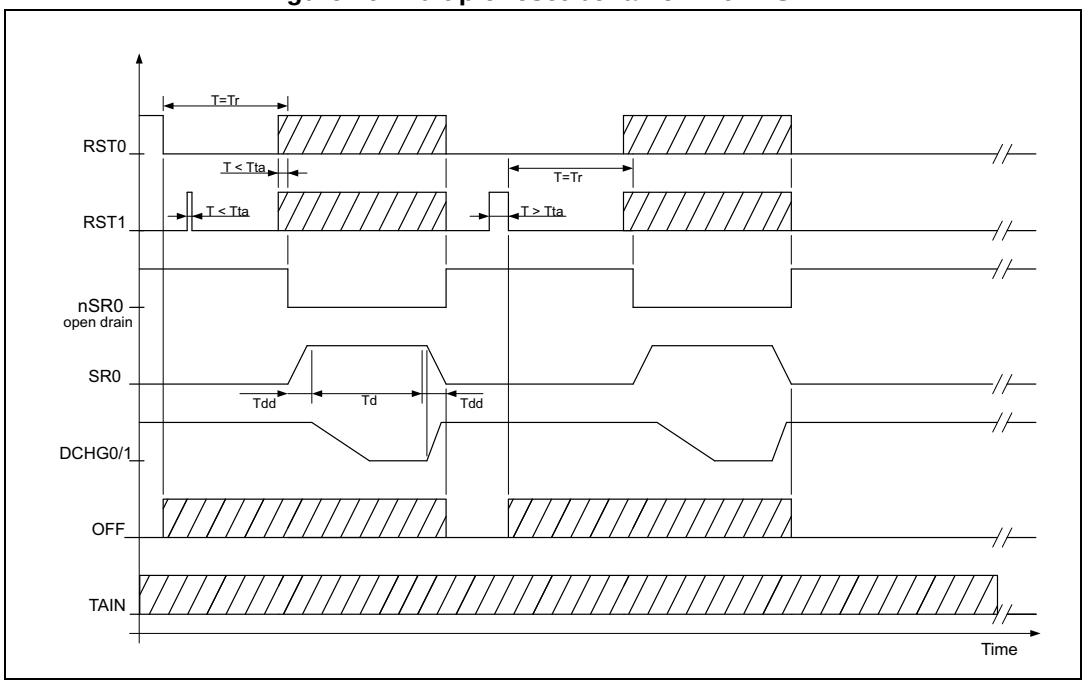


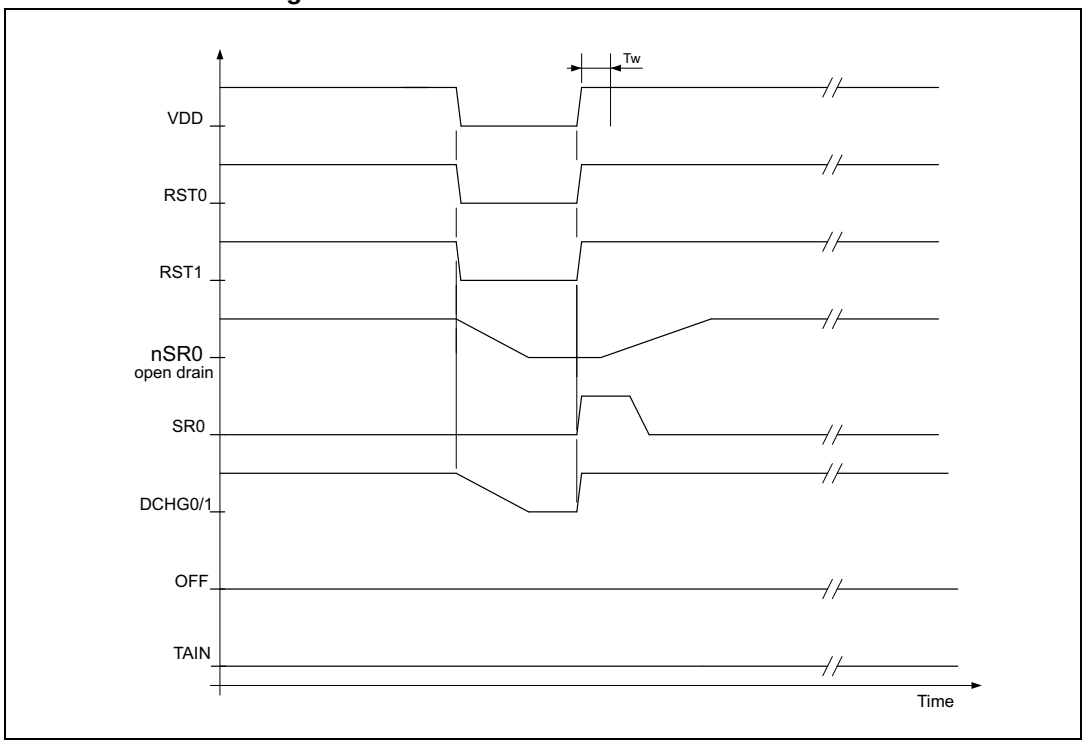
Figure 19. Multiple reset behavior with RST1



5.6 Power ON

For many reasons, batteries can be removed from smartphones. The STM6620S must correctly handle such a situation and must avoid inappropriate behavior. *Figure 20* shows the behavior of the STM6620S when a battery is removed and replaced with a disconnected charger (TAIN at a low level).

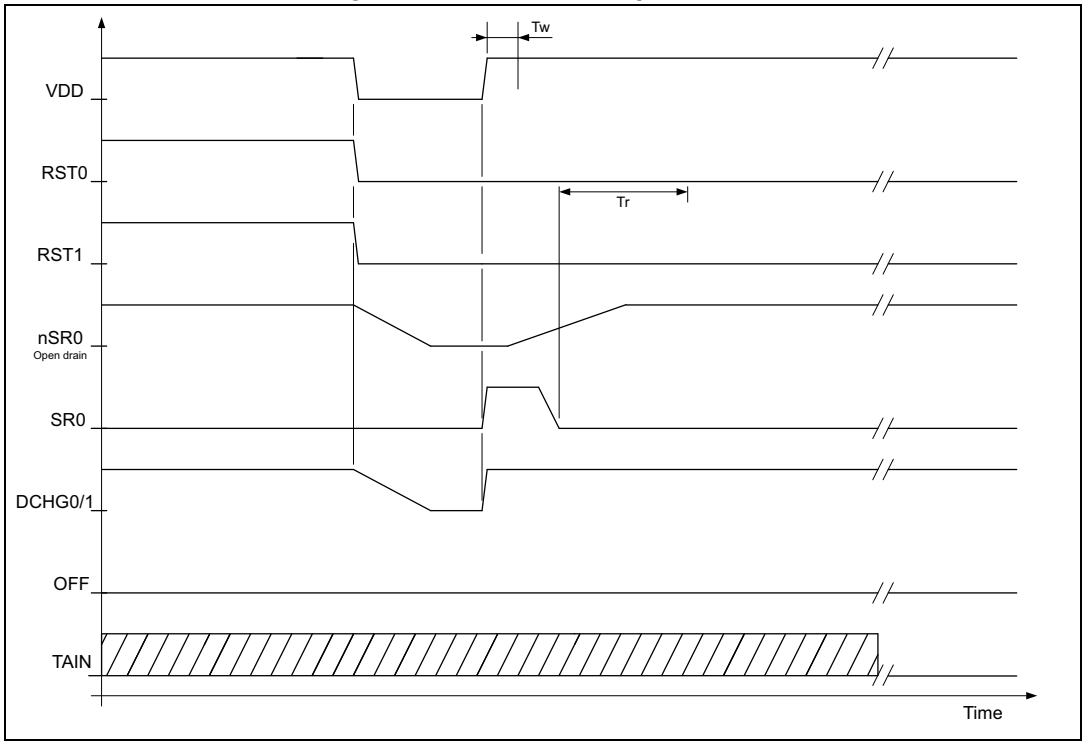
Figure 20. Power ON with TAIN at a low level



If the supply voltage is high (12 V for instance), the parasitic capacitor of the external PMOS can transmit this high voltage to the STM6620S through the resistor Rpmos. This phenomenon is linked to the rise time of the supply voltage. It is then recommended to use a supply voltage rise time above 3 ms to ensure that the AMR are fully respected on the SR0 pin.

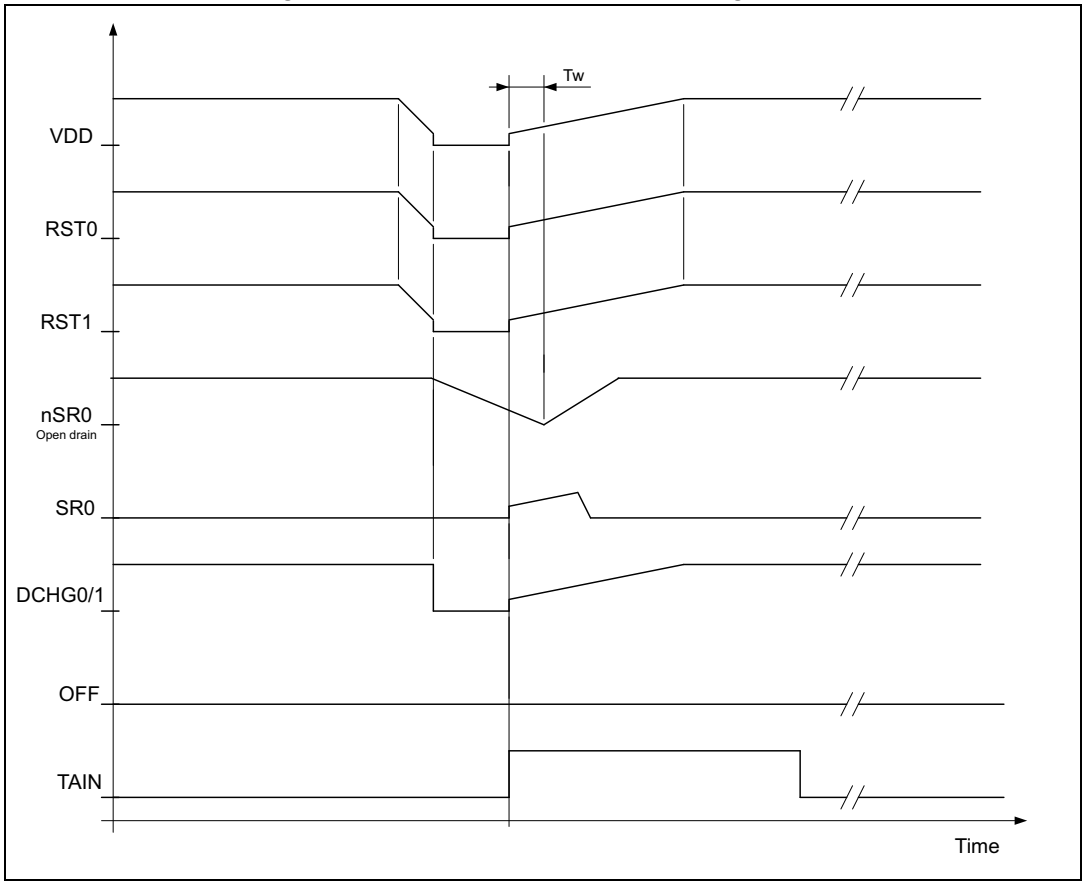
A reset does not occur immediately after power ON even if conditions are ideal (see *Figure 21*).

Figure 21. No reset after power ON



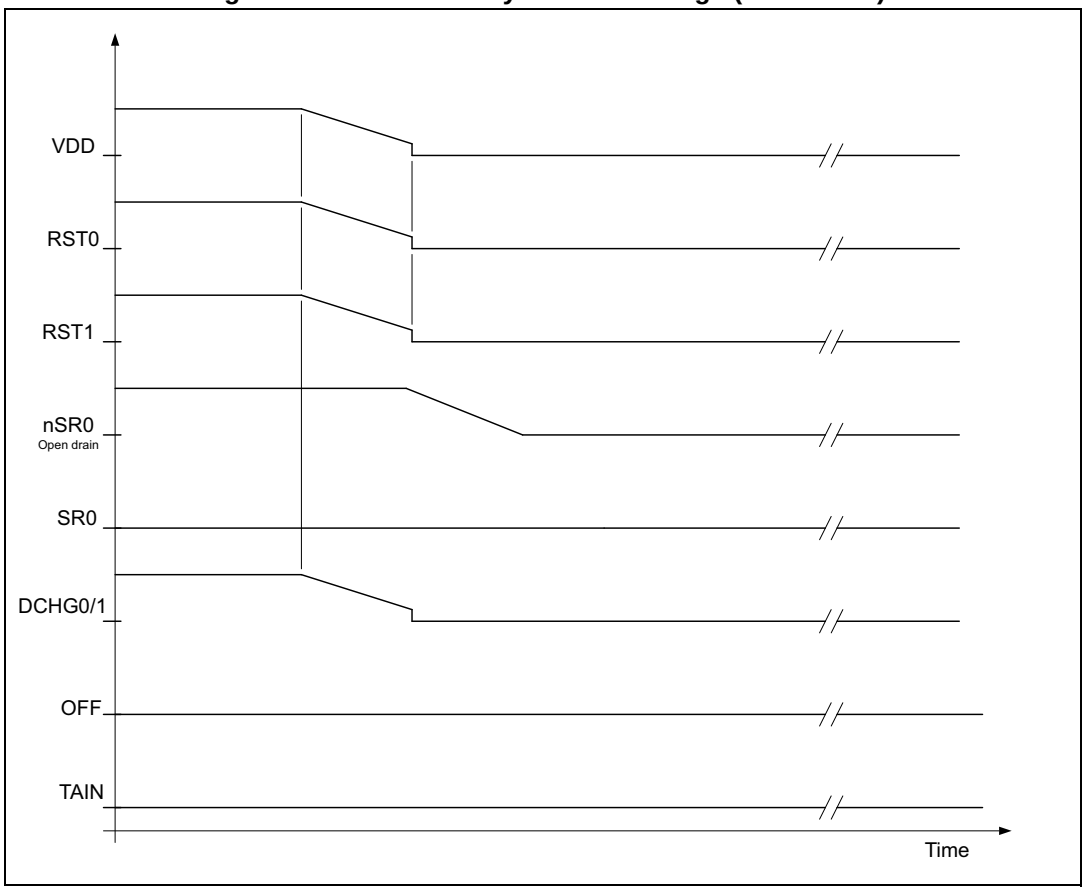
Power ON can occur with a charger (TAIN at a high level). *Figure 22* shows the behavior of the STM6620S in such a case.

Figure 22. Power ON with TAIN at a high level



When a battery is depleted and no charger inserted (TAIN at a low level), V_{DD} reaches cut OFF voltage and is set to 0 V. The behavior of the STM6620S in such a case is shown in *Figure 23*.

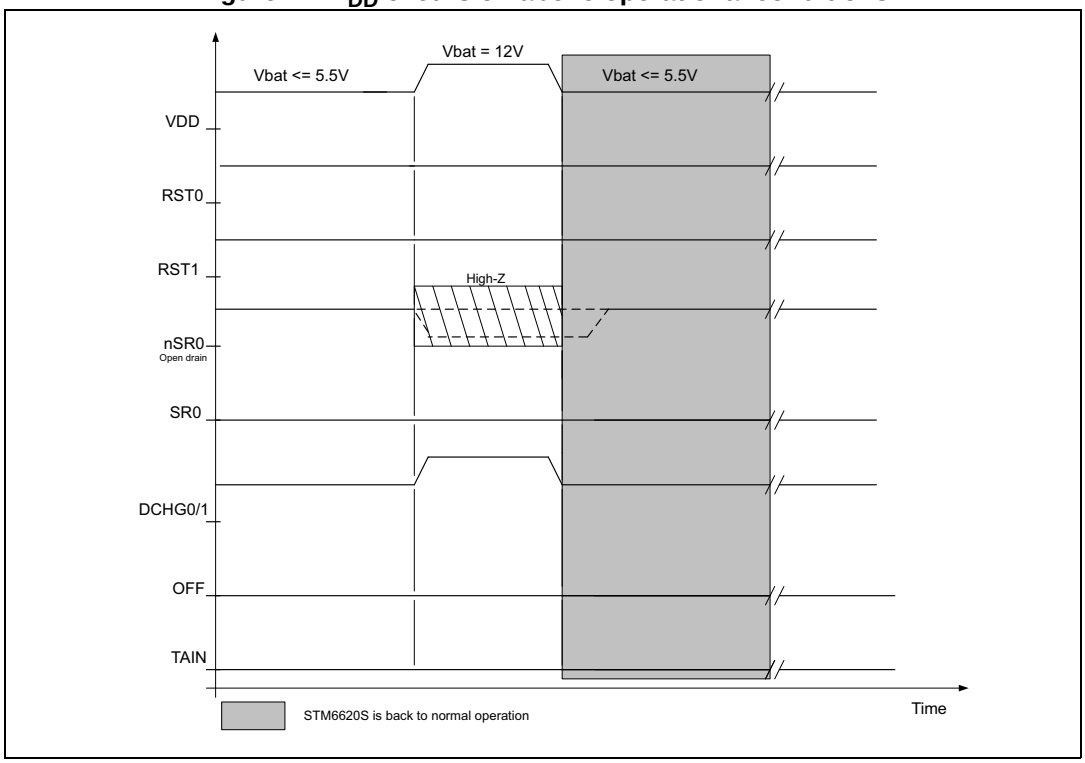
Figure 23. VDD at battery cut OFF voltage (TAIN = low)



5.7 VDD above operating conditions

According to *Table 3*, the STM6620S operates normally in the range 2.2 V to 5.5 V applied on the V_{DD} pin. Although V_{DD} can reach 12 V absolute maximum rating as per *Table 2*, the STM6620S is not operational above 5.5 V applied on V_{DD} as shown in *Figure 24*. This is because an internal LDO protects the STM6620S circuitry by limiting the internal supply voltage to a maximum operating voltage of 5.5 V. With $V_{DD} < 5.5$ V, the internal LDO voltage is equal to V_{DD}. With $5.5\ V < V_{DD} < 12$ V, the LDO limits the internal voltage to 5.5 V.

Figure 24. V_{DD} excursion above operational conditions



6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

6.1 QFN10 package information

Figure 25. QFN10 package outline

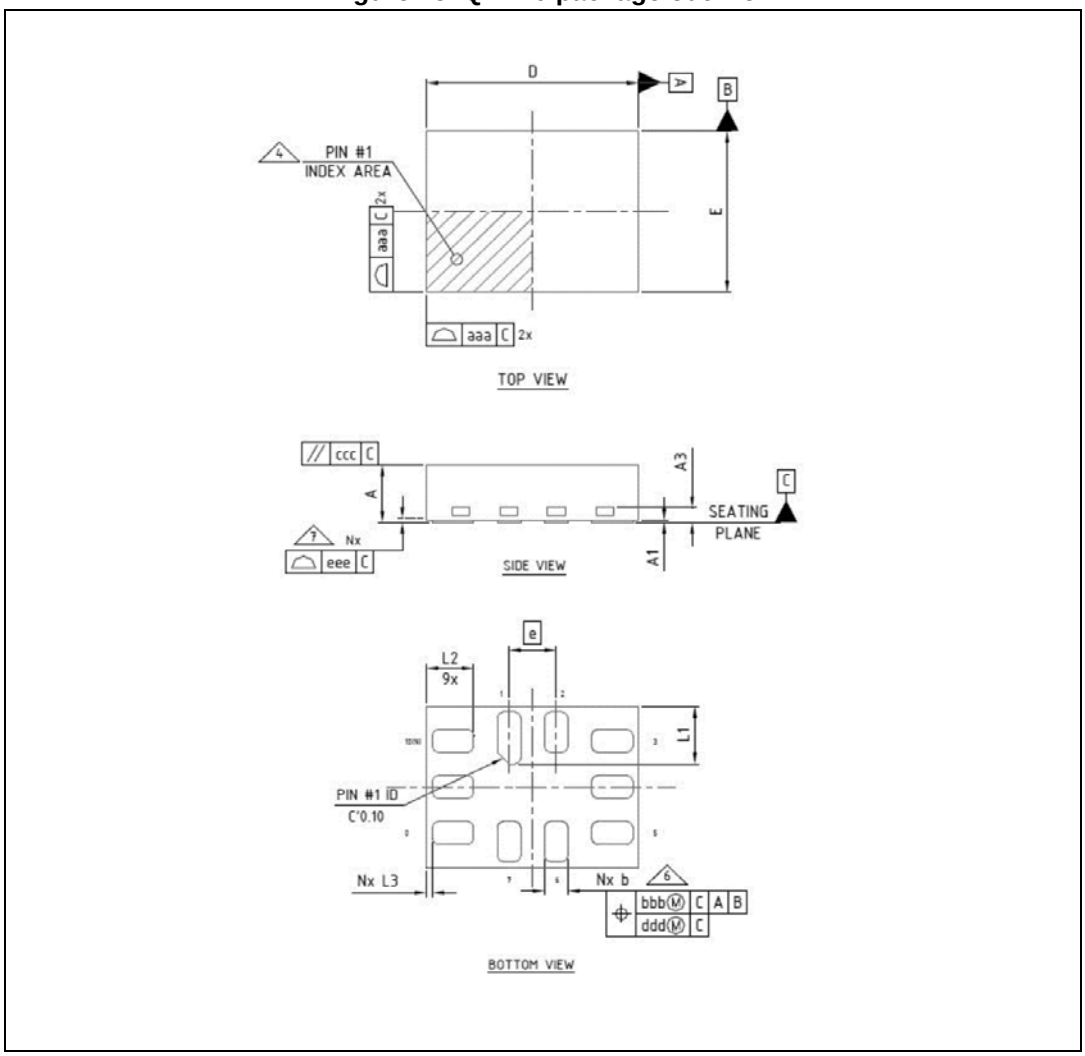
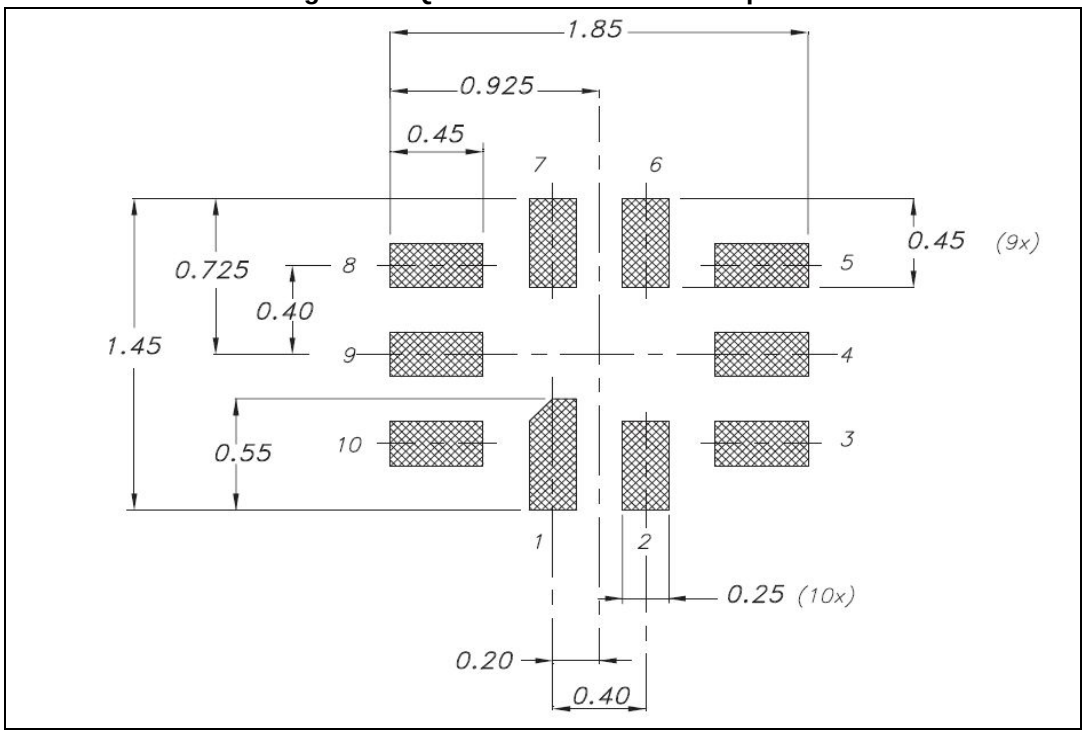


Table 5. QFN10 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.45	0.50	0.55	0.018	0.020	0.022
A1	0	0.02	0.05	0	0.001	0.002
A3		0.12			0.005	
b	0.15	0.20	0.25	0.006	0.008	0.010
D	1.75	1.80	1.85	0.069	0.071	0.073
E	1.35	1.40	1.45	0.053	0.055	0.057
e		0.40			0.016	
L1	0.45	0.50	0.55	0.018	0.020	0.022
L2	0.35	0.40	0.45	0.014	0.016	0.018
L3		0.05			0.002	
aaa		0.05			0.002	
bbb		0.07			0.003	
ccc		0.10			0.004	
ddd		0.05			0.002	
eee		0.08			0.003	

Figure 26. QFN10 recommended footprint



7 Ordering information

Table 6. Order code

Order code	Smart Reset™ delay	Discharge time	Package	Packing	Marking
STM6620SAAQT	8 s	200 ms	QFN10 1.8x1.4x0.5	Tape and reel	SAA
STM6620SABQT		300 ms			SAB
STM6620SACQT		400 ms			SAC
STM6620SADQT		600 ms			SAD
STM6620SBAQT	10 s	200 ms			SBA
STM6620SBBQT		300 ms			SBB
STM6620SBCQT		400 ms			SBC
STM6620SBDQT		600 ms			SBD
STM6620SCAQT	12 s	200 ms			SCA
STM6620SCBQT		300 ms			SCB
STM6620SCCQT		400 ms			SCC
STM6620SCDQT		600 ms			SCD
STM6620SDAQT	16 s	200 ms			SDA
STM6620SDBQT		300 ms			SDB
STM6620SDCQT		400 ms			SDC
STM6620SDDQT		600 ms			SDD

8 Revision history

Table 7. Document revision history

Date	Revision	Changes
26-Jan-2018	1	Initial release.
09-Nov-2021	2	First public release.