STMUX3040

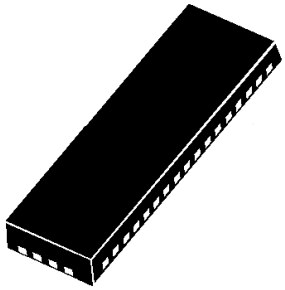
Octal SPDT high bandwidth signal switch

Features

- Supports PCIExpress signaling at 2.5Gbps
- Supports 3.0Gbps generic data rate
- Octal SPDT switch to support 2 PCI lanes
- Low Ron: 5.5Ω typical
- Internal voltage regulator
- V_{CC} operating range
  - 1.65 - 2.0V (Internal regulator bypassed)
  - 2.7 - 3.6V (Internal regulator active)
- Low current consumption: 150µA
- ESD HBM model : 2kV
- Channel on capacitance: 6pF typical
- Switching time speed: 9ns
- Near to zero propagation delay: 250ps
- Bandwidth: -3dB at 1200MHz
- Low crosstalk: -20dB at 1200MHz
- Bit to bit skew: 50 ps typical
- Data and control inputs provide undershoot clamp diode
- Wide bandwidth minimizes skew and jitter
- Hot insertion capable
- Supports bi-directional operation
- -40°C to 85°C operating temperature range

Applications

- Workstation
- PC and Notebook



TQFN42

Description

The STMUX3040 is a differential Single Pole Double Throw (SPDT) 2 to 1, low Ron, bi-directional signal switch designed for PCIe signaling.

It is designed for very low cross-talk, low bit-to-bit skew, high channel-to-channel noise isolation and low I/O capacitance. The switch offers very little or practically no attenuation of the high speed signals at the outputs, thus preserving the signal integrity to pass stringent requirements.

Table 1. Device summary

Order code	Package	Packaging
STMUX3040	TQFN42	Tape and reel

Contents

1 Functional diagrams

Figure 1. Functional diagram (Switches)

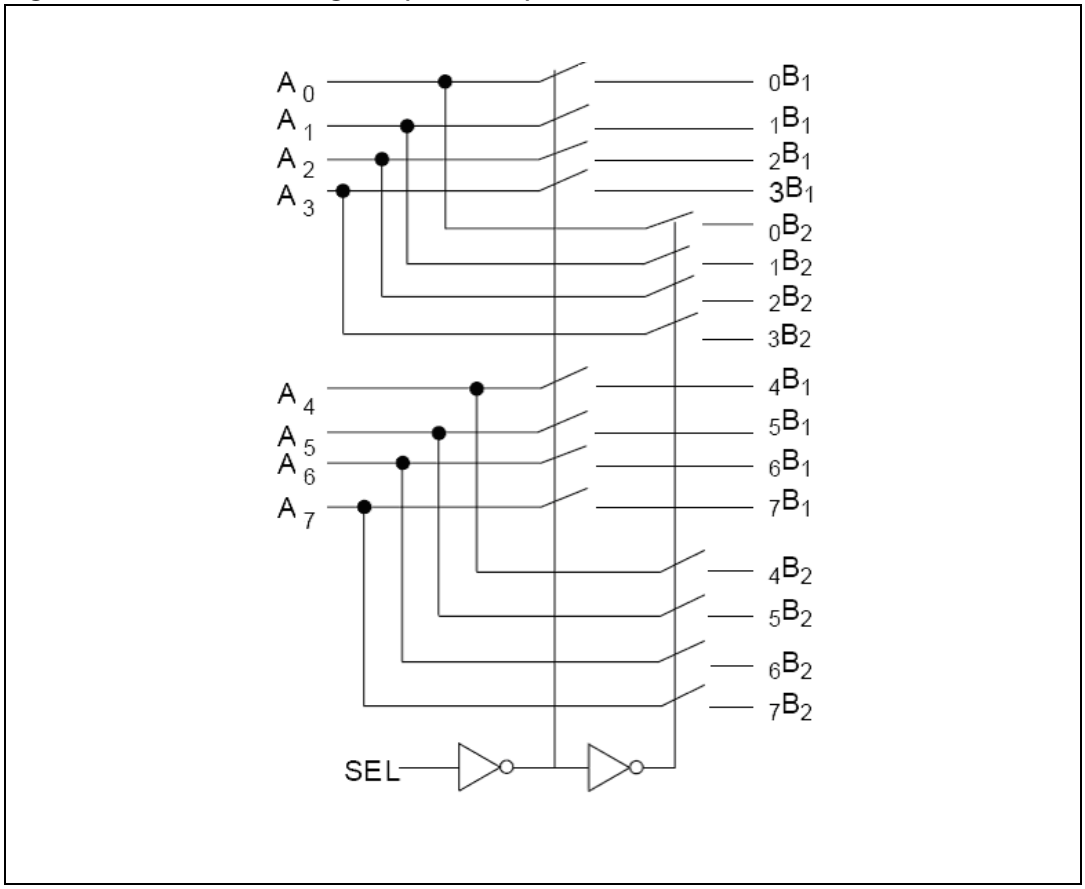
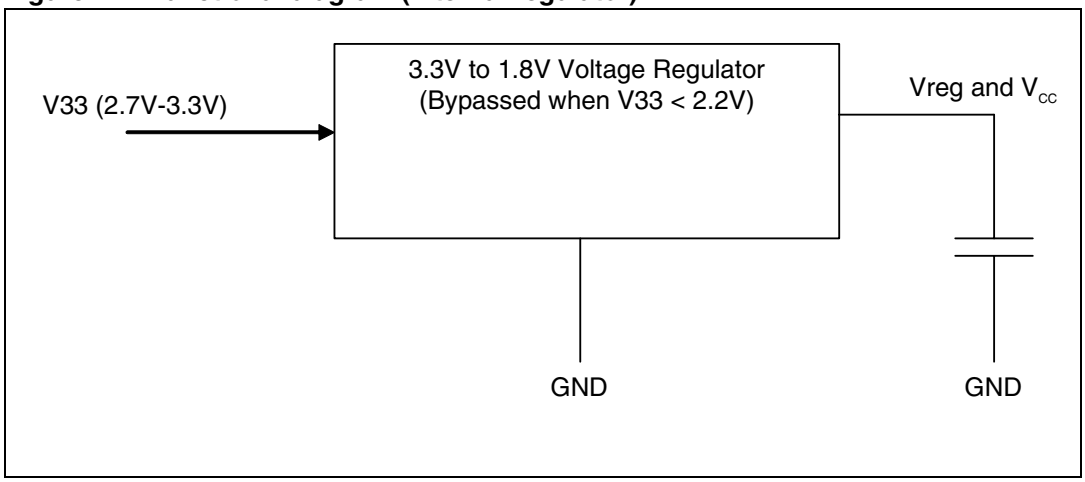


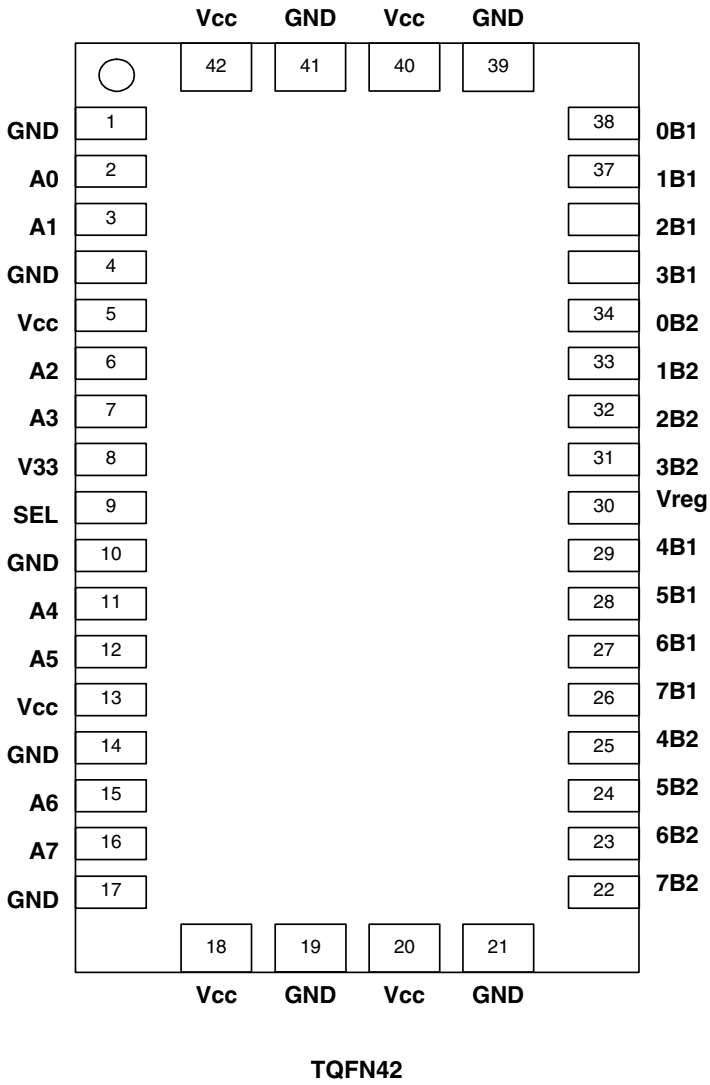
Figure 2. Functional diagram (Internal regulator)



2 Pin settings

2.1 Pin connection

Figure 3. Pin connection (Top through view)



TQFN42

2.2 Pin description

Table 2. Pin description

Pin number	Pin Name	Function
1	GND	Ground
2	A_0	Switch
3	A_1	Switch
4	GND	Ground
5	Vcc	1.65 - 2.0V Supply Tied to VREG if V33 > 2.2V
6	A_2	Switch
7	A_3	Switch
8	V33	2.7V – 3.3V (Internal Regulator Active) 1.65 – 2.0V (Internal Regulator Bypassed)
9	SEL	Switch select pin
10	GND	Ground
11	A_4	Switch
12	A_5	Switch
13	Vcc	1.65-2.0V Supply Tied to VREG if V33>2.2V
14	GND	Ground
15	A_6	Switch
16	A_7	Switch
17	GND	Ground
18	Vcc	1.65-2.0V Supply Tied to VREG if V33>2.2V
19	GND	Ground
20	Vcc	1.65-2.0V Supply Tied to VREG if V33>2.2V
21	GND	Ground
22	$_7B_2$	Switch
23	$_6B_2$	Switch
24	$_5B_2$	Switch
25	$_4B_2$	Switch
26	$_7B_1$	Switch
27	$_6B_1$	Switch
28	$_5B_1$	Switch

Table 2. Pin description (continued)

Pin number	Pin Name	Function
29	$_4B_1$	Switch
30	VREG	Output of internal regulator 22nF capacitor required here.
31	$_3B_2$	Switch
32	$_2B_2$	Switch
33	$_1B_2$	Switch
34	$_0B_2$	Switch
35	$_3B_1$	Switch
36	$_2B_1$	Switch
37	$_1B_1$	Switch
38	$_0B_1$	Switch
39	GND	Ground
40	Vcc	1.65-2.0V Supply Tied to V_{REG} if V33>2.2V
41	GND	Ground
42	Vcc	1.65-2.0V Supply Tied to V_{REG} if V33>2.2V

2.3 Device operation table

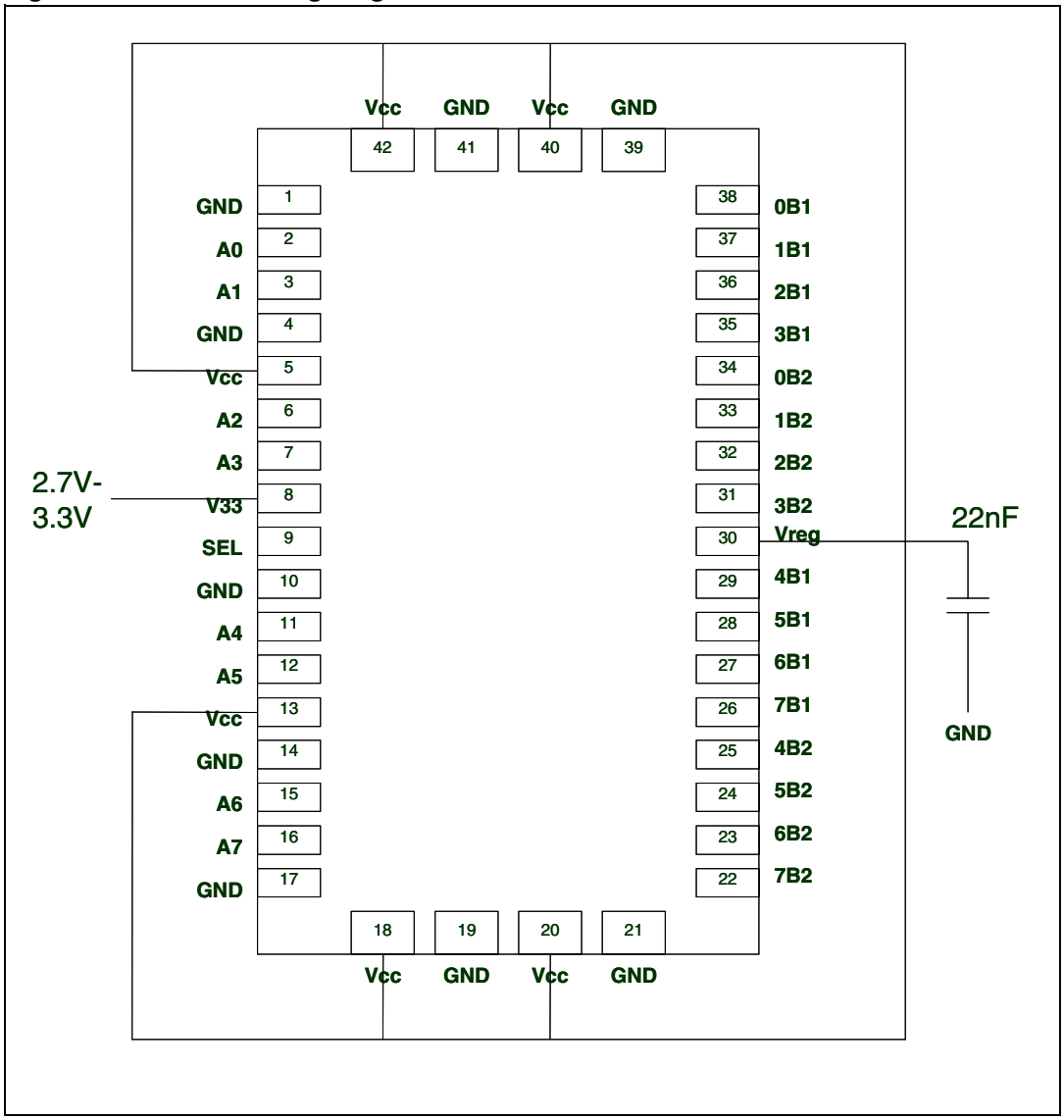
Table 3. Operation table

SEL	Function
L	A_N to $_NB_1$
H	A_N to $_NB_2$

3 Internal voltage regulator

STMUX3040 is integrated with an internal voltage regulator. The voltage regulator is activated when supply voltage to the Vreg pin is more than 2.7V. If the supply to V_{reg} is less than 2.2V, the regulator is bypassed.

Figure 4. Internal voltage regulator



When internal regulator is activated:

- V33 is used as supply input
- V_{reg} is used as output of the internal regulator, a 22nF capacitor should be connected from this pin to ground

When internal regulator is not used:

- V_{CC}, V33 and V_{reg} are all connected to 1.8V supply

4 Maximum rating

Stressing the device above the rating listed in the “Absolute Maximum Ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

4.1 Absolute maximum rating

Table 4. Absolute maximum rating

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage to Ground	-0.5 to +2.5	V
V_{33}	Supply voltage to internal regulator	-0.5 to +4.5	V
V_I	DC input voltage	-0.5 to Vcc (1)	V
V_{IC}	DC control input voltage	-0.5 to Vcc (1)	V
I_O	DC output current	120	mA
T_{STG}	Storage temperature	-65 to +150	°C
T_L	Lead temperature (10 sec)	300	°C

1. V_{CC} = 1.8V ± 10% in regulator mode

4.2 Thermal data

Table 5. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Thermal resistance junction-ambient	40.8	°C/W

5 Electrical specification

5.1 DC electrical characteristics

T_A = -40 to +85°C, V_{CC} = 1.8V ± 10%

Table 6. SEL Pin

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{IH}	HIGH level input voltage	High level guaranteed	0.65Vcc			V
V_{IL}	LOW level input voltage	Low level guaranteed	-0.5		0.35Vcc	V
V_{IK}	Clamp diode voltage	V_{CC} = 1.8V, I_{IN} = -18mA		-0.8	-1.2	V
I_{IH}	Input high current	V_{CC} = 1.8V, V_{IN} = V_{CC}			±5	µA
I_{IL}	Input low current	V_{CC} = 1.8V, V_{IN} = GND			±5	µA

Table 7. All signal switch pins

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_{IN}	Input leakage	V_{CC} = 1.8V, V_{IN} = V_{CC} All non-tested switches floating			1	uA
V_{IK}	Clamp diode voltage	V_{CC} = 1.8V, I_{IN} = -18mA		-0.8	-1.2	V
R_{ON}	Switch ON resistance (1)	V_{CC} = 1.8V, V_{IN} = 0.9 to V_{CC}, I_{IN} = -30mA		5.5	8.0	Ω
R_{FLAT}	ON resistance flatness (1) (2)	V_{CC} = 1.8V, V_{IN} = 0.9 to V_{CC}, I_{IN} = -30mA		1	1.3	Ω
ΔR_{ON}	ON resistance match between channels $\Delta R_{ON} = R_{ONMAX} - R_{ONMIN}$ (2) (3)	V_{CC} = 1.8V, V_{IN} = 0.9 to V_{CC}, I_{IN} = -30mA		0.5	1	Ω

1. Measured by voltage drop between channels at the indicated current through the switch.
2. Flatness is defined as the difference between the R_{ONMAX} and the R_{ONMIN} of the on resistance over the specified range on the same channel
3. ΔR_{ON} measured at the same V_{CC}, temperature and voltage level.

5.2 Capacitance

Table 8. Capacitance (T_A = 25°C, f = 1MHz)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
C_{OFF}	Port x0 to Port x1, Switch off	V_{IN} = 0V		4		pF
C_{ON}	Capacitance switch on	V_{IN} = 0V		6		pF

5.3 Power supply characteristics

Table 9. Power supply characteristics (T_A = -40 to +85 °C)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{CC}	Supply voltage (internal regulator inactive)		1.65	1.8	2.0	V
V33	Supply voltage (internal regulator active)		2.7	3.3	3.6	V
I_{CC}	Quiescent power supply current (Internal regulator inactive)	V_{CC} = 2.0 V, V_{IN} = V_{CC} or GND		150	500	µA
I_{CC}	Quiescent power supply current (Internal regulator active)	V33 = 3.3V, V_{IN} = 1.8V or GND		250	700	µA

5.4 Dynamic electrical characteristics

Table 10. Dynamic electrical characteristics (T_A = -40 to +85 °C, V_{CC} = 1.8V ± 10%)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
X_{TALK}	Non-adjacent channel Cross-talk	R_L = 100Ω, f = 300MHz			-30	dB
		R_L = 100Ω, f = 600MHz			-20	dB
		R_L = 100Ω, f = 1200MHz			-20	dB
O_{IRR}	Off Isolation	R_L = 100Ω, f = 300MHz			-35	dB
		R_L = 100Ω, f = 600MHz			-28	dB
		R_L = 100Ω, f = 1200MHz			-20	dB
D_R	Data rate per channel			3.0		Gbps
BW	Bandwidth	-3dB bandwidth	1200	1300		MHz

5.5 Dynamic switching characteristics

Table 11. Dynamic switching characteristics (T_A = -40 to +85 °C, V_{CC} = 1.8V ± 10%)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
t_{PD}	Propagation delay	V_{CC} = 1.65V - 2.0V		0.25		ns
t_{PZH}, t_{PZL}	Line enable time, SEL to x to x0 or x to x1	V_{CC} = 1.65V - 2.0V	0.5	6.5	9	ns
t_{PHZ}, t_{PLZ}	Line Disable Time, SEL to x to x0 or x to x1	V_{CC} = 1.65V - 2.0V	0.5	6.5	8.5	ns
$t_{SK(O)}$	Output skew between center port to any other port	V_{CC} = 1.65V - 2.0V		50	100	ps
$t_{SK(P)}$	Skew between opposite transition of the same output (t_{PHL} - t_{PLH})	V_{CC} = 1.65V - 2.0V		50	100	ps
t_{ON}	Switching delay	V_{CC} = 1.65V - 2.0V			50	ns
t_{OFF}	Switching delay	V_{CC} = 1.65V - 2.0V			30	ns

5.6 ESD performance

Table 12. ESD performance

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
ESD	IEC-61000-4-2	Air discharge (10 pulses)		±2		kV
		Contact discharge (10 pulses)		±2		kV

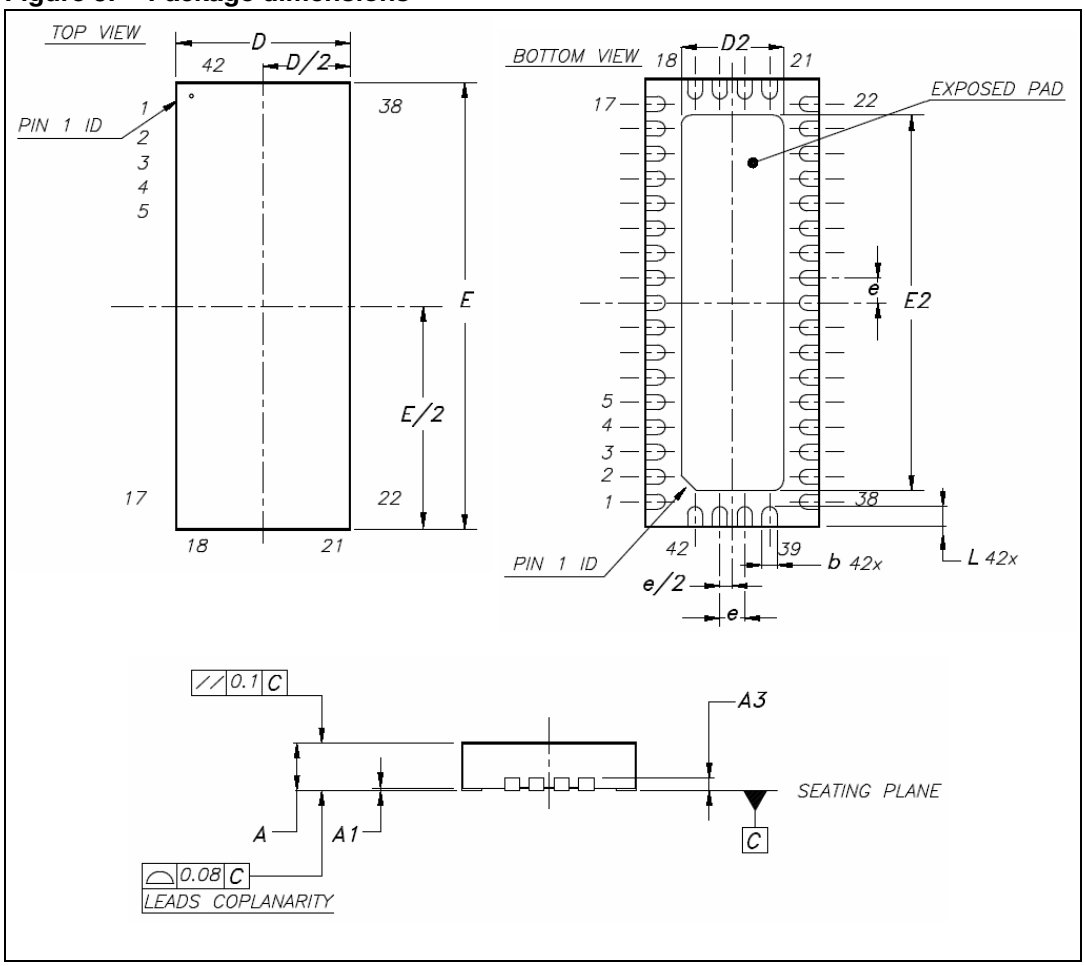
6 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

Table 13. TQFN42 mechanical data

Dim.	mm.		
	Min	Typ	Max
A	0.70	.075	0.80
A1	0	0.02	0.05
A3		0.20	
b	0.20	0.25	0.30
D	3.40	3.50	3.60
D2	2	2.05	2.10
E	8.90	9	9.10
E2	7.50	7.55	7.60
e		0.50	
L	0.30	0.40	0.50

Figure 5. Package dimensions



7 Revision history

Table 14. Revision history

Date	Revision	Changes
05-Jul-2007	1	Initial release

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