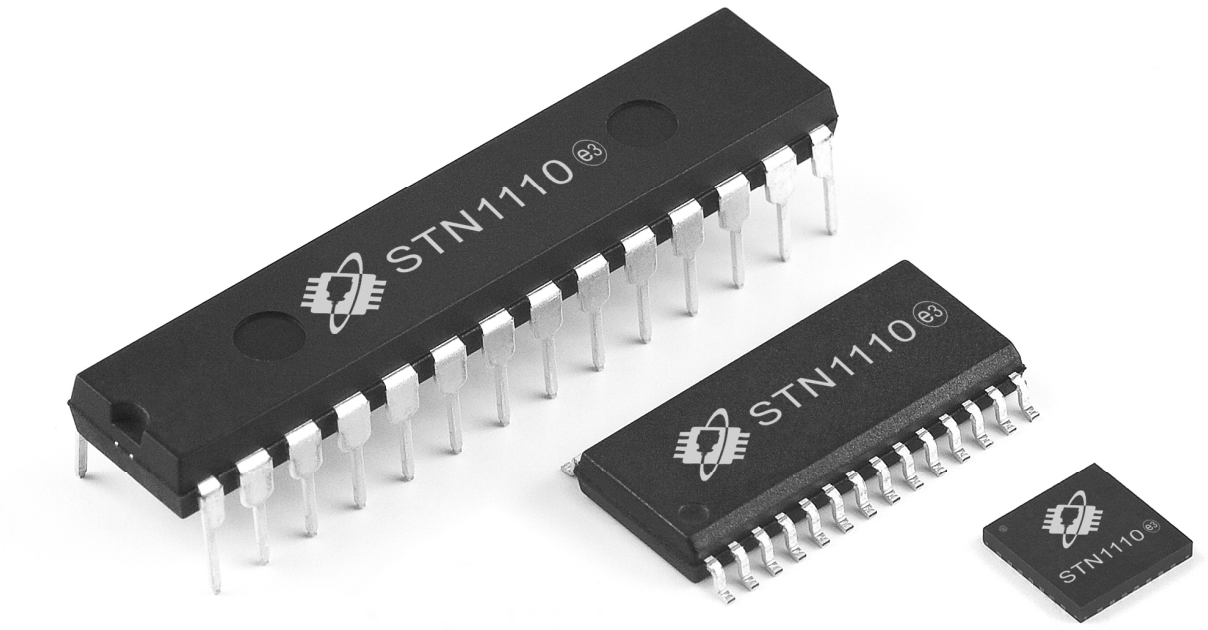
STN1110

Multiprotocol OBD to UART Interpreter
Datasheet



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1.0 Overview

This datasheet summarizes the features of the STN1110 device. It is not intended as a comprehensive reference source. To complement the information in this datasheet refer to the **"STN1100 Family Reference and Programming Manual"**. Please see the OBD Solutions website (www.obdsol.com) for the latest version of the STN1100 Family Reference Manual.

On-Board Diagnostics, Second Generation (OBD-II) is a set of standards for implementing a computer based system to control emissions from vehicles. It was first introduced in the United States in 1994, and became a requirement on all 1996 and newer US vehicles. Other countries, including Canada, parts of the European Union, Japan, Australia, and Brazil adopted similar legislation. A large portion of the modern vehicle fleet supports OBD-II or one of its regional flavors (EOBD, JOBD, etc).

Among other things, OBD-II requires that each compliant vehicle be equipped with a standard diagnostic connector (DLC) and describes a standard way of communicating with the vehicle's computer, also known as the ECU (Electronic Control Unit).

A wealth of information can be obtained by tapping into the OBD bus, including the status of the malfunction indicator light (MIL), diagnostic trouble codes (DTCs), inspection and maintenance (I/M) information, freeze frames, VIN, hundreds of real-time parameters, and more.

The STN1110 integrated circuit is an OBD to UART interpreter that can be used to convert messages between any of the OBD-II protocols currently in use, and UART. It is fully compatible with the *de facto* industry standard ELM327 command set. Based on a 16-bit processor core, the STN1110 offers more features and better performance than any other ELM327 compatible IC.

2.0 Feature Highlights

- Fully **compatible with the ELM327** AT command set
- **Extended** ST **command set**
- **UART interface** (baud rates from 38 bps to 10 Mbps[1])
- Secure **bootloader** for easy firmware updates
- Support for **all legislated OBD-II protocols:**
  - ISO 15765-4 (CAN)
  - ISO 14230-4 (Keyword Protocol 2000)
  - ISO 9141-2 (Asian, European, Chrysler vehicles)
  - SAE J1850 VPW (GM vehicles)
  - SAE J1850 PWM (Ford vehicles)
- Support for **non-legislated OBD protocols:**
  - ISO 15765
  - ISO 11898 (raw CAN)
- Support for **SAE J1939 OBD protocol**
- Superior **automatic protocol detection** algorithm
- **Large memory buffer**
- Voltage input for **battery monitoring**
- Available in **SPDIP, SOIC** and **QFN-S** packages
- **RoHS** compliant

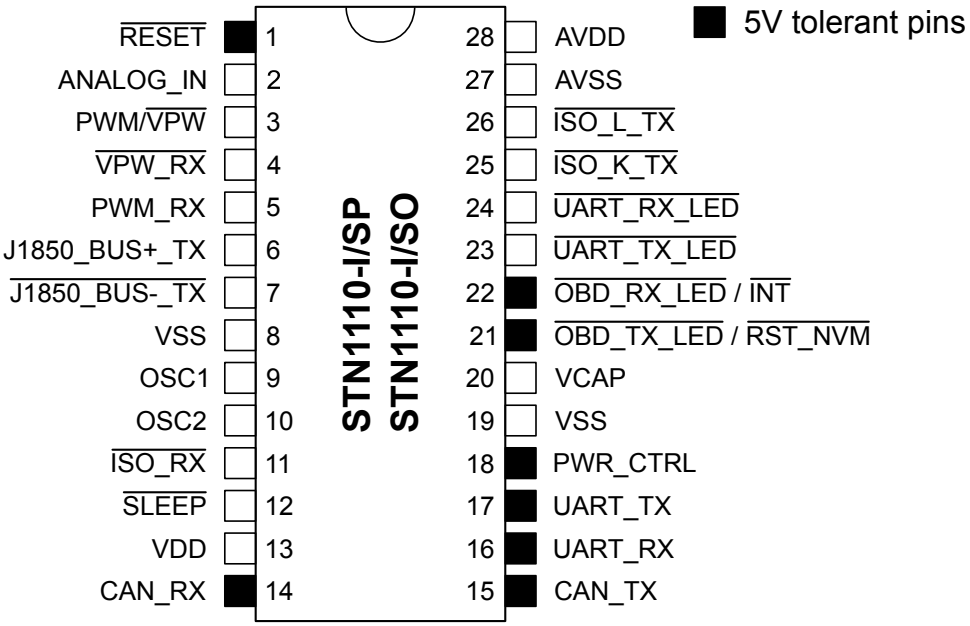
Note 1: Maximum theoretical baud rate. Actual maximum baud rate is application dependent and may be limited by driver hardware.

3.0 Typical Applications

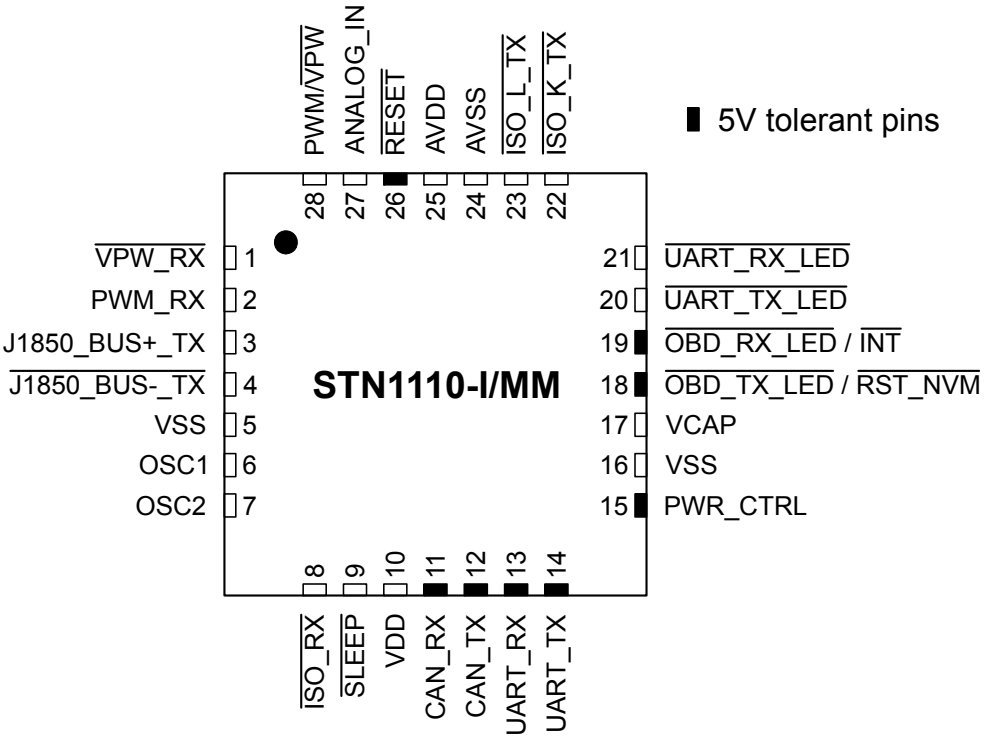
- Academic projects
- Automotive diagnostic scan tools and code readers
- Digital dashboards
- Fleet management and tracking applications
- OBD data loggers

4.0 Pinout

28-Pin SPDIP, SOIC



28-Pin QFN-S[(1)]



Note 1. The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.

4.1 Pinout Summary

Pin Number		Pin Name	Pin Type	Pin Description
SOIC SPDIP	QFN-S			
1	26	$\overline{\text{RESET}}$	I, 5V	Active low device reset input
2	27	ANALOG_IN	A	Analog voltage measurement input
3	28	PWM/$\overline{\text{VPW}}$	O	SAE J1850 PWM/VPW Bus+ voltage select output
4	1	$\overline{\text{VPW\_RX}}$	I	Active low J1850 VPW receive input
5	2	PWM_RX	I	SAE J1850 PWM receive input
6	3	J1850_BUS+_TX	O	SAE J1850 Bus+ transmit output
7	4	$\overline{\text{J1850\_BUS-\_TX}}$	O	Active low SAE J1850 Bus- transmit output
8	5	VSS	P	Ground reference for logic and I/O pins
9	6	OSC1	I	16.000 MHz oscillator crystal input
10	7	OSC2	O	16.000 MHz oscillator crystal output
11	8	$\overline{\text{ISO\_RX}}$	I	Active low ISO 9141/ISO 14230 K-line input
12	9	$\overline{\text{SLEEP}}$	I	External sleep control input
13	10	VDD	P	Positive supply for logic and I/O pins
14	11	CAN_RX	I, 5V	CAN receive input
15	12	CAN_TX	OD, 5V	CAN transmit output
16	13	UART_RX	I, 5V	UART receive input
17	14	UART_TX	OD, 5V	UART transmit output
18	15	PWR_CTRL	OD, 5V	External power control output
19	16	VSS	P	Ground reference for logic and I/O pins
20	17	VCAP	P	CPU logic filter capacitor connection
21	18	$\overline{\text{OBD\_TX\_LED}}$ / $\overline{\text{RST\_NVM}}$	OD/I, 5V	Active low OBD transmit activity LED output *and* active low input to reset non-volatile settings to factory defaults
22	19	$\overline{\text{OBD\_RX\_LED}}$ / $\overline{\text{INT}}$	OD/O, 5V	Active low OBD receive activity LED *or* interrupt output
23	20	$\overline{\text{UART\_TX\_LED}}$	O	Active low UART transmit activity LED output
24	21	$\overline{\text{UART\_RX\_LED}}$	O	Active low UART transmit activity LED output
25	22	$\overline{\text{ISO\_K\_TX}}$	O	Active low ISO 9141/ISO 14230 K-line output
26	23	$\overline{\text{ISO\_L\_TX}}$	O	Active low ISO 9141/ISO 14230 L-line output
27	24	AVSS	P	Analog ground reference
28	25	AVDD	P	Analog positive supply

Legend: I – Schmitt trigger input with CMOS levels; A – analog input; O – digital output; OD – open drain output; 5V – 5 volt tolerant pin; P – power pin

4.2 Detailed Pin Descriptions

$\overline{\text{RESET}}$

Device reset input. A logic low pulse (min 2 µs) on this pin will reset the device. Apply a continuous logic low to hold the device in reset. If your circuit does not use this functionality, connect this pin to VDD.

ANALOG_IN

Analog voltage measurement input (AVDD max). By default, this input is calibrated for an external 62kΩ/10kΩ voltage divider connected to battery positive. Connect to AVSS if unused.

PWM / $\overline{\text{VPW}}$

The firmware uses this pin to control the voltage level of the SAE J1850 PWM/VPW Bus+ supply. When the PWM protocol is selected, it outputs a logic high to switch the supply voltage to a nominal 5V. When the VPW protocol is selected, it outputs a logic low to switch the supply voltage to a nominal 8V. Leave unconnected if unused.

$\overline{\text{VPW\_RX}}$

Active low SAE J1850 VPW receive input. When the SAE J1850 Bus+ is in the recessive (low) state, this pin should be at a logic high level. When the SAE J1850 Bus+ is in the dominant (high) state, this pin should be at a logic low level. Pull up to VDD if unused.

PWM_RX

SAE J1850 PWM receive input. When the SAE J1850 bus is in the recessive state (Bus+ is low, Bus- is high), this pin should be at a logic low level. When the SAE J1850 bus is in the dominant (Bus+ is high) state, this pin should be at a logic high level. Pull up to VDD if unused.

J1850_BUS+_TX

SAE J1850 Bus+ transmit output. When the pin is high, Bus+ should be high (dominant). Leave unconnected if unused.

$\overline{\text{J1850\_BUS-\_TX}}$

Active low SAE J1850 Bus- transmit output. When the pin is high, Bus- should be low (dominant). Leave unconnected if unused.

VSS

Ground reference for logic and I/O pins.

OSC1, OSC2

16.000 MHz oscillator crystal connection.

$\overline{\text{ISO\_RX}}$

Active low ISO 9141/ISO 14230 K-line receive input. When K-line is high (recessive), this pin should be at a logic low level. Connect to VSS if unused.

$\overline{\text{SLEEP}}$

External sleep control input. When enabled in firmware, puts the device into low-power sleep mode. Polarity of this pin can be configured in firmware; default configuration is active low. Internal pull-up to VDD is enabled by default, but can be disabled in firmware. Leave unconnected if unused.

VDD

Positive 3.0 – 3.6V supply for logic and I/O pins.

CAN_RX

CAN receive input. Must be connected to a CAN transceiver IC. Compatible with +3.3V and +5V logic. Pull up to VDD if unused.

CAN_TX

CAN transmit output. Must be connected to a CAN transceiver IC. Open drain – requires a pull-up to VDD or +5V (12 mA max). Pull-up resistor value depends on CAN baud rates used and the trace length (higher resistor values can be used with lower baud rates and shorter traces); recommended value is 1 kΩ. Pull up to VDD via 100 kΩ resistor if unused.

UART_RX

UART receive input. Compatible with +3.3V and +5V logic.

UART_TX

UART transmit output. Open drain – requires a pull-up to VDD or +5V (4 mA max). Pull-up value depends on UART baud rate and the trace length (higher resistor values can be used with lower baud rates and shorter traces); typical value is 4.7 kΩ.

PWR_CTRL

External power control output. Used to switch external circuitry into low-power (sleep) state. Polarity can be configured in firmware; default configuration is active high (logic low = sleep mode). Open drain – requires a pull-up to VDD or +5V (12 mA max); be mindful of the fact that the pull-up will draw current in low-power state. Pull up to VDD via 100 kΩ resistor if unused.

VCAP

CPU logic filter capacitor connection. Must be connected to a low-ESR (< 5Ω) minimum 4.7 µF capacitor; typical value is 10 µF.

$\overline{\text{OBD\_TX\_LED}}$ / $\overline{\text{RST\_NVM}}$

Active low OBD transmit activity LED output (12 mA max) *and* active low input to reset NVM to factory defaults. Open drain – requires a pull-up to VDD or +5V (12 mA max) if not pulled up via an LED connection. Pull up to VDD if unused.

$\overline{\text{OBD\_RX\_LED}}$ / $\overline{\text{INT}}$

Active low OBD receive activity LED *or* interrupt output (12 mA max). Open drain by default (requires a pull-up to VDD or +5V when configured as interrupt); can be configured as a digital output. If unused, pull up to VDD or configure as digital output and leave unconnected.

$\overline{\text{UART\_TX\_LED}}$

Active low UART transmit activity LED output (4 mA max). Voltage on the anode of the LED must not exceed VDD + 0.3V. Leave unconnected if unused.

$\overline{\text{UART\_RX\_LED}}$

Active low UART transmit activity LED output (4 mA max). Voltage on the anode of the LED must not exceed VDD + 0.3V. Leave unconnected if unused.

$\overline{\text{ISO\_K\_TX}}$

Active low ISO 9141/ISO 14230 K-line output. When the pin is logic high, K-line should be low. Leave unconnected if unused.

$\overline{\text{ISO\_L\_TX}}$

Active low ISO 9141/ISO 14230 L-line output. When the pin is logic high, L-line should be low. Leave unconnected if unused.

AVSS

Analog ground reference. Must be connected to analog “clean” ground (between VSS – 0.3V and VSS + 0.3V) or VSS.

AVDD

Analog positive supply. Must be connected to VDD or an external voltage reference (between VDD - 0.3V or 3.0V, whichever is greater and VDD + 0.3V or 3.6V, whichever is lesser). AVDD may be decoupled from digital supply by connecting it to VDD via a 10 Ω resistor.

5.0 Guidelines for Getting Started with STN1110

5.1 Basic Connection Requirements

Getting started with the STN1110 IC requires attention to a minimal set of device pin connections before proceeding with development. The following is a list of pin names, which must always be connected:

- **VDD and both Vss** pins (see Section 5.2 "Decoupling Capacitors")
- **AVDD and AVss** pins (see Section 5.2 "Decoupling Capacitors" and Section 5.3 "AVDD and AVSS Pins")
- **VCAP** (see Section 5.4 "Internal Voltage Regulator Filter Capacitor")
- $\overline{\textbf{RESET}}$ pin (see Section 5.5 "Device Reset Pin")
- **OSC1 and OSC2** pins (see Section 5.6 "Oscillator Pins")
- $\overline{\textbf{RST\_NVM}}$ pin (see Section 5.7 "NVM Reset Input")
- **Open Drain Output Pull-ups** (see Section 5.8 "Open Drain Outputs")

5.2 Decoupling Capacitors

The use of decoupling capacitors on every pair of power supply pins, such as VDD, VSS and AVDD, AVSS is required. Consider the following criteria when using decoupling capacitors:

- **Value and type of capacitor:** Recommendation of 1 µF, 10-20V. This capacitor should be a low-ESR and have resonance frequency in the range of 20 MHz and higher. It is recommended that ceramic capacitors be used.
- **Placement on the printed circuit board:** The decoupling capacitors should be placed as close to the pins as possible. It is recommended to place the capacitors on the same side of the board as the device. If space is constricted, the capacitor can be placed on another layer on the PCB using a via; however, ensure that the trace length from the pin to the capacitor is within ¼" (6 mm) in length.
- **Handling high frequency noise:** If the board is experiencing high frequency noise, upward of tens of MHz, add a second ceramic-type capacitor in parallel to the above described decoupling capacitor. The value of the second capacitor can be in the range of 0.01 µF to 0.001 µF. Place this second capacitor next to the primary decoupling capacitor.
- **Maximizing performance:** On the board layout from the power supply circuit, run the power and return traces to the decoupling capacitors first, and then to the device pins. This ensures that the decoupling capacitors are first in the power chain. Equally important is to keep the trace length between the capacitor and the power pins to a minimum thereby reducing PCB track inductance.

5.2.1 Tank Capacitors

On boards with power traces running longer than six inches in length, it is suggested to use a tank capacitor for integrated circuits, including STN1110, to supply a local power source. The value of the tank capacitor should be determined based on the trace resistance that connects the power supply source to the device, and the maximum current drawn by the device in the application. In other words, select the tank capacitor so that it meets the acceptable voltage sag at the device. Typical values range from 4.7 µF to 47 µF.

5.3 AVDD and AVSS Pins

As a minimum, AVDD must be connected directly to VDD and AVSS must be connected to directly VSS.
It is recommended that AVDD be connected to to VDD via a 10 Ω resistor or a small (10 µH – 47 µH) inductor.
AVSS should be connected to the electrically cleanest ground net (plane). For best results, analog circuitry should have a separate ground plane with a point connection to VSS ground plane as close as possible to the AVSS pin.

5.4 Internal Voltage Regulator Filter Capacitor

A low-ESR (< 5 Ω) capacitor is required on the VCAP pin, which is used to stabilize the internal voltage regulator output voltage. The VCAP pin must not be connected to VDD, and must have a capacitor between 4.7 µF and 10 µF, 16V connected to ground. The type can be ceramic or tantalum. Refer to **Section 7.2 "Electrical Characteristics"** for additional information. The placement of this capacitor should be close to the VCAP pin. It is recommended that the trace length not exceed ¼" (6 mm).

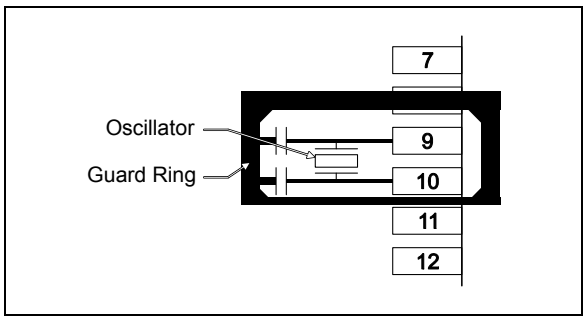
5.5 Device Reset Pin

$\overline{\text{RESET}}$ pin must be logic high for STN1110 to run. If this pin is not controlled by the host controller, it must be connected to VDD.
It is recommended to pull up $\overline{\text{RESET}}$ pin to VDD via a 10 kΩ resistor.

5.6 Oscillator Pins

The oscillator circuit should be placed on the same side of the board as the device. Also, place the oscillator circuit close to the oscillator pins, not exceeding one-half inch (12 mm) distance between them. The load capacitors should be placed next to the oscillator itself, on the same side of the board. Use a grounded copper pour around the oscillator circuit to isolate them from surrounding circuits. The grounded copper pour should be routed directly to the STN1110 ground. Do not run any signal traces or power traces inside the ground pour. Also, if using a two-sided board, avoid any traces on the other side of the board where the crystal is placed. A suggested layout is shown in Figure 1.

Figure 1 – Suggested Placement of the Oscillator Circuit



5.7 NVM Reset Input

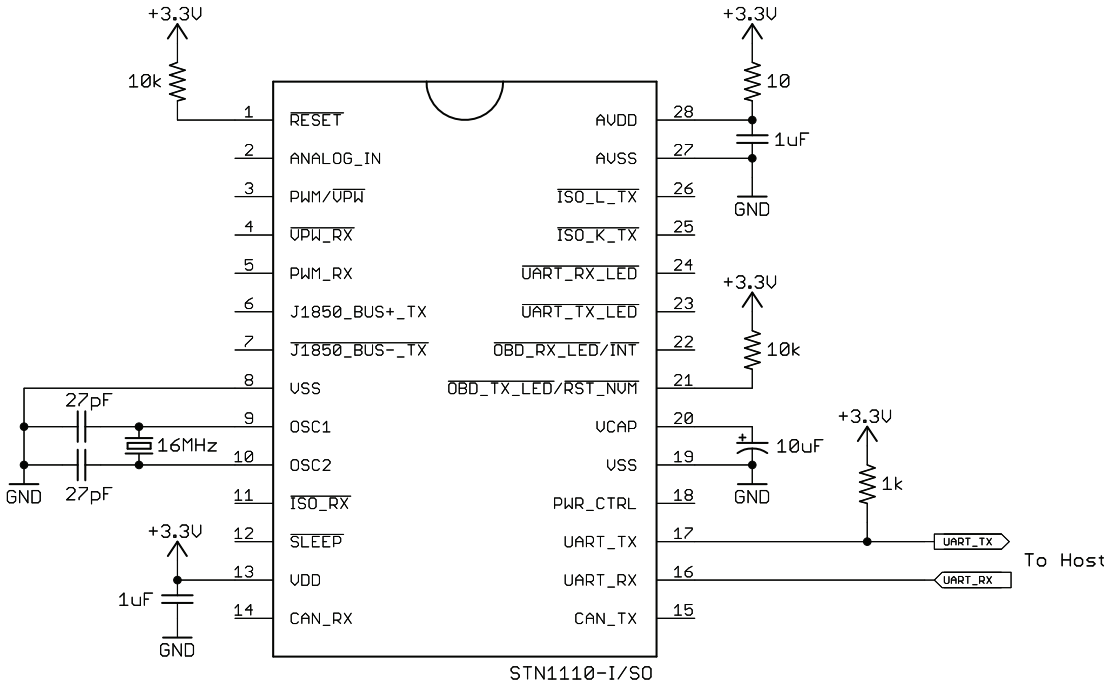
$\overline{\text{RST\_NVM}}$ pin must be pulled up to VDD via a 10 kΩ resistor for proper device operation.
If $\overline{\text{OBD\_TX\_LED}}$ / $\overline{\text{RST\_NVM}}$ pin is used to directly drive an LED, the pull-up is unnecessary.

5.8 Open Drain Outputs

All open drain outputs (as specified in section 4.1) that are in use must be pulled up to VDD or +5V.
Specifically, UART_TX pin must be pulled up in order to be able to communicate with the device.
See section 4.2 “Detailed Pin Descriptions” for more information.

6.0 Reference Schematics

6.1 Recommended Minimum Connection



6.2 Typical Configuration

Figure 2 – STN1110 IC

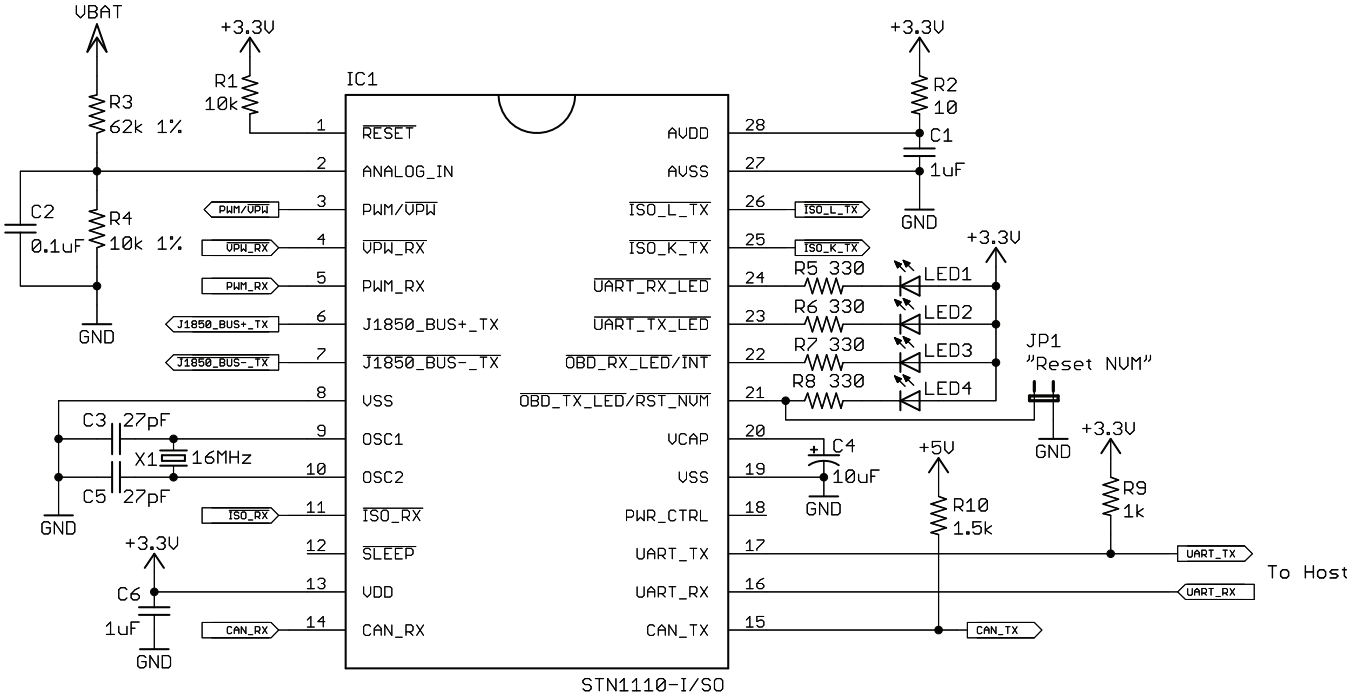


Figure 3 – OBD Connections

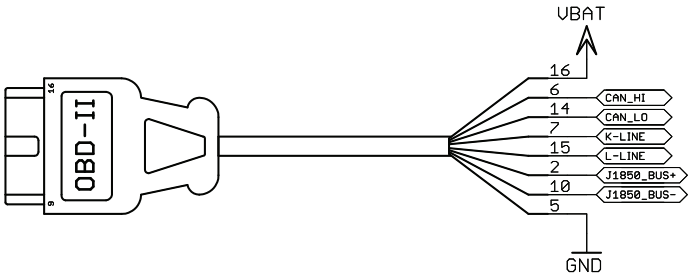
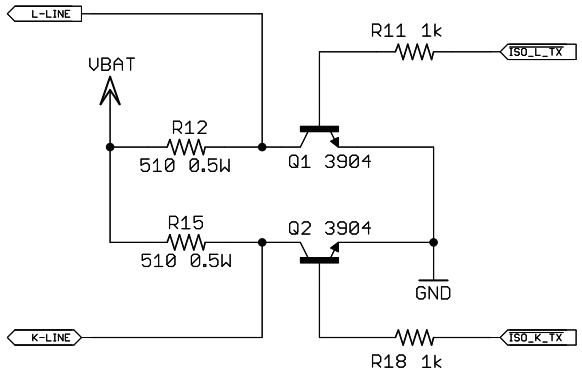


Figure 4 – ISO Transceiver



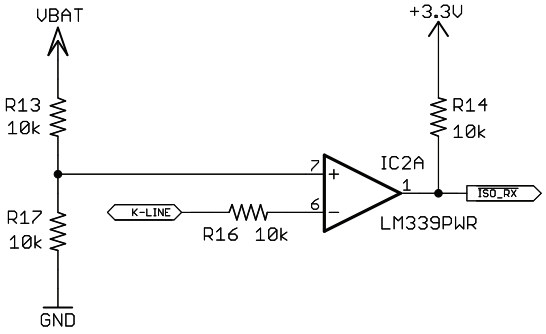


Figure 5 – CAN Transceiver

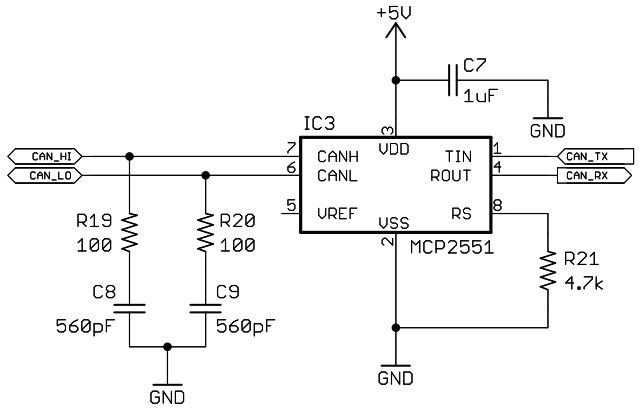


Figure 6 – J1850 Transceiver

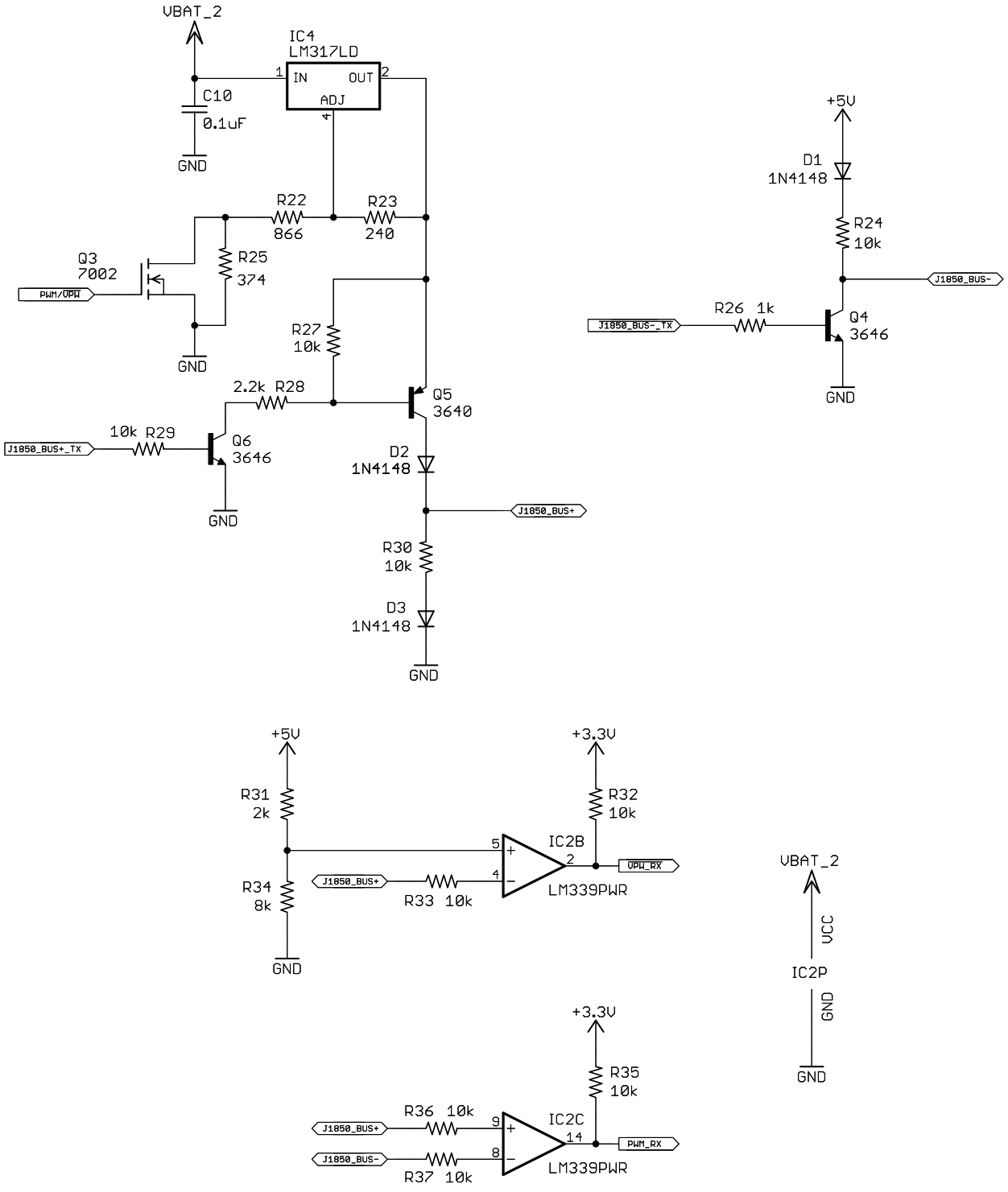
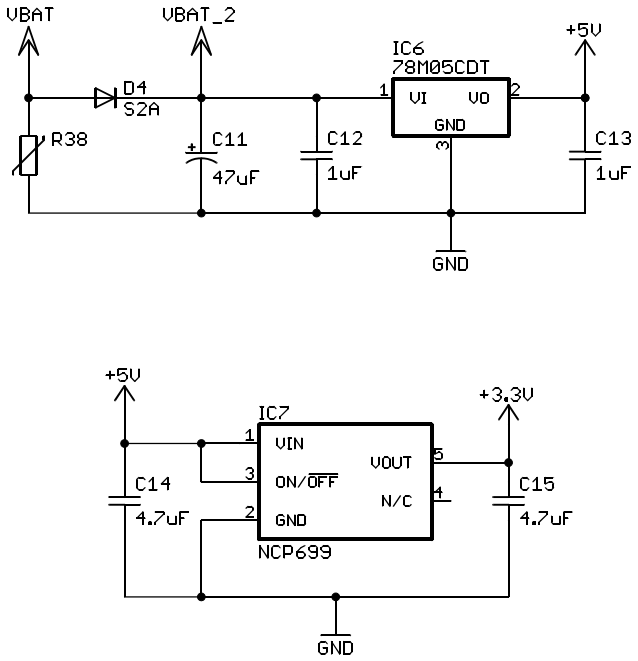


Figure 7 – Power Supplies



7.0 Electrical Characteristics

This section provides an overview of STN1110 electrical characteristics. Additional information will be provided in future revisions of this document as it becomes available.

STN1110 integrated circuit is based on PIC24HJ128GP502 device from Microchip Technology. For more detailed device specifications or clarification, refer to Microchip documentation, available at http://www.microchip.com.

7.1 Absolute Maximum Ratings (1)

Storage temperature ..... -65°C to +150°C
Ambient temperature under bias ..... -40°C to +125°C
Voltage on V_{DD} with respect to Vss ..... -0.3V to +4.0V
Voltage on any pin that is not 5V tolerant with respect to Vss(2) ..... -0.3V to (V_{DD} + 0.3V)
Voltage on any 5V tolerant pin with respect to Vss when V_{DD} ≥ 3.0V(2) ..... -0.3V to +5.6V
Voltage on any 5V tolerant pin with respect to Vss when V_{DD} < 3.0V(2) ..... -0.3V to (V_{DD} + 0.3V)
Maximum current sourced/sunk by PWM/$\overline{\text{VPW}}$, CAN_TX, UART_TX, PWR_CTRL, $\overline{\text{OBD\_TX\_LED}}$, and $\overline{\text{OBD\_RX\_LED}}$ / $\overline{\text{INT}}$ outputs ..... 12 mA
Maximum current sourced/sunk by any other output ..... 4 mA

Note 1. Stresses beyond those listed here can cause permanent damage to the device. These are stress ratings only, and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods can affect device reliability.

2. See "Pin Summary" section for the list of 5V tolerant pins.

7.2 Electrical Characteristics

Table 1: Thermal Operating Conditions

Sym	Characteristic	Min	Typ	Max	Units	Conditions
T_J	**Operating Junction Temperature**	-40	—	+125	°C	
T_A	**Operating Ambient Temperature**	-40	—	+85	°C	

Table 2: Power Specifications

Sym	Characteristic	Min	Typ(1)	Max	Units	Conditions
V_{DD}	**Supply Voltage**	3.0	3.3	3.6	V	
V_{POR}	**V_{DD} Start Voltage(2)** to ensure internal power-on reset (POR) signal	—	—	V_{SS}	V	
S_{VDD}	**V_{DD} Rise Rate(3)** to ensure internal power-on reset (POR) signal	0.03	—	—	V/ms	0–3.0V in 0.1s
AV_{DD}	**Analog Supply Voltage**	Greater of V_{DD} – 0.3 or 3.0	—	Lesser of V_{DD} + 0.3 or 3.6	V	
AV_{SS}	**Analog Ground Reference**	V_{SS} – 0.3	—	V_{SS} + 0.3	V	
V_{BOR}	**Brown-out Reset Voltage(4)**	2.40	—	2.55	V	

	on V_{DD} transition high-to-low					
I_{DD}	**Operating Current**[5]	—	60	90	mA	
I_{PD}	**Power-Down Current**[5]	—	30	500	µA	T_A = -40°C, T_A = +25°C
		—	130	750	µA	T_A = +85°C
C_{EFC}	**External Filter Capacitor** connected to V_{CAP} pin	4.7	10	—	µF	ESR < 5 Ω

Note
1. Data in Typ column is at 3.3V, 25°C, unless otherwise stated
2. V_{DD} voltage must remain at V_{SS} for a minimum of 200 µs to ensure POR
3. This spec must be met in order to ensure that a correct internal power-on reset (POR) occurs. It is easily achieved using most common types of supplies, but may be violated if a supply with slowly varying voltage is used, as may be obtained through direct connection to solar sells or some charge pump circuits.
4. This parameter is for design guidance only and is not tested in manufacturing
5. STN1110 device current only. Does not include any load currents

Table 3: I/O Pin DC Specifications

Sym	Characteristic	Min	Typ[1]	Max	Units	Conditions
V_{IL}	**Input Low Voltage**					
	CAN_RX pin	V_{SS}	—	0.3 V_{DD}	V	
	all other inputs	V_{SS}	—	0.2 V_{DD}	V	
V_{IH}	**Input High Voltage**					
	not 5V tolerant pins[2]	0.7 V_{DD}	—	V_{DD}	V	
	5V tolerant pins[2]	0.7 V_{DD}	—	5.5	V	
V_{IN}	**ANALOG_IN Input Voltage**	AV_{SS}	—	AV_{DD}	V	
V_{OL}	**Output Low Voltage**	—	—	0.4	V	I_{OL} = 2 mA, V_{DD} = 3.3V
V_{OH}	**Output High Voltage**	2.4	—	—	V	I_{OH} = -2.3 mA, V_{DD} = 3.3V
I_{PU}	**Internal Pull-up Current**	50	250	400	µA	V_{DD} = 3.3V, V_{PIN} = V_{SS}

Note
1. Data in Typ column is at 3.3V, 25°C, unless otherwise stated
2. See “Pin Summary” section for the list of 5V tolerant pins

Table 4: I/O Pin Timing Requirements

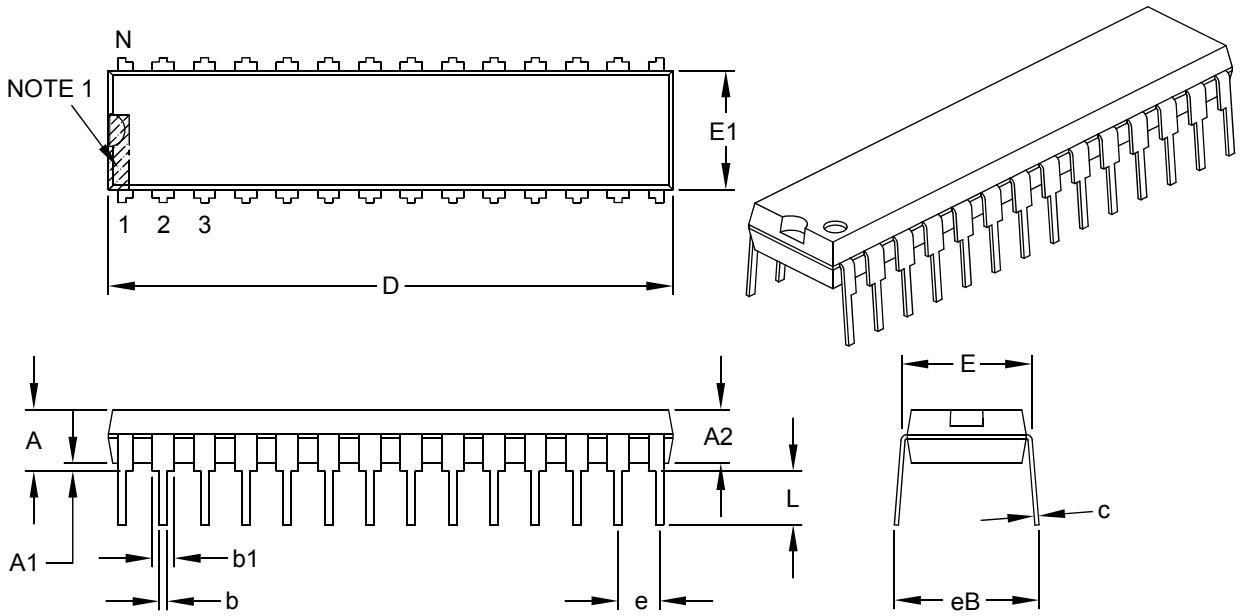
Sym	Characteristic	Min	Typ	Max	Units	Conditions
T_{RST}	**$\overline{\text{RESET}}$ Pulse Width** (low)	2	—	—	µs	
T_{UWM}	**Minimum UART Rx Pulse Width** required for wakeup (user settable)	—	20	—	ns	user setting < 15
		15	—	65534	µs	user setting ≥ 15
T_{STM}	**Minimum $\overline{\text{SLEEP}}$ Input Time** to stay high before wakeup (user settable)	—	15	—	µs	user setting = 0
		1	—	65534	ms	user setting > 0

8.0 Packaging Diagrams and Parameters

8.1 SPDIP (SP) Package

28-Lead Skinny Plastic Dual In-Line (SP) – 300 mil Body [SPDIP]

For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		28	
Pitch	e		.100 BSC	
Top to Seating Plane	A	—	—	.200
Molded Package Thickness	A2	.120	.135	.150
Base to Seating Plane	A1	.015	—	—
Shoulder to Shoulder Width	E	.290	.310	.335
Molded Package Width	E1	.240	.285	.295
Overall Length	D	1.345	1.365	1.400
Tip to Seating Plane	L	.110	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.040	.050	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	—	—	.430

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

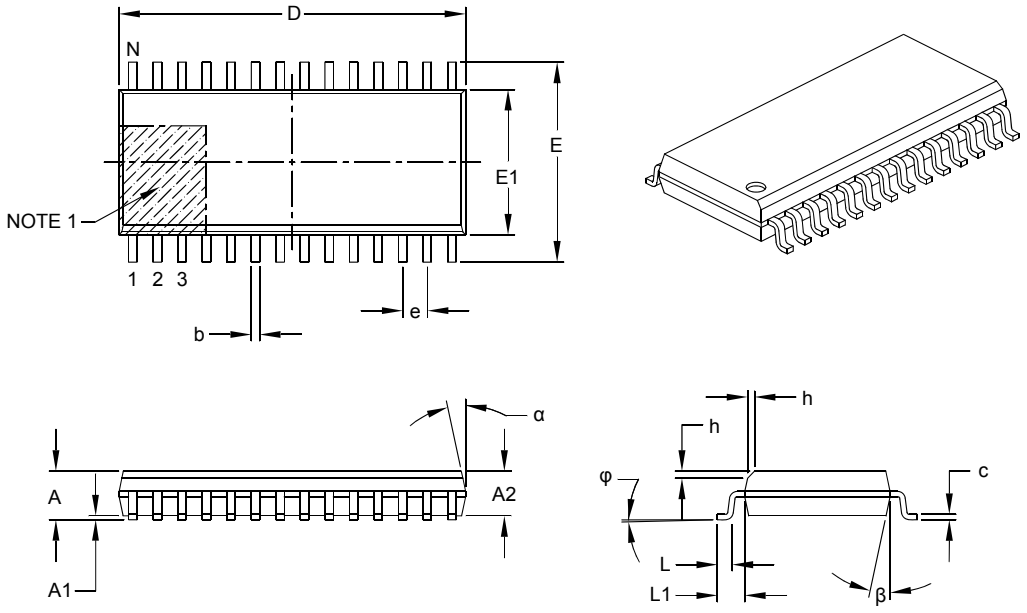
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-070B

8.2 SOIC 300mil (SO) Package

28-Lead Plastic Small Outline (SO) – Wide, 7.50 mm Body [SOIC]

For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		28	
Pitch	e		1.27 BSC	
Overall Height	A	—	—	2.65
Molded Package Thickness	A2	2.05	—	—
Standoff §	A1	0.10	—	0.30
Overall Width	E		10.30 BSC	
Molded Package Width	E1		7.50 BSC	
Overall Length	D		17.90 BSC	
Chamfer (optional)	h	0.25	—	0.75
Foot Length	L	0.40	—	1.27
Footprint	L1		1.40 REF	
Foot Angle Top	φ	0°	—	8°
Lead Thickness	c	0.18	—	0.33
Lead Width	b	0.31	—	0.51
Mold Draft Angle Top	α	5°	—	15°
Mold Draft Angle Bottom	β	5°	—	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

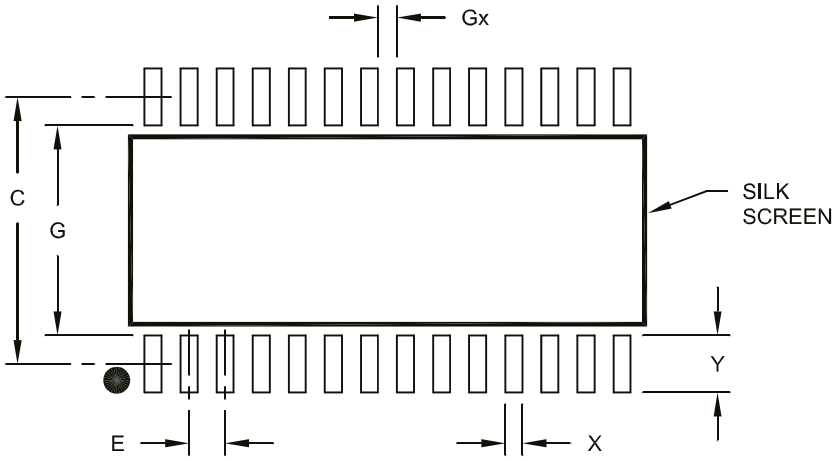
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-052B

8.3 SOIC 300mil (SO) Land Pattern

28-Lead Plastic Small Outline (SO) – Wide, 7.50 mm Body [SOIC]

For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pad Spacing	C		9.40	
Contact Pad Width (x28)	X			0.60
Contact Pad Length (x28)	Y			2.00
Distance Between Pads	Gx	0.67		
Distance Between Pads	G	7.40		

Notes:

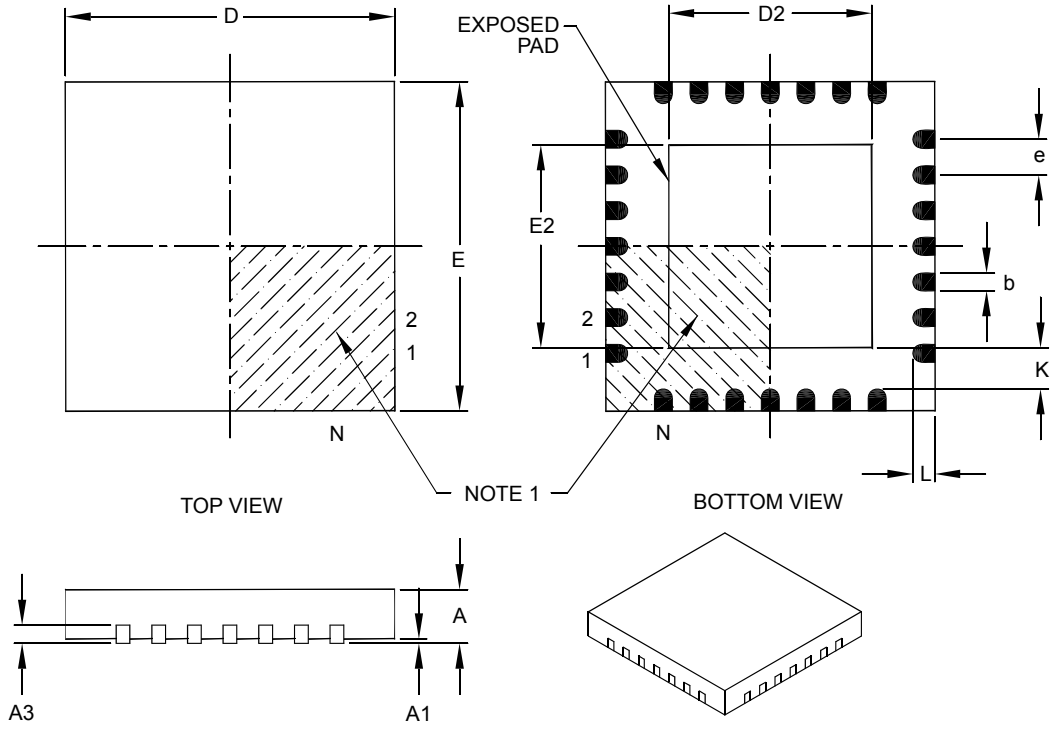
1. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2052A

8.4 QFN-S (MM) Package

28-Lead Plastic Quad Flat, No Lead Package (MM) – 6x6x0.9 mm Body [QFN-S] with 0.40 mm Contact Length

For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		28	
Pitch	e		0.65 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Width	E		6.00 BSC	
Exposed Pad Width	E2	3.65	3.70	4.70
Overall Length	D		6.00 BSC	
Exposed Pad Length	D2	3.65	3.70	4.70
Contact Width	b	0.23	0.38	0.43
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	—	—

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

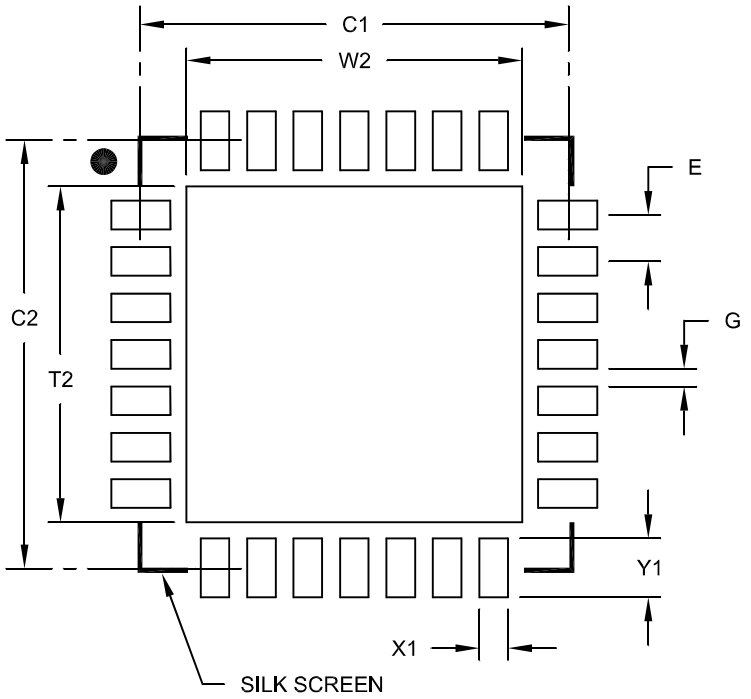
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-124B

8.5 QFN-S (MM) Land Pattern

28-Lead Plastic Quad Flat, No Lead Package (MM) – 6x6x0.9 mm Body [QFN-S] with 0.40 mm Contact Length

For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Optional Center Pad Width	W2			4.70
Optional Center Pad Length	T2			4.70
Contact Pad Spacing	C1		6.00	
Contact Pad Spacing	C2		6.00	
Contact Pad Width (x28)	X1			0.40
Contact Pad Length (x28)	Y1			0.85
Distance Between Pads	G	0.25		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2124

9.0 Ordering Information

T_A	Package		Part Number	SKU
-40°C to +85°C	SPDIP (SP)	Tube	STN1110-I/SP	365101
	SOIC (SO)	Tube	STN1110-I/SO	365111
	QFN-S (MM)	Tube	STN1110-I/MM	365121

Appendix A: Revision History

Revision A (October 22, 2010)

Initial release of this document.

Appendix B: Contact Information

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