STN1170

Multiprotocol OBD to UART Interpreter Datasheet

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1.0 Overview

This datasheet summarizes the features of the STN1170 device. It is not intended as a comprehensive reference source. To complement the information in this datasheet refer to the **"STN1100 Family Reference and Programming Manual".** Please see the OBD Solutions website (www.obdsol.com) for the latest version of the STN1100 Family Reference Manual.

The STN1170 is an OBD to UART interpreter IC designed to provide bi-directional half-duplex communication with the vehicle's On-Board Diagnostic system (OBD-II). It supports all legislated OBD-II protocols, as well as two proprietary networks: GM Single Wire CAN (GMLAN), and Ford Medium Speed CAN (MS CAN).

A wealth of information can be obtained by tapping into the OBD bus, including the status of the malfunction indicator light (MIL), diagnostic trouble codes (DTCs), inspection and maintenance (I/M) information, freeze frames, VIN, hundreds of real-time parameters, and more.

The STN1170 is fully compatible with the *de facto* industry standard ELM327 command set. Based on a 16-bit processor core, the STN1170 offers more features and better performance than any other ELM327 compatible IC.

2.0 Feature Highlights

- **Stable, field-tested firmware**
- Fully **compatible with the ELM327** AT command set
- Fully **backwards compatible with the STN1110** command set
- **Extended** ST **command set**
- **UART interface** (baud rates from 38 bps to 10 Mbps[1])
- Secure **bootloader** for easy firmware updates
- Support for **all legislated OBD-II protocols:**
  - o ISO 15765-4 (CAN)
  - o ISO 14230-4 (Keyword Protocol 2000)
  - o ISO 9141-2 (Asian, European, Chrysler vehicles)
  - o SAE J1850 VPW (GM vehicles)
  - o SAE J1850 PWM (Ford vehicles)
- Support for **non-legislated OBD protocols:**
  - o ISO 15765
  - o ISO 11898 (raw CAN)
  - o GMLAN Single Wire CAN (GMW3089)
  - o Ford Medium Speed CAN (MS CAN)
- Support for the heavy-duty **SAE J1939 OBD protocol**
- Superior **automatic protocol detection** algorithm
- **Large message buffer**
- Sophisticated **PowerSave Sleep/Wakeup Triggers**
- Available in **TQFP** and **QFN** packages
- **RoHS** compliant

Note 1: Maximum theoretical baud rate. Actual maximum baud rate is application dependent and may be limited by driver hardware.

3.0 Typical Applications

- Vehicle telematics
- Fleet management and tracking applications
- Usage-based insurance (UBI)
- OBD data loggers
- Automotive diagnostic scan tools and code readers
- Digital dashboards

4.0 Pinout

44-Pin TQFP

■ 5V tolerant pins

44-Pin QFN[(1)]

■ 5V tolerant pins
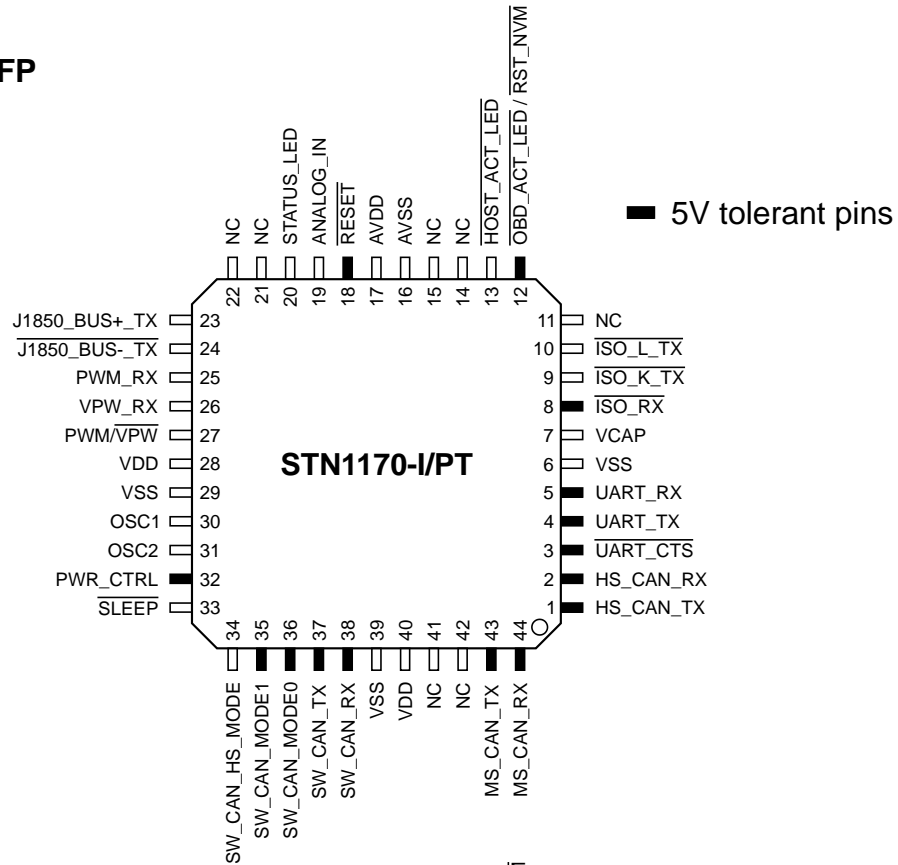
Note   1. The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to Vss externally.

4.1 Pinout Summary

Table 1: Pinout Summary

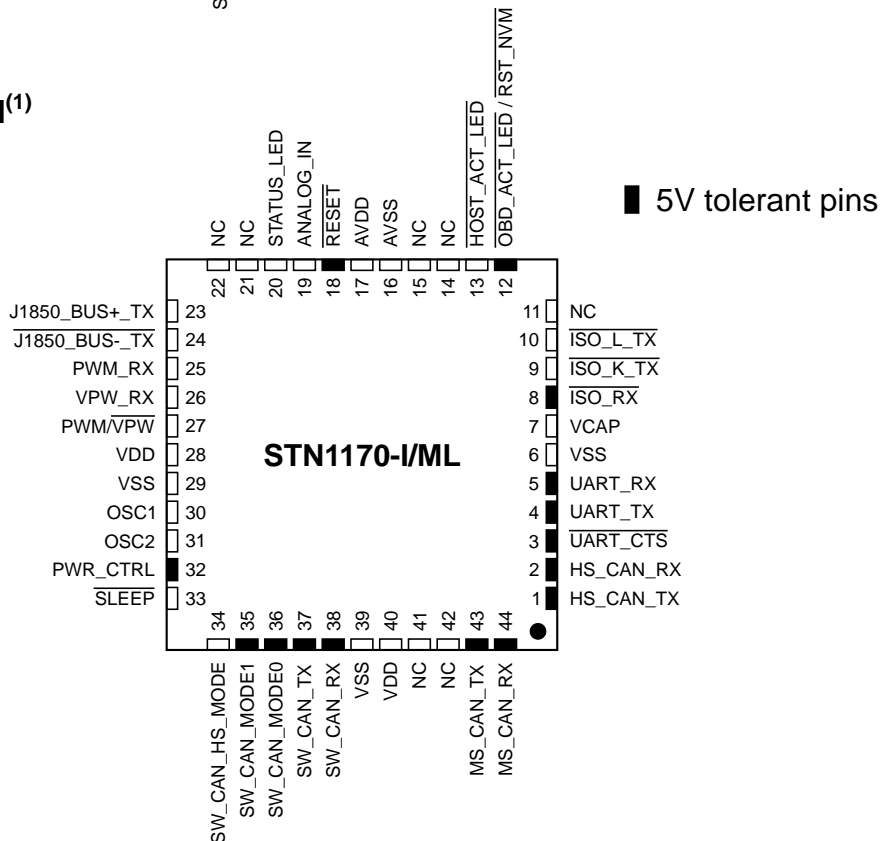| Pin Number	Pin Name	Pin Type	Pin Description
1	HS_CAN_TX	OD, 5V, 4x	High-speed CAN transmit output
2	HS_CAN_RX	I, 5V	High-speed CAN receive input
3	UART_CTS	I, 5V	Active low UART clear to send input
4	UART_TX	OD, 5V, 2x	UART transmit output
5	UART_RX	I, 5V	UART receive input
6	VSS	P	Ground reference for logic and I/O pins
7	VCAP	P	CPU logic filter capacitor connection
8	ISO_RX	I, 5V	Active low ISO 9141/ISO 14230 K-line input
9	ISO_K_TX	O, 2x	Active low ISO 9141/ISO 14230 K-line output
10	ISO_L_TX	O, 4x	Active low ISO 9141/ISO 14230 L-line output
11	NC	–	Do not connect
12	OBD_ACT_LED / RST_NVM	OD/I, 5V, 2x	Active low OBD activity LED output *and* active low input to reset non-volatile settings to factory defaults
13	HOST_ACT_LED	O, 2x	Active low host activity LED output
14	NC	–	Do not connect
15	NC	–	Do not connect
16	AVSS	P	Analog ground reference
17	AVDD	P	Analog positive supply
18	RESET	I, 5V	Active low device reset input
19	ANALOG_IN	A	Analog voltage measurement input
20	STATUS_LED	O, 4x	Status LED output
21	NC	–	Do not connect
22	NC	–	Do not connect
23	J1850_BUS+_TX	O, 4x	SAE J1850 Bus+ transmit output
24	J1850_BUS-_TX	O, 4x	Active low SAE J1850 Bus- transmit output
25	PWM_RX	I	SAE J1850 PWM receive input
26	VPW_RX	I	SAE J1850 VPW receive input
27	PWM/VPW	O, 4x	SAE J1850 PWM/VPW Bus+ voltage select output
28	VDD	P	Positive supply for logic and I/O pins
29	VSS	P	Ground reference for logic and I/O pins
30	OSC1	I	16.000 MHz oscillator crystal input
31	OSC2	O	16.000 MHz oscillator crystal output
32	PWR_CTRL	OD, 5V, 2x	External power control output
33	SLEEP	I	External sleep control input

Pin Number	Pin Name	Pin Type	Pin Description
34	SW_CAN_LOAD	O, 8x	Single-wire CAN high-speed tool load enable output
35	SW_CAN_MODE1	OD, 5V, 2x	Single-wire CAN transceiver operating mode selection output 1
36	SW_CAN_MODE0	OD, 5V, 2x	Single-wire CAN transceiver operating mode selection output 0
37	SW_CAN_TX	OD, 5V, 2x	Single-wire CAN transmit output
38	SW_CAN_RX	I, 5V	Single-wire CAN receive input
39	VSS	P	Ground reference for logic and I/O pins
40	VDD	P	Positive supply for logic and I/O pins
41	NC	–	Do not connect
42	NC	–	Do not connect
43	MS_CAN_TX	OD, 5V, 2x	Medium-speed CAN transmit output
44	MS_CAN_RX	I, 5V	Medium-speed CAN receive input
PAD		–	Thermal pad

Legend:

I	– Schmitt trigger input with CMOS levels	O	– digital output	2x	– 2x source/sink driver
A	– analog input	OD	– open drain output	4x	– 4x source/sink driver
P	– power pin	5V	– 5 volt tolerant pin	8x	– 8x source/sink driver

4.2 Detailed Pin Descriptions

HS_CAN_TX

High-speed CAN transmit output. Open drain – requires a pull-up to V$_{DD}$ or 5V. This pin has a 4x current rating (see Table 6 "Output Pin DC Specifications"). Pull-up value depends on CAN baud rates used and the trace length (higher resistor values can be used with lower baud rates and shorter traces); recommended value is 1 kΩ. Pull up to V$_{DD}$ via 100 kΩ resistor if unused.

HS_CAN_RX

High-speed CAN receive input. Compatible with 3.3V and 5V logic. Pull up to V$_{DD}$ if unused.

U̅A̅R̅T̅_CTS

Active low UART clear to send input. Compatible with 3.3V and 5V logic. Connect to V$_{SS}$ if unused.

UART_TX

UART transmit output. Open drain – requires a pull-up to V$_{DD}$ or 5V. This pin has a 2x current rating (see Table 6 "Output Pin DC Specifications"). Pull-up value depends on UART baud rate and the trace length (higher resistor values can be used with lower baud rates and shorter traces); typical value is 1 kΩ (1.5 kΩ, if pulled up to 5V).

UART_RX

UART receive input. Compatible with 3.3V and 5V logic.

VSS

Ground reference for logic and I/O pins.

VCAP

CPU logic filter capacitor connection. Connect to a low-ESR (< 5 Ω) tantalum or ceramic capacitor. Minimum value is 4.7 µF; typical value is 10 µF.

I̅S̅O̅_RX

Active low ISO 9141/ISO 14230 K-line receive input. When K-line is high (recessive), this pin should be at a logic low level. Connect to V$_{SS}$ if unused.

I̅S̅O̅_K̅_TX

Active low ISO 9141/ISO 14230 K-line output. When the pin is logic high, K-line should be low. This pin has a 2x current rating (see Table 6 "Output Pin DC Specifications"). Leave unconnected if unused.

I̅S̅O̅_L̅_TX

Active low ISO 9141/ISO 14230 L-line output. When the pin is logic high, L-line should be low. This pin has a 4x current rating (see Table 6 "Output Pin DC Specifications"). Leave unconnected if unused.

O̅B̅D̅_A̅C̅T̅_L̅E̅D̅ / R̅S̅T̅_N̅V̅M̅

Active low OBD activity LED output and active low input to reset NVM to factory defaults. Open drain – requires a pull-up to V$_{DD}$ or 5V if not pulled up via an LED connection. This pin has a 2x current rating (see Table 6 "Output Pin DC Specifications"). Pull up to V$_{DD}$ if unused.

H̅O̅S̅T̅_A̅C̅T̅_L̅E̅D̅

Active low host activity LED output. This pin has a 2x current rating (see Table 6 "Output Pin DC Specifications"). Leave unconnected if unused.

AVSS

Analog ground reference. Must be connected to analog "clean" ground (between V$_{SS}$ - 0.3V and V$_{SS}$ + 0.3V) or V$_{SS}$.

AVDD

Analog positive supply. Must be connected to V$_{DD}$ or an external voltage reference (between V$_{DD}$ - 0.3V or 3.0V, whichever is greater and V$_{DD}$ + 0.3V or 3.6V, whichever is less). AV$_{DD}$ may be decoupled from digital supply by connecting it to V$_{DD}$ via a 10 Ω resistor or a small (10 µH – 47 µH) inductor.

R̅E̅S̅E̅T̅

Device reset input. A logic low pulse (min 2 µs) on this pin will reset the device. Apply a continuous logic low to hold the device in reset. If your circuit does not use this functionality, pull up this pin to V$_{DD}$.

ANALOG_IN

Analog voltage measurement input (AVDD max). By default, this input is calibrated for an external 62 kΩ/10 kΩ voltage divider connected to battery positive. Connect to AVSS if unused.

STATUS_LED

Status LED output. This pin will output constant high when the device is running and will output low with 5 ms high pulses every 3 seconds when in sleep mode. This pin has a 4x current rating (see Table 6 "Output Pin DC Specifications"). Leave unconnected if unused.

J1850_BUS+_TX

SAE J1850 Bus+ transmit output. When the pin is high, Bus+ should be high (dominant). This pin has a 4x current rating (see Table 6 "Output Pin DC Specifications"). Leave unconnected if unused.

J1850_BUS-_TX

Active low SAE J1850 Bus- transmit output. When the pin is high, Bus- should be low (dominant). This pin has a 4x current rating (see Table 6 "Output Pin DC Specifications"). Leave unconnected if unused.

PWM_RX

SAE J1850 PWM receive input. When the SAE J1850 bus is in the recessive state (Bus+ is low, Bus- is high), this pin should be at a logic low level. When the SAE J1850 bus is in the dominant (Bus+ is high) state, this pin should be at a logic high level. Connect to VSS if unused.

VPW_RX

SAE J1850 VPW receive input. When the SAE J1850 Bus+ is in the recessive (low) state, this pin should be at a logic low level. When the SAE J1850 Bus+ is in the dominant (high) state, this pin should be at a logic high level. Connect to VSS if unused.

PWM/VPW

The firmware uses this pin to control the voltage level of the SAE J1850 PWM/VPW Bus+ supply. When the PWM protocol is selected, it outputs a logic high to switch the supply voltage to a nominal 5V. When the VPW protocol is selected, it outputs a logic low to switch the supply voltage to a nominal 8V. This

pin has a 4x current rating (see Table 6 "Output Pin DC Specifications"). Leave unconnected if unused.

VDD

Positive 3.0 – 3.6V supply for logic and I/O pins.

OSC1, OSC2

16.000 MHz oscillator crystal connection.

PWR_CTRL

External power control output. Used to switch external circuitry into low-power (sleep) state. Polarity can be configured in firmware; default configuration is active high (logic low = sleep mode). Open drain – requires a pull-up to VDD or 5V; be mindful of the fact that the pull-up will draw current in low-power state. This pin has a 2x current rating (see Table 6 "Output Pin DC Specifications"). Pull down to VSS via 100 kΩ resistor if unused.

SLEEP

External sleep control input. When enabled in firmware, puts the device into low-power sleep mode. Polarity of this pin can be configured in firmware; default configuration is active low. Pull up to VDD if unused.

SW_CAN_LOAD

Single-wire CAN high-speed tool load enable output. The pin outputs logic high when high-speed tool load is enabled via the STCSWM command. This pin has an 8x current rating (see Table 6 "Output Pin DC Specifications"). Leave unconnected if unused.

SW_CAN_MODE0, SW_CAN_MODE1

Single-wire CAN transceiver operating mode selection outputs. Connect to MODE0, MODE1 pins of a single-wire CAN transceiver IC. Open drain – require pull-ups to VDD or 5V; recommended value is 10 kΩ. These pins have 2x current ratings (see Table 6 "Output Pin DC Specifications"). Both pins are driven low in sleep mode – it is recommended to pull up to a switched power to reduce power consumption during sleep. Leave unconnected if unused.

SW_CAN_RX

Single-wire CAN receive input. Compatible with 3.3V and 5V logic. Pull up to VDD if unused.

SW_CAN_TX

Single-wire CAN transmit output. Open drain – requires a pull-up to V$_{DD}$ or 5V. Pull-up resistor value depends on CAN baud rates used and the trace length (higher resistor values can be used with lower baud rates and shorter traces); recommended value is 1 kΩ (1.5 kΩ, if pulled up to 5V). This pin has a 2x current rating (see Table 6 "Output Pin DC Specifications"). Pull up to V$_{DD}$ via 100 kΩ resistor if unused.

MS_CAN_TX

Medium-speed CAN transmit output. Open drain – requires a pull-up to V$_{DD}$ or 5V. Pull-up resistor value depends on CAN baud rates used and the trace length (higher resistor values can be used with lower baud rates and shorter traces); recommended value is 1 kΩ (1.5 kΩ, if pulled up to 5V). This pin has a 2x current rating (see Table 6 "Output Pin DC Specifications"). Pull up to V$_{DD}$ via 100 kΩ resistor if unused.

MS_CAN_RX

Medium-speed CAN receive input. Compatible with 3.3V and 5V logic. Pull up to V$_{DD}$ if unused.

PAD

The metal plane at the bottom of the device (QFN package only). It is not connected to any pins internally. Connect to V$_{SS}$ externally.

5.0 Guidelines for Getting Started with STN1170

5.1 Basic Connection Requirements

Getting started with the STN1170 IC requires attention to a minimal set of device pin connections before proceeding with development. The following is a list of pin names, which must always be connected:

- All **VDD and VSS** pins (see Section 5.2 "Decoupling Capacitors")

- **AVDD and AVSS** pins (see Section 5.2 "Decoupling Capacitors" and Section 5.3 "AVDD and AVSS Pins")

- **VCAP** (see Section 5.4 "Internal Voltage Regulator Filter Capacitor")

- **RESET** pin (see Section 5.5 "Device Reset Pin")

- **OSC1 and OSC2** pins (see Section 5.6 "Oscillator Pins")

- **RST_NVM** pin (see Section 5.7 "NVM Reset Input")

- **Open Drain Output Pull-ups** (see Section 5.8 "Open Drain Outputs")

5.2 Decoupling Capacitors

You must use decoupling capacitors on every pair of power supply pins, such as VDD, VSS and AVDD, AVSS. Consider the following criteria when using decoupling capacitors:

- **Value and type of capacitor:** Recommendation of 1 µF, 10-20V. This capacitor should be a low-ESR and have resonance frequency in the range of 20 MHz and higher. It is recommended that ceramic capacitors be used.

- **Placement on the printed circuit board:** The decoupling capacitors should be placed as close to the pins as possible. It is recommended to place the capacitors on the same side of the board as the device. If space is constricted, the capacitor can be placed on another layer on the PCB using a via; however, ensure that the trace length from the pin to the capacitor is within ¼" (6 mm) in length.

- **Handling high frequency noise:** If the board is experiencing high frequency noise, upward of tens of MHz, add a second ceramic-type capacitor in parallel to the above described decoupling capacitor. The value of the second capacitor can be in the range of 0.01 µF to 0.001 µF. Place this second capacitor next to the primary decoupling capacitor.

- **Maximizing performance:** On the board layout from the power supply circuit, run the power and return traces to the decoupling capacitors first, and then to the device pins. This ensures that the decoupling capacitors are first in the power chain. Equally important is to keep the trace length between the capacitor and the power pins to a minimum thereby reducing PCB track inductance.

5.2.1 Tank Capacitors

On boards with power traces running longer than six inches in length, use a tank capacitor for integrated circuits, including the STN1170, to supply a local power source. The value of the tank capacitor should be determined based on the trace resistance that connects the power supply source to the device, and the maximum current drawn by the device in the application. In other words, select the tank capacitor so that it meets the acceptable voltage sag at the device. Typical values range from 4.7 µF to 47 µF.

5.3 AVDD and AVSS Pins

As a minimum, AVDD must be connected directly to VDD and AVSS must be connected directly to VSS.

It is recommended that AVDD be connected to to VDD via a 10 Ω resistor or a small (10 µH – 47 µH) inductor.

AVSS should be connected to the electrically cleanest ground net (plane). For best results, analog circuitry should have a separate ground plane with a point connection to VSS ground plane as close as possible to the AVSS pin.

5.4 Internal Voltage Regulator Filter Capacitor

A low-ESR (< 5 Ω) capacitor is required on the VCAP pin, which is used to stabilize the internal voltage regulator output voltage. The VCAP pin must not be connected to VDD, and must have a capacitor between 4.7 µF and 10 µF, 16V connected to ground. The type can be ceramic or tantalum. Refer to Section 7.2 "Electrical Characteristics" for additional information. The placement of this capacitor should be close to the VCAP pin. It is recommended that the trace length not exceed ¼" (6 mm).

5.5 Device Reset Pin

RESET pin must be logic high for STN1170 to run. If this pin is not controlled by the host controller, it must be connected to VDD.

It is recommended to pull up RESET pin to VDD via a 10 kΩ resistor.

5.6 Oscillator Pins

The oscillator circuit should be placed on the same side of the board as the device. Also, place the oscillator circuit close to the oscillator pins, not exceeding one-half inch (12 mm) distance between them. The load capacitors should be placed next to the oscillator itself, on the same side of the board. Use a grounded copper pour around the oscillator circuit to isolate them from surrounding circuits. The grounded copper pour should be routed directly to the STN1170 ground. Do not run any signal traces or power traces inside the ground pour. Also, if using a two-sided board, avoid any traces on the other side of the board where the crystal is placed.

5.7 NVM Reset Input

RST_NVM pin must be pulled up to VDD via a 100 kΩ resistor for proper device operation.

5.8 Open Drain Outputs

All open drain outputs (as specified in section 4.1) that are in use must be pulled up to VDD or 5V. Specifically, UART_TX pin must be pulled up in order to be able to communicate with the device. See section 4.2 "Detailed Pin Descriptions" for more information.

5.9 Unused Inputs and Unused Open Drain Outputs

None of the unused inputs or unused open drain outputs (as specified in section 4.1) should be left unconnected. The STN1170 is a CMOS integrated circuit. Leaving any of its inputs or open drain outputs floating may result in IC damage.

Unused open drain outputs can only be terminated with a resistor connected to VDD or 5V. Unused inputs can be terminated via a resistor or direct connection to VSS or VDD.

Unused inputs and open drain outputs should be connected as shown in Table 2. See section 4.2 "Detailed Pin Descriptions" and section 6.1 "Recommended Minimum Connection" for more information.

Table 2 – Recommended Unused Input and Open Drain Output Connections

| Pin Number	Pin Name	Level
1	HS_CAN_TX	H[2]
2	HS_CAN_RX	H
3	UART_CTS	L
4	UART_TX	H[2]
5	UART_RX	H
8	ISO_RX	L[1]
12	OBD_ACT_LED / RST_NVM	H[2]
18	RESET	H
19	ANALOG_IN	L[1]
25	PWM_RX	L[1]
26	VPW_RX	L[1]
32	PWR_CTRL	L[3]
33	SLEEP	H
35	SW_CAN_MODE1	—[4]
36	SW_CAN_MODE0	—[4]
37	SW_CAN_TX	H[2]
38	SW_CAN_RX	H
43	MS_CAN_TX	H[2]
44	MS_CAN_RX	H

Note 1. These inputs may be connected to either VDD or VSS. However, the preferred level is shown.

2. These open drain outputs cannot be connected to VDD directly. They can only be connected to VDD or 5V via a resistor.

3. These open drain outputs should not be connected to VSS directly. For reduced current consumption during sleep, when unused, these outputs should be connected to VSS via a resistor.

4. These open drain outputs are driven low when the single-wire CAN channel is not selected. Therefore, they can be left unconnected if unused.

6.0 Reference Schematics

6.1 Recommended Minimum Connection

Figure 1 shows the recommended minimum of components necessary to get the STN1170 to operate reliably, while minimizing power consumption. It is not a practical circuit; it is intended as a reference to show what to do with unused pins. Refer to the detailed pin descriptions (section 4.2) for more information.

Figure 1 – Recommended Minimum Connection
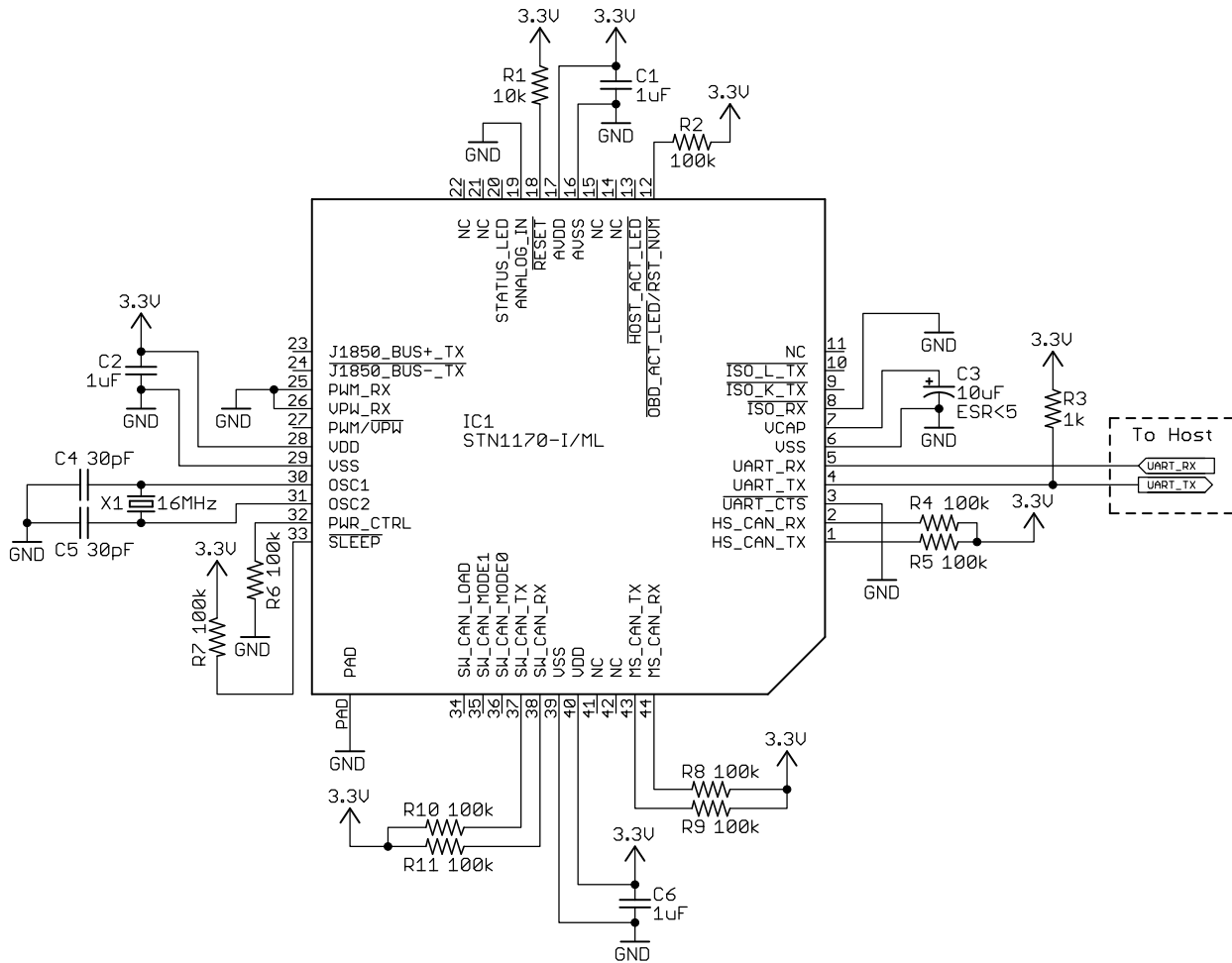
6.2 Typical Configuration

This section contains schematics showing the typical configuration for the various circuit blocks. Pay special attention when choosing substitutes for components with specific part numbers, to make sure they have the same or better characteristics. Components without specific part numbers are generic. Use good engineering practices and common sense to make sure the specific parts you choose are appropriate for your application.
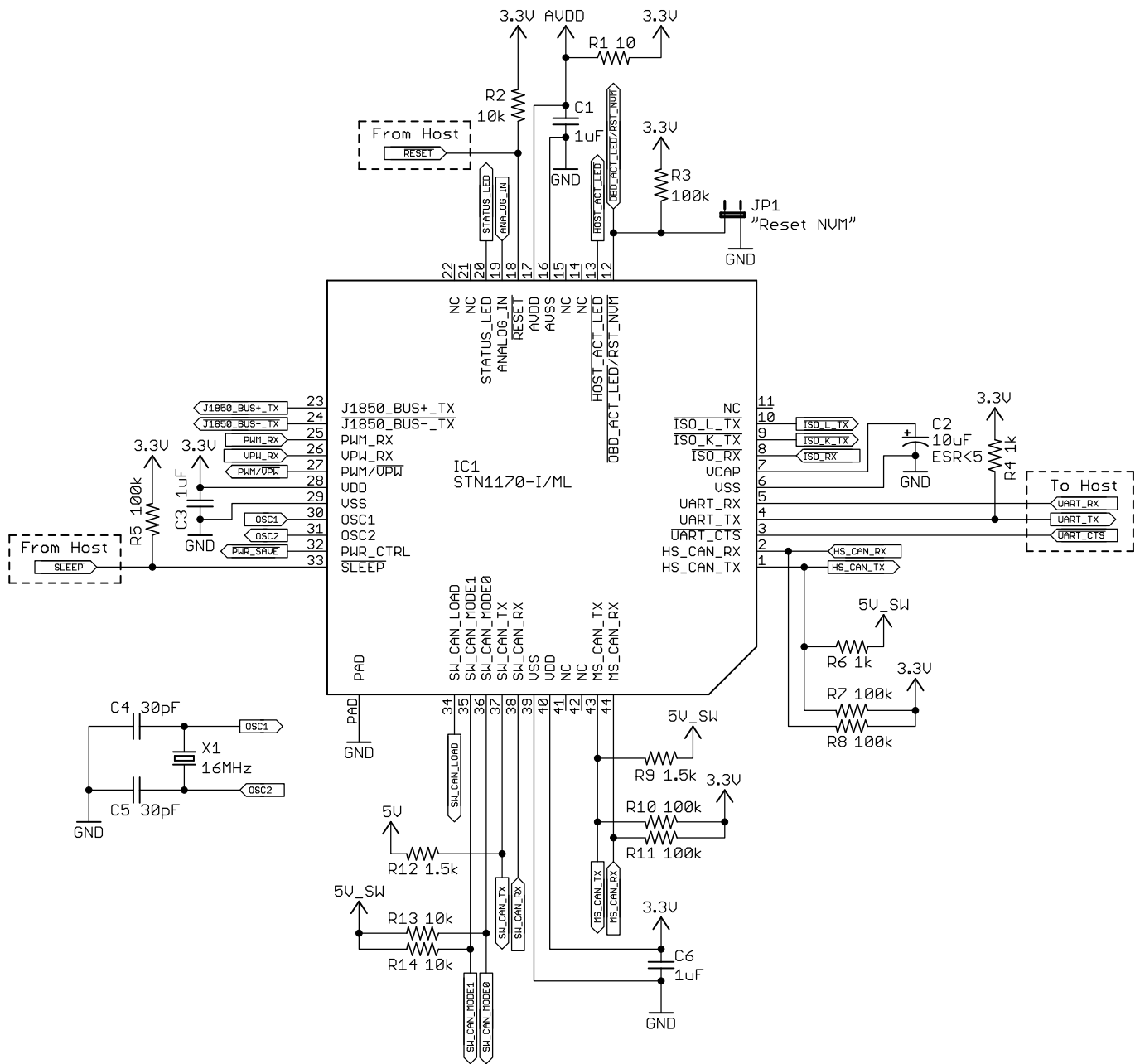
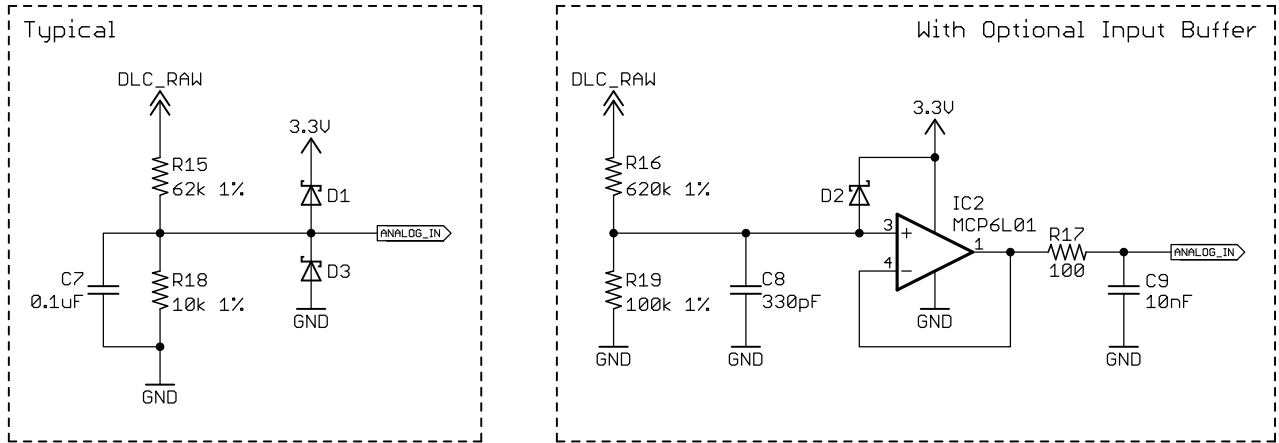**Figure 2 – STN1170 IC**

Figure 3 – Voltage Sense

Figure 4 – LEDs
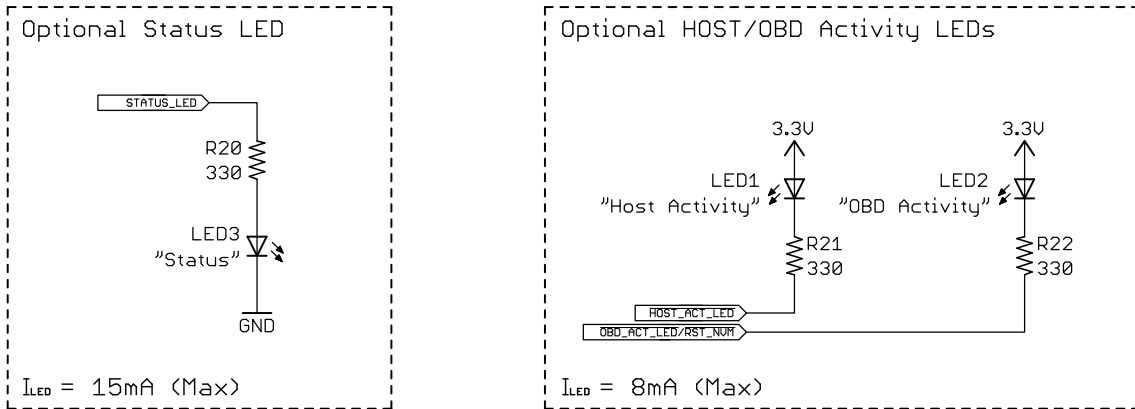
Figure 5 – OBD Port Connector
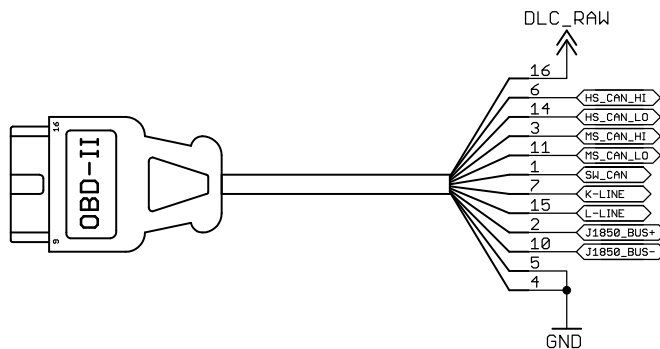
Figure 6 – Power Supplies
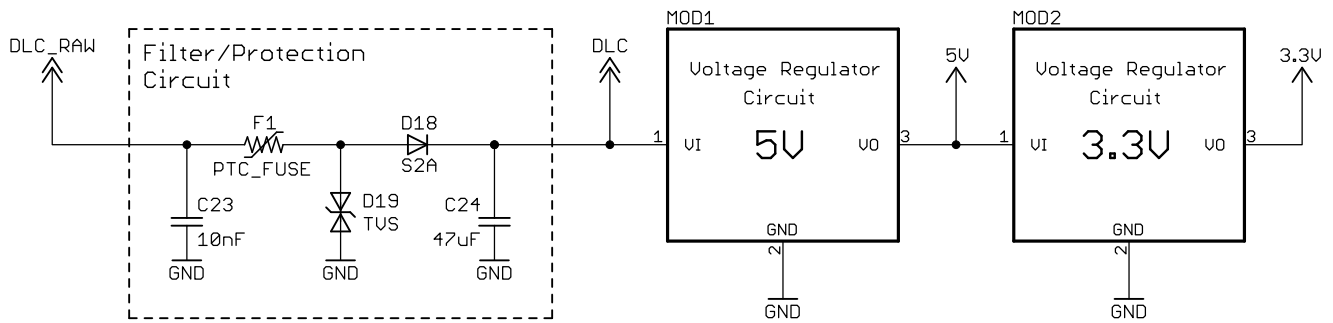
Figure 7 – Switched Power Control
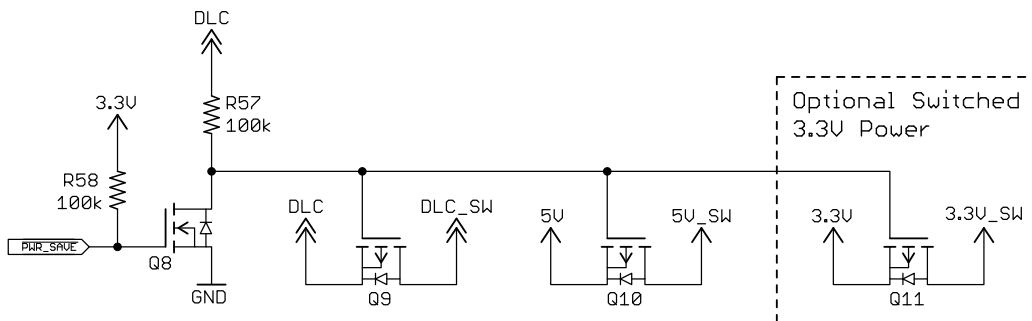
Figure 8 – ISO 9141/ISO 14230 Transceiver
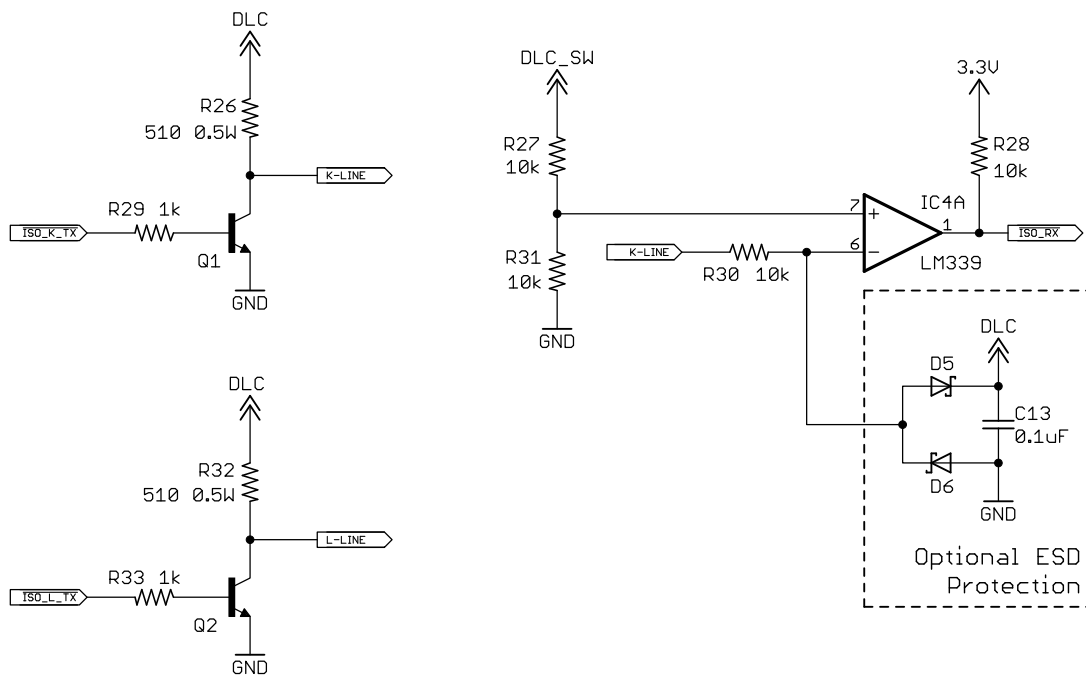
Figure 9 – High Speed CAN Transceiver
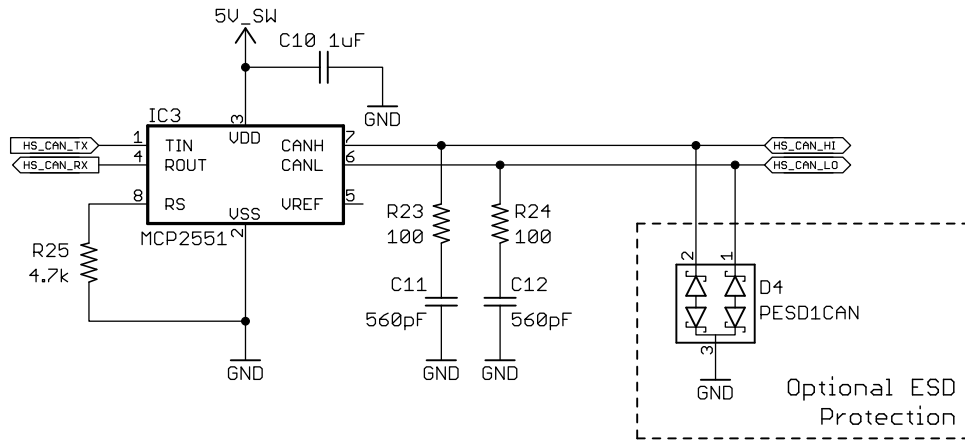
Figure 10 – Medium Speed CAN Transceiver
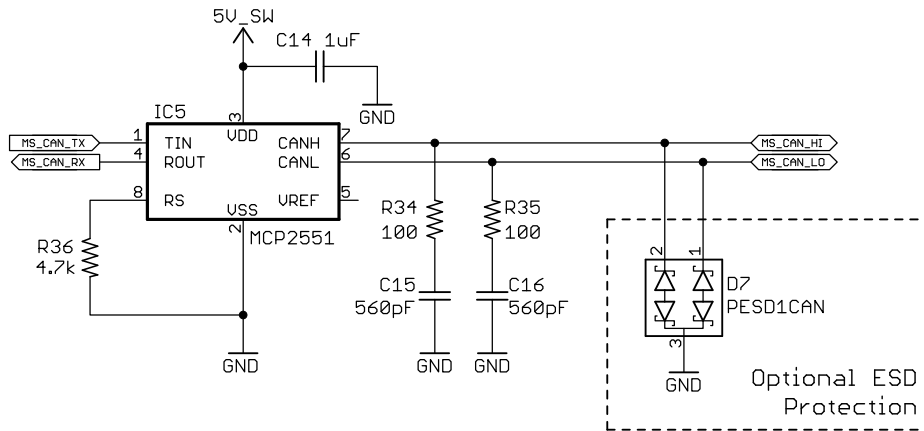
Figure 11 – Single Wire CAN Transceiver
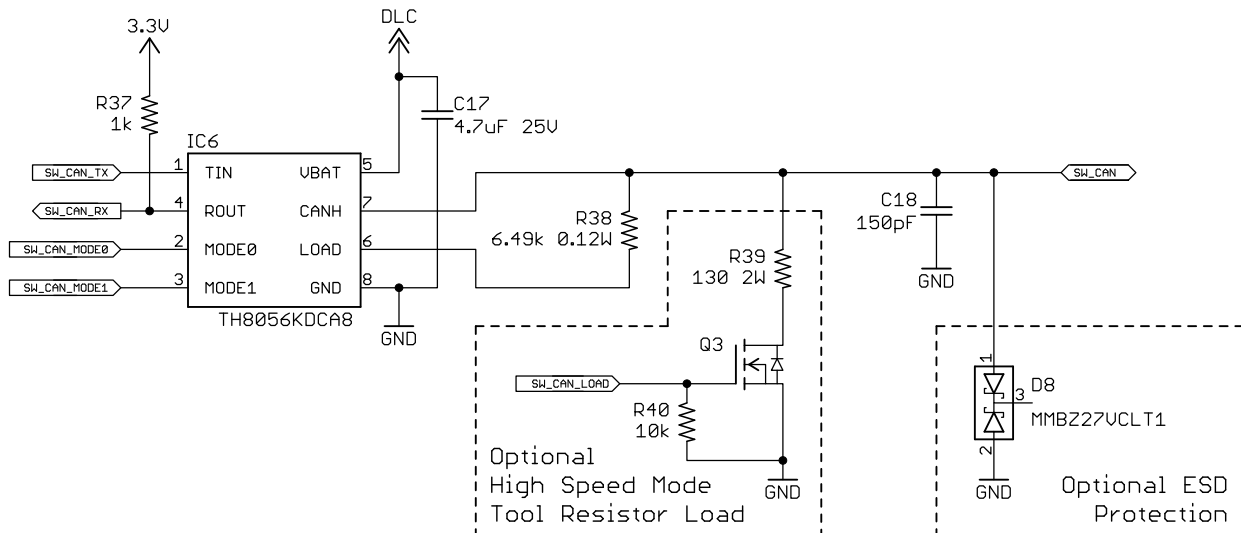
Important: Q5, Q6, and Q7 can only be substituted with transistors that have the same or better switching characteristics. OK to substitute fast-switching silicon diodes (e.g., 1N4148) for D10, D12 and D13. Also, note that the comparator IC4 is powered from DLC_SW.

Figure 12 – SAE J1850 Transceiver
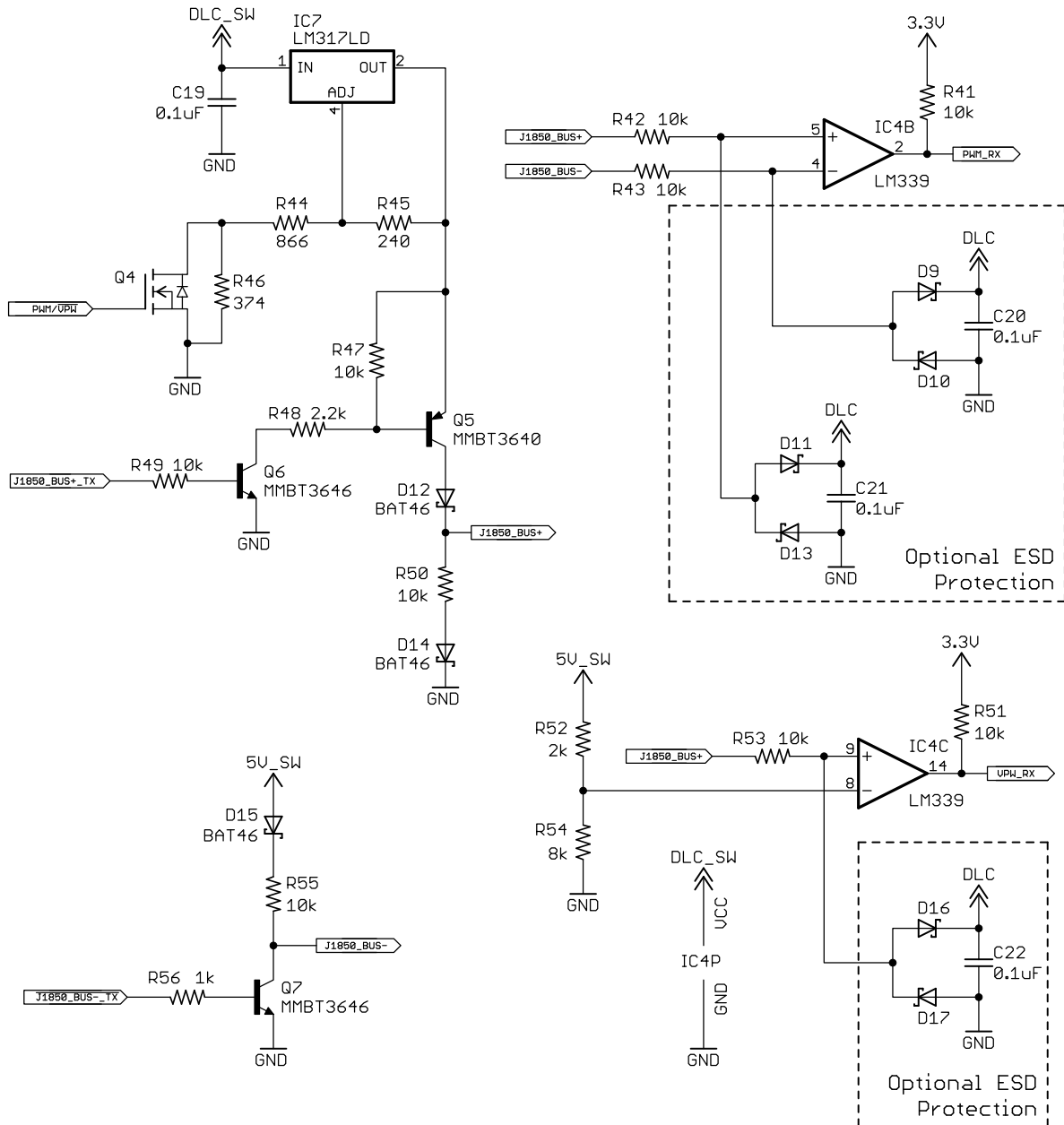
7.0 Electrical Characteristics

This section provides an overview of the STN1170 electrical characteristics. Additional information will be provided in future revisions of this document as it becomes available.

The STN1170 is based on the PIC24HJ128GP504 device from Microchip Technology. For more detailed device specifications or clarification, refer to Microchip documentation, available at http://www.microchip.com.

7.1 Absolute Maximum Ratings [1]

Ambient temperature under bias .... -40°C to +125°C
Storage temperature .... -65°C to +160°C
Voltage on VDD with respect to VSS .... -0.3V to +4.0V
Voltage on any pin that is not 5V tolerant with respect to VSS[2] .... -0.3V to (VDD + 0.3V)
Voltage on any 5V tolerant pin with respect to VSS when VDD ≥ 3.0V[2] .... -0.3V to +5.6V
Voltage on any 5V tolerant pin with respect to VSS when VDD < 3.0V[2] .... -0.3V to 3.6V
Maximum current sourced/sunk by any 2x output[3] .... 8 mA
Maximum current sourced/sunk by any 4x output[3] .... 15 mA
Maximum current sourced/sunk by any 8x output[3] .... 25 mA

Note 1. Stresses beyond those listed here can cause permanent damage to the device. These are stress ratings only, and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods can affect device reliability.

2. See section 4.0 "Pinout" for the list of 5V tolerant pins.

3. See section 4.1 "Pinout Summary" to determine current rating of individual pins.

7.2 Electrical Characteristics

Table 3: Thermal Operating Conditions

Sym	Characteristic	Min	Typ	Max	Units	Conditions
TJ	**Operating Junction Temperature**	-40	—	+125	°C	
TA	**Operating Ambient Temperature**	-40	—	+85	°C	

Table 4: Power Specifications

Sym	Characteristic	Min	Typ[1]	Max	Units	Conditions
VDD	**Supply Voltage**	3.0	—	3.6	V	
VPOR	**VDD Start Voltage** to ensure internal power-on reset (POR) signal	—	—	VSS	V	
SVDD	**VDD Rise Rate**[2] to ensure internal power-on reset (POR) signal	0.03	—	—	V/ms	0–3.0V in 0.1s
AVDD	**Analog Supply Voltage**	Greater of VDD – 0.3 or 3.0	—	Lesser of VDD + 0.3 or 3.6	V	
AVSS	**Analog Ground Reference**	VSS – 0.3	—	VSS + 0.3	V	

Sym	Characteristic	Min	Typ[1]	Max	Units	Conditions
V$_{BOR}$	**Brown-out Reset Voltage**[3] on V$_{DD}$ transition high-to-low	2.40	—	2.55	V	
I$_{DD}$	**Operating Current**[4]	—	68	82[5]	mA	
I$_{PD}$	**Average Sleep Current**[4,6]	—	98	210[5]	µA	T$_A$ = +25°C
		—	300[5]	710[5]	µA	T$_A$ = +85°C
C$_{EFC}$	**External Filter Capacitor**[7] connected to V$_{CAP}$ pin	4.7	10	—	µF	ESR < 5 Ω

Note
1. Data in Typ column is at 3.3V, 25°C, unless otherwise stated.
2. This spec must be met in order to ensure that a correct internal power-on reset (POR) occurs. It is easily achieved using most common types of supplies, but may be violated if a supply with slowly varying voltage is used, as may be obtained through direct connection to solar cells or some charge pump circuits.
3. This parameter is for design guidance only and is not tested in manufacturing.
4. STN1170 device current only. Does not include any load currents.
5. Values are characterized, but not tested.
6. All wakeup triggers are on and wakeup trigger inputs are in their inactive states.
7. Typical V$_{CAP}$ voltage = 2.5V when V$_{DD}$ ≥ V$_{DDMIN}$.

Table 5: Input Pin DC Specifications

Sym	Characteristic	Min	Typ[1]	Max	Units	Conditions
V$_{IL}$	**Input Low Voltage**					
	MS_CAN_RX pin	V$_{SS}$	—	0.3 V$_{DD}$	V	
	all other inputs	V$_{SS}$	—	0.2 V$_{DD}$	V	
V$_{IH}$	**Input High Voltage**					
	non-5V tolerant pins[2]	0.7 V$_{DD}$	—	V$_{DD}$	V	
	5V tolerant pins[2]	0.7 V$_{DD}$	—	5.5	V	
V$_{IN}$	**ANALOG_IN Input Voltage**	AV$_{SS}$	—	AV$_{DD}$	V	
R$_{IN}$	**Recommended ANALOG_IN Voltage Source Impedance**	—	—	200	Ω	
I$_{ICL}$	**Input Low Injection Current**	0	—	-5[4,7]	mA	All pins, except V$_{DD}$, V$_{SS}$, AV$_{DD}$, AV$_{SS}$, $\overline{RESET}$, V$_{CAP}$, $\overline{SLEEP}$, and SW_CAN_LOAD
I$_{ICH}$	**Input High Injection Current**	0	—	+5[5,6,7]	mA	All pins, except V$_{DD}$, V$_{SS}$, AV$_{DD}$, AV$_{SS}$, $\overline{RESET}$, V$_{CAP}$, $\overline{SLEEP}$, SW_CAN_LOAD and 5V tolerant designated pins
Σ$_{IICT}$	**Total Input Injection Current** sum of all I/O and control pins	0	—	20[8]	mA	Absolute instantaneous sum of all ± input injection currents from all I/O pins (|I$_{ICL}$| + |I$_{ICH}$|) ≤ Σ$_{IICT}$

Note
1. Data in Typ column is at 3.3V, 25°C, unless otherwise stated.
2. See section 4.0 "Pinout" for the list of 5V tolerant pins.
3. Negative current is defined as current sourced by the pin.
4. V$_{IL}$ source < (V$_{SS}$ – 0.3). Characterized, but not tested.

5. Non-5V tolerant pins: V_{IH} source > (V_{DD} + 0.3), 5V tolerant pins: V_{IH} source > 5.5V. Characterized, but not tested.

6. 5V tolerant pins cannot tolerate any "positive" input injection current from input sources > 5.5V.

7. Injection currents > 0 can affect the ADC results by approximately 4-6 counts.

8. Any number and/or combination of inputs listed under I_{ICL} or I_{ICH} conditions are permitted, provided the mathematical "absolute instantaneous" sum of the input injection currents from all pins does not exceed the specified limit. Characterized, but not tested.

Table 6: Output Pin DC Specifications

Sym	Characteristic	Min	Typ	Max	Units	Conditions
V_{OL}	**Output Low Voltage**[1]					
	2x Sink Driver Pins[2]	—	—	0.4	V	$I_{OL} \leq$ 3 mA, V_{DD} = 3.3V
	4x Sink Driver Pins[2]	—	—	0.4	V	$I_{OL} \leq$ 6 mA, V_{DD} = 3.3V
	8x Sink Driver Pin[2]	—	—	0.4	V	$I_{OL} \leq$ 10 mA, V_{DD} = 3.3V
V_{OH}	**Output High Voltage**[1]					
	2x Source Driver Pins[2]	2.4	—	—	V	$I_{OH} \geq$ -3 mA, V_{DD} = 3.3V
	4x Source Driver Pins[2]	2.4	—	—	V	$I_{OH} \geq$ -6 mA, V_{DD} = 3.3V
	8x Source Driver Pin[2]	2.4	—	—	V	$I_{OH} \geq$ -10 mA, V_{DD} = 3.3V
V_{OH1}	**Output High Voltage**[1]					
	2x Source Driver Pins[2]	1.5	—	—	V	$I_{OH} \geq$ -6 mA, V_{DD} = 3.3V
		2.0	—	—	V	$I_{OH} \geq$ -5 mA, V_{DD} = 3.3V
		3.0	—	—	V	$I_{OH} \geq$ -2 mA, V_{DD} = 3.3V
	4x Source Driver Pins[2]	1.5	—	—	V	$I_{OH} \geq$ -12 mA, V_{DD} = 3.3V
		2.0	—	—	V	$I_{OH} \geq$ -11 mA, V_{DD} = 3.3V
		3.0	—	—	V	$I_{OH} \geq$ -3 mA, V_{DD} = 3.3V
	8x Source Driver Pin[2]	1.5	—	—	V	$I_{OH} \geq$ -16 mA, V_{DD} = 3.3V
		2.0	—	—	V	$I_{OH} \geq$ -12 mA, V_{DD} = 3.3V
		3.0	—	—	V	$I_{OH} \geq$ -4 mA, V_{DD} = 3.3V

Note **1.** Parameters are characterized, but not tested.

2. See section 4.1 "Pinout Summary" for the output driver current rating designations.

Table 7: I/O Pin Timing Requirements

Sym	Characteristic	Min	Typ	Max	Units	Conditions
T_{RST}	$\overline{\text{RESET}}$ Pulse Width (low)	2	—	—	µs	
T_{UWM}	**Minimum UART Rx Pulse Width** required for wakeup (user settable)	—	20	—	ns	user setting < 15
		15	—	65,534	µs	user setting ≥ 15
T_{STM}	**Minimum $\overline{\text{SLEEP}}$ Input Time** to stay high before wakeup (user settable)	—	15	—	µs	user setting = 0
		1	—	65,534	ms	user setting > 0

8.0 Packaging Diagrams and Parameters

8.1 TQFP (PT) Package

44-Lead Plastic Thin Quad Flatpack – 10x10x1 mm Body, 2.00 mm Footprint

For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.
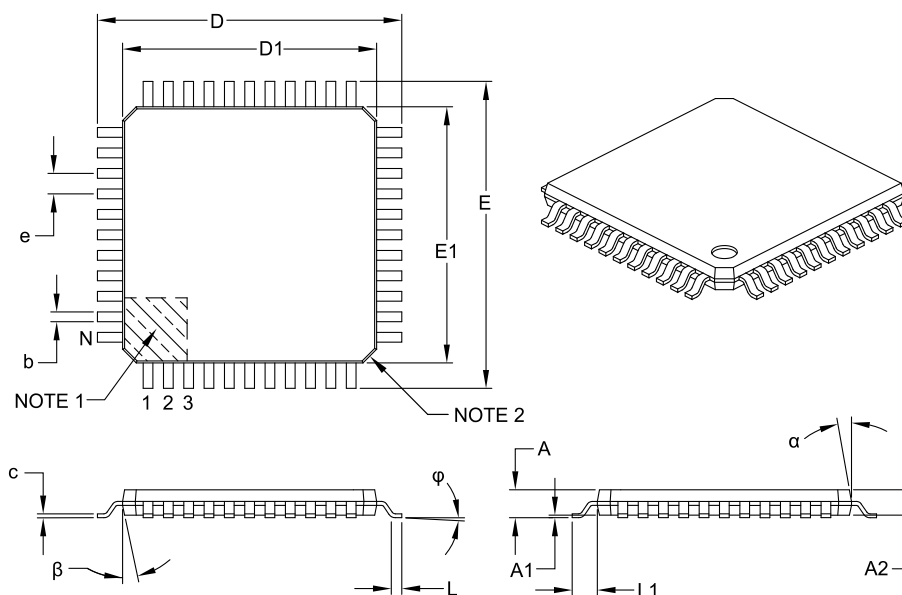
	Units		MILLIMETERS	
	Dimension Limits	MIN	NOM	MAX
Number of Leads	N		44	
Lead Pitch	e		0.80 BSC	
Overall Height	A	—	—	1.20
Molded Package Thickness	A2	0.95	1.00	1.05
Standoff	A1	0.05	—	0.15
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Foot Angle	φ	0°	3.5°	7°
Overall Width	E		12.00 BSC	
Overall Length	D		12.00 BSC	
Molded Package Width	E1		10.00 BSC	
Molded Package Length	D1		10.00 BSC	
Lead Thickness	c	0.09	—	0.20
Lead Width	b	0.30	0.37	0.45
Mold Draft Angle Top	α	11°	12°	13°
Mold Draft Angle Bottom	β	11°	12°	13°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Chamfers at corners are optional; size may vary.
3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

     BSC: Basic Dimension. Theoretically exact value shown without tolerances.
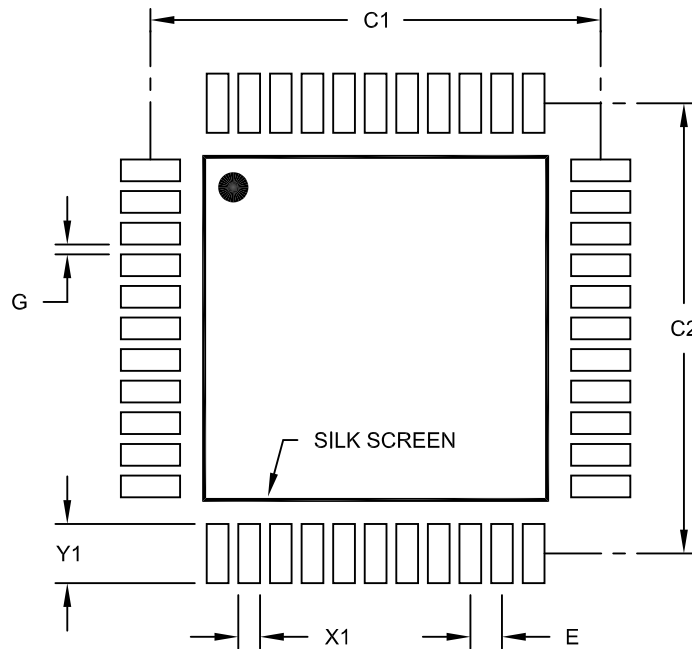
     REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-076B

8.2 TQFP (PT) Land Pattern

44-Lead Plastic Thin Quad Flatpack – 10x10x1 mm Body, 2.00 mm Footprint

For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

RECOMMENDED LAND PATTERN

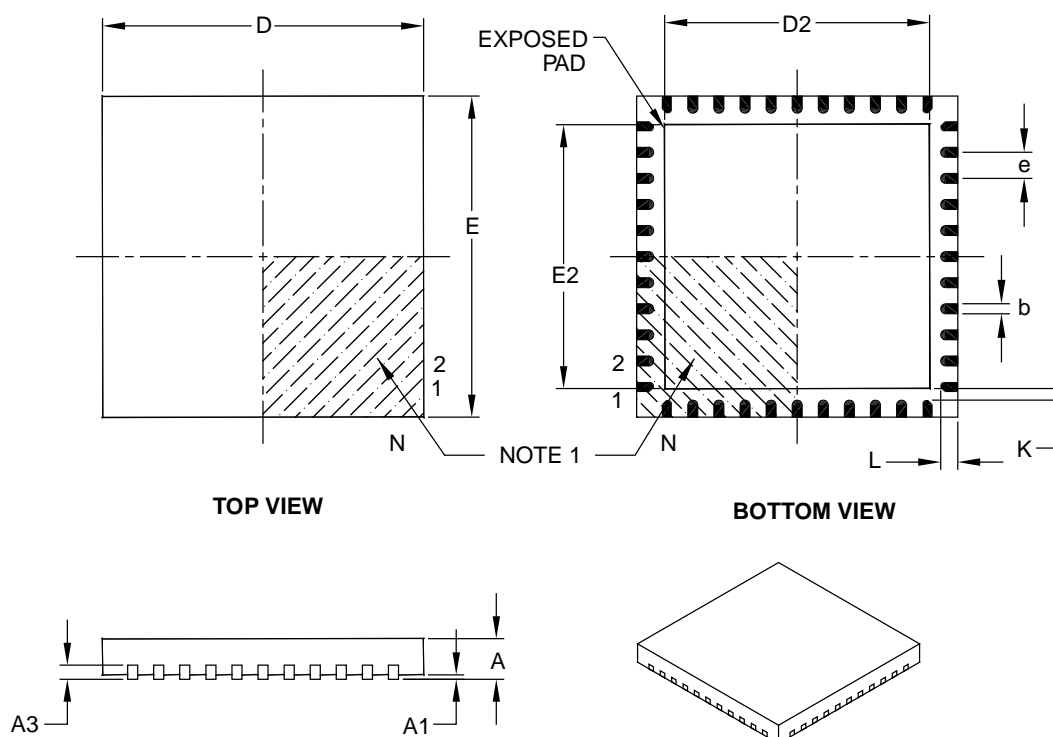|	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Contact Pitch	E	0.80 BSC		
Contact Pad Spacing	C1	—	11.40	—
Contact Pad Spacing	C2	—	11.40	—
Contact Pad Width (x44)	X1	—	—	0.55
Contact Pad Length (x44)	Y1	—	—	1.50
Distance Between Pads	G	0.25	—	—

Notes:
1. Dimensioning and tolerancing per ASME Y14.5M.
     BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2076A

8.3 QFN (ML) Package
44-Lead Plastic Quad Flat, No Lead Package – 8x8 mm Body

For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

TOP VIEW

BOTTOM VIEW

	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Number of Pins	N	44		
Pitch	e	0.65 BSC		
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3	0.20 REF		
Overall Width	E	8.00 BSC		
Exposed Pad Width	E2	6.30	6.45	6.80
Overall Length	D	8.00 BSC		
Exposed Pad Length	D2	6.30	6.45	6.80
Contact Width	b	0.25	0.30	0.38
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	—	—

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.
      BSC: Basic Dimension. Theoretically exact value shown without tolerances.
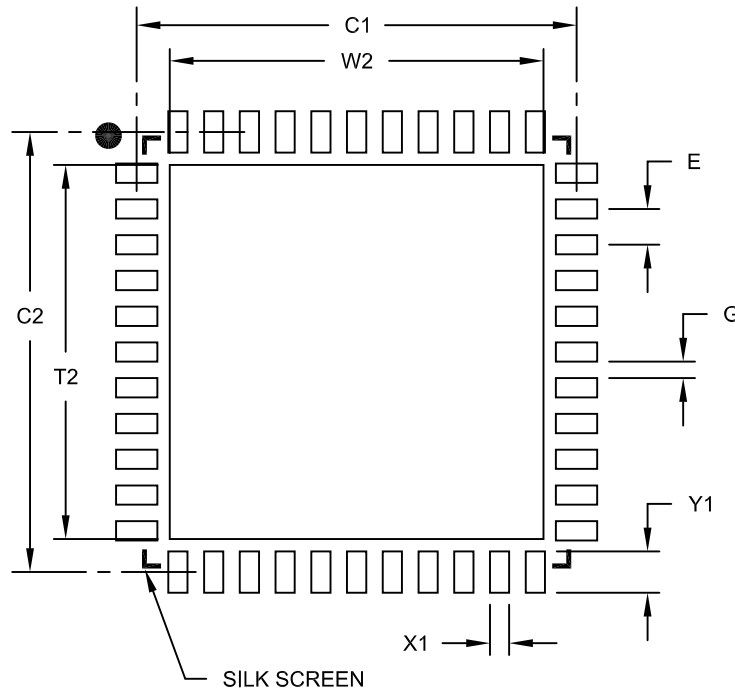   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-103B

8.4 QFN (ML) Land Pattern
44-Lead Plastic Quad Flat, No Lead Package – 8x8 mm Body

For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

SILK SCREEN

RECOMMENDED LAND PATTERN

	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Optional Center Pad Width	W2	—	—	6.80
Optional Center Pad Length	T2	—	—	6.80
Contact Pad Spacing	C1	—	8.00	—
Contact Pad Spacing	C2	—	8.00	—
Contact Pad Width (x44)	X1	—	—	0.35
Contact Pad Length (x44)	Y1	—	—	0.80
Distance Between Pads	G	0.25	—	—

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M.

    BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2103A

9.0 Ordering Information

T$_A$	Package		Part Number	SKU
-40°C to +85°C	TQFP (PT)	Tray	STN1170-I/PT	365401
	QFN (ML)	Tube	STN1170-I/ML	365411

Appendix A: Revision History

Revision A (May 31, 2012)

Initial release of this document.

Revision B (June 26, 2012)

Updated schematics, and added short descriptions to the "Recommended Minimum Connection" and "Typical Configuration" sections. Corrected detailed description of the VPW_RX pin (incorrect polarity was specified). Deleted figure titled "Suggested Placement of the Oscillator Circuit". Minor typographical and formatting changes.

Revision C (July 13, 2012)

Changed the value of most pullups and pulldowns for unused pins, from 10k to 100k. Updated description of SW_CAN_MODE pins to indicate that pins should be left unconnected if unused. Deleted last sentence of NVM Reset Input description (RST_NVM needs a pullup whether an LED is connected or not). Added "Recommended ANALOG_IN Voltage Source Impedance" (R_{IN}) specification to "Input Pin Specifications" table. Renamed the SW_CAN_HS_MODE pin to SW_CAN_LOAD. Updated "Recommended Minimum Connection" and "Typical Configuration" schematics and descriptions.

Appendix B: Contact Information

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