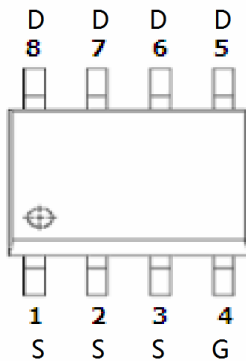


## DESCRIPTION

STN2018 is the N-Channel logic enhancement mode power field effect transistors which are produced using high cell density DMOS trench technology. This high density process is especially tailored to minimize on-state resistance.

These devices are particularly suited for low voltage application, notebook computer power management and other battery powered circuits where high-side switching.

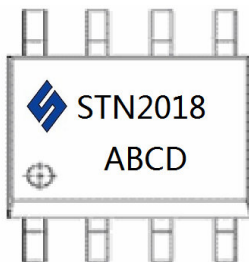
## PIN CONFIGURATION SOP-8



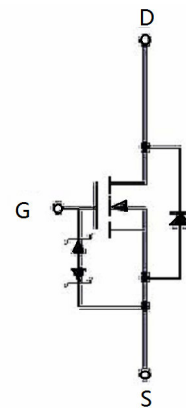
## FEATURE

- 20V/10A,  $R_{DS(ON)} = 10m\Omega$   
@VGS = 4.5V
- 20V/7A,  $R_{DS(ON)} = 15m\Omega$   
@VGS = 2.5V
- Super high density cell design for extremely low  $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- SOP-8 package design

## PART MARKING SOP-8



A : Year    B : Date Code  
C : Manufacture    D : Wafer Lot





**STN2018**  Lead-free

N Channel Enhancement Mode MOSFET  
**10.0A**

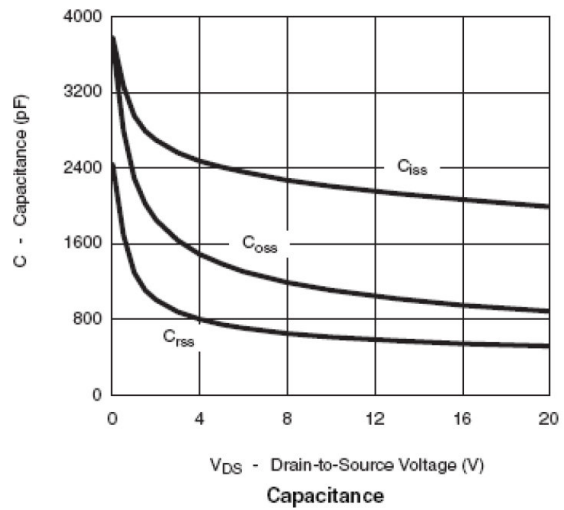
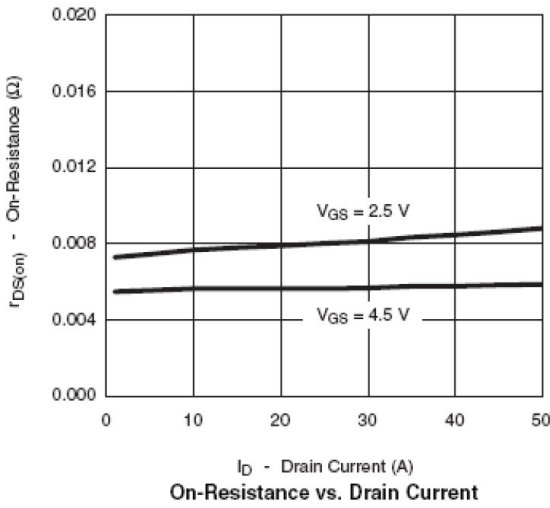
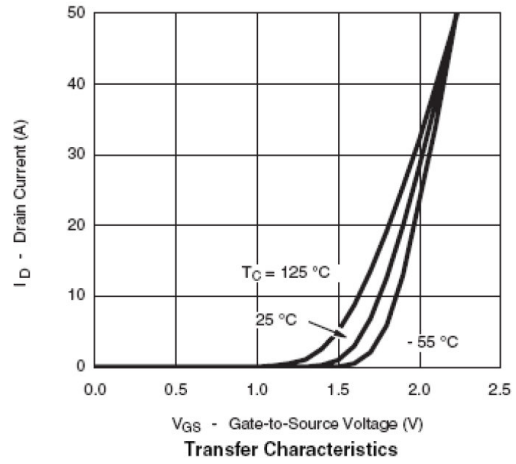
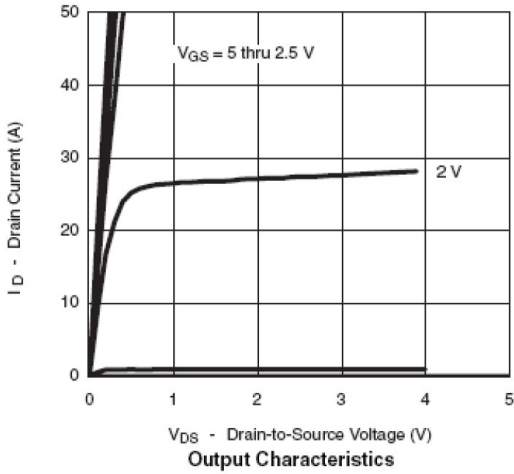
**ABSOLUTE MAXIMUM RATINGS** (Ta = 25°C Unless otherwise noted )

Parameter	Symbol	Typical	Unit
Drain-Source Voltage	V <sub>DSS</sub>	20	V
Gate-Source Voltage	V <sub>GSS</sub>	±12	V
Continuous Drain Current (T <sub>J</sub> =150°C)	I <sub>D</sub>	T <sub>A</sub> =25°C 10.0	A
		T <sub>A</sub> =70°C 8.0	
Pulsed Drain Current	I <sub>DM</sub>	35	A
Continuous Source Current (Diode Conduction)	I <sub>S</sub>	2.3	A
Power Dissipation	P <sub>D</sub>	T <sub>A</sub> =25°C 2.5	W
		T <sub>A</sub> =70°C 1.6	
Operation Junction Temperature	T <sub>J</sub>	-55/150	°C
Storage Temperature Range	T <sub>STG</sub>	-55/150	°C
Thermal Resistance-Junction to Ambient	R <sub>θJA</sub>	80	°C/W

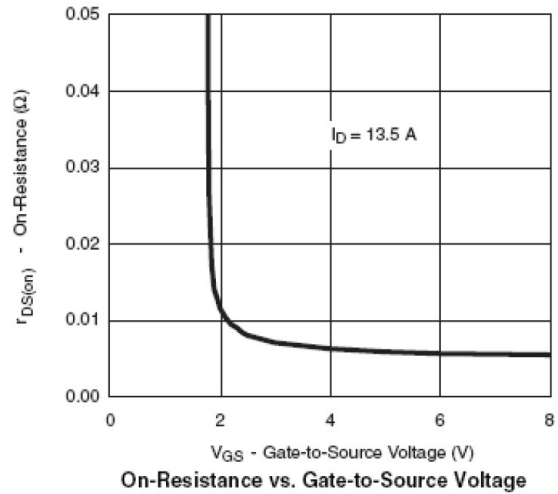
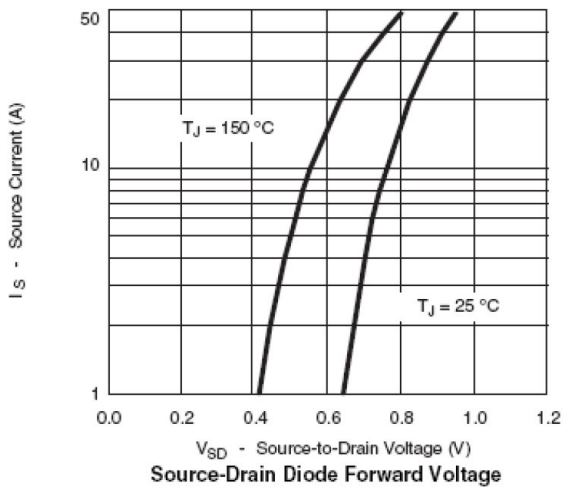
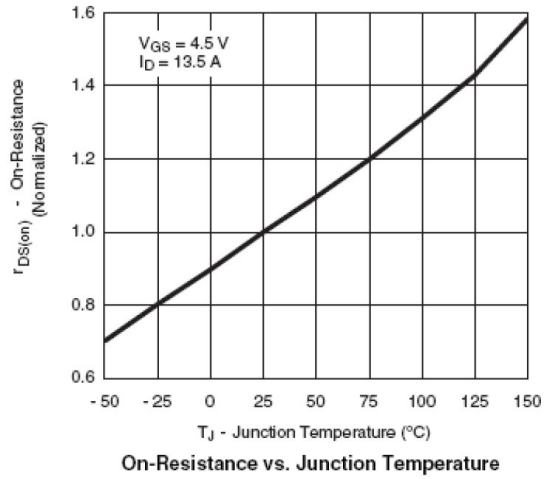
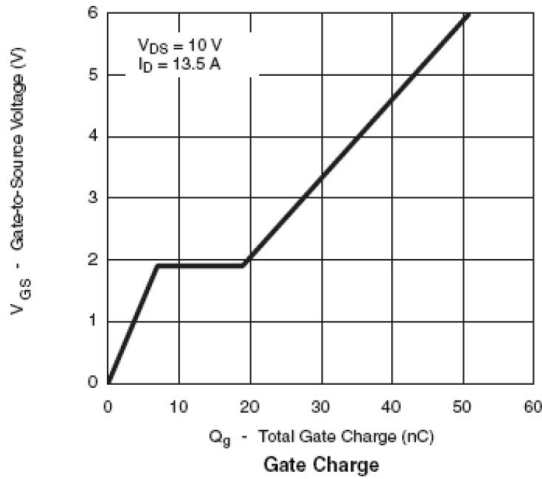
**ELECTRICAL CHARACTERISTICS** ( Ta = 25°C Unless otherwise noted )

Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\mu A$	20			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	0.6		1.4	V
Gate Leakage Current	$I_{GSS}$	$V_{DS}=0V, V_{GS}=\pm 12V$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$ $T_J=55^\circ C$	$V_{DS}=20V, V_{GS}=0V$			1	uA
		$V_{DS}=20V, V_{GS}=0V$			10	
On-State Drain Current	$I_{D(on)}$	$V_{DS}\geq 5V, V_{GS}=4.5$	6			A
Drain-source On-Resistance	$R_{DS(on)}$	$V_{GS}=4.5V, I_D=10A$ $V_{GS}=2.5V, I_D=7.0A$		0.008 0.011	0.012 0.015	$\Omega$
Forward Tran Conductance	$g_{fs}$	$V_{DS}=15.0V, I_D=5.0A$		30		S
Diode Forward Voltage	$V_{SD}$	$I_S=1.0A, V_{GS}=0V$		0.8	1.2	V
<b>Dynamic</b>						
Total Gate Charge	$Q_g$	$V_{DS}=10V, V_{GS}=4.5V$ $I_D=5.0A$		18	25	nC
Gate-Source Charge	$Q_{gs}$			4.2		
Gate-Drain Charge	$Q_{gd}$			6.8		
Input Capacitance	$C_{iss}$	$V_{DS}=10V, V_{GS}=0V$ $f=1MHz$		850		pF
Output Capacitance	$C_{oss}$			135		
Reverse Transfer Capacitance	$C_{rss}$			105		
Turn-On Time	$t_{d(on)tr}$	$V_{DD}=10V, R_L=10\Omega$ $I_D=1.0A, V_{GEN}=4.5V$ $R_G=6\Omega$		12	16	nS
				10	28	
Turn-Off Time	$t_{d(off)tf}$			30	55	
				35	58	

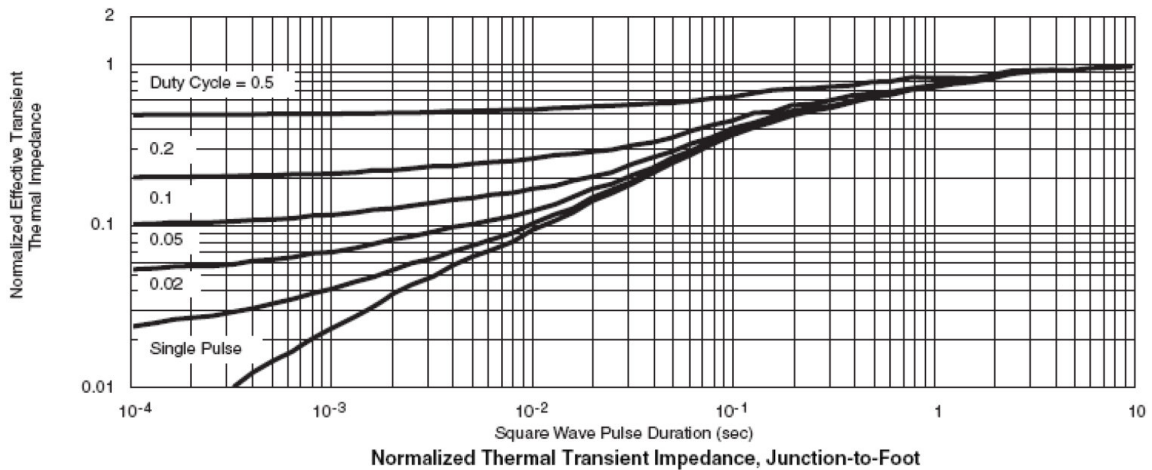
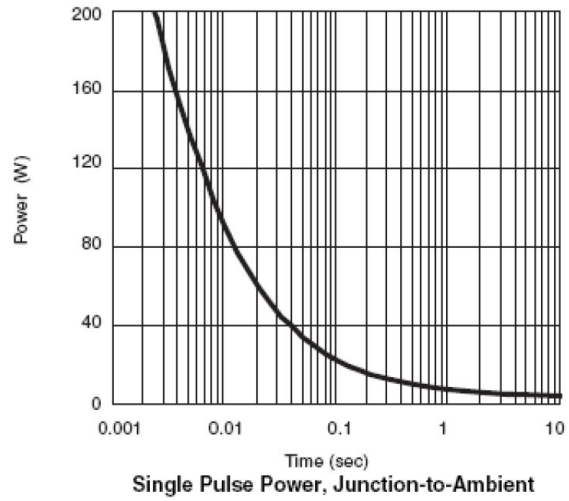
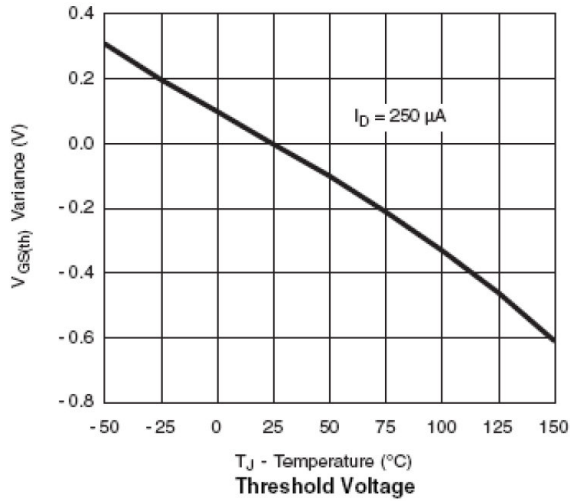
**TYPICAL CHARACTERISTICS (25°C Unless Note)**

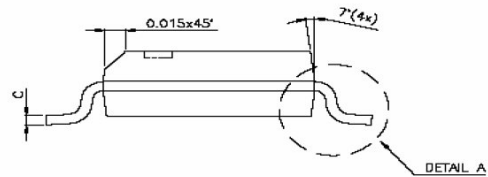
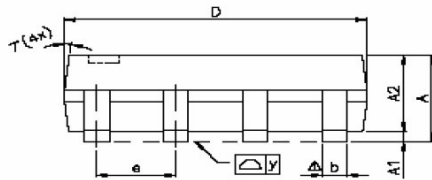
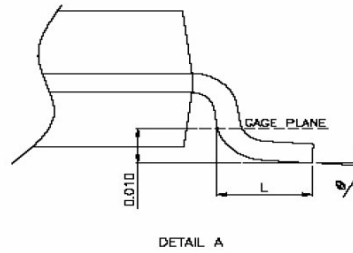
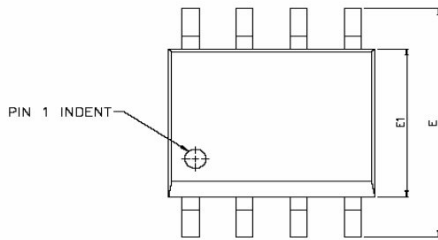


**TYPICAL CHARACTERISTICS (25°C Unless Note)**



**TYPICAL CHARACTERISTICS** (25°C Unless Note)



**SOP-8 PACKAGE OUTLINE**


SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.47	1.60	1.73	0.058	0.063	0.068
A1	0.10	—	0.25	0.004	—	0.010
A2	—	1.45	—	—	0.057	—
b	0.33	0.41	0.51	0.013	0.016	0.020
C	0.19	0.20	0.25	0.0075	0.008	0.0098
D	4.80	4.85	4.95	0.189	0.191	0.195
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e	—	1.27	—	—	0.050	—
L	0.38	0.71	1.27	0.015	0.028	0.050
y	—	—	0.076	—	—	0.003
φ	0°	—	8°	0°	—	8°