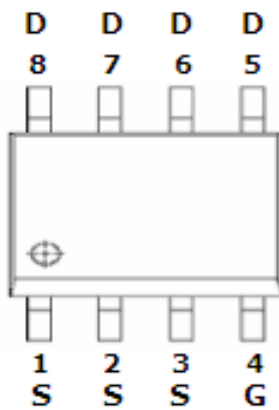


**DESCRIPTION**

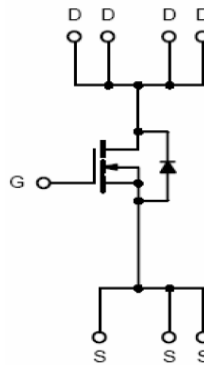
STN4260 is the N-Channel logic enhancement mode power field effect transistor which is produced using high cell density. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as power management and other battery powered circuits where high-side switching.

**PIN CONFIGURATION  
SOP-8**

**PART MARKING**


**Y: Year Code**  
**A: Produce Code**  
**P: Process Code**

**FEATURE**

- 60V/10A,  $R_{DS(ON)} = 11.5m\Omega$  (Typ.) @ $V_{GS} = 10V$
- 60V/8A,  $R_{DS(ON)} = 12.5m\Omega$  @ $V_{GS} = 4.5V$
- Super high density cell design for extremely low  $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- SOP-8 package design





**STN4260** 

N Channel Enhancement Mode MOSFET

18A

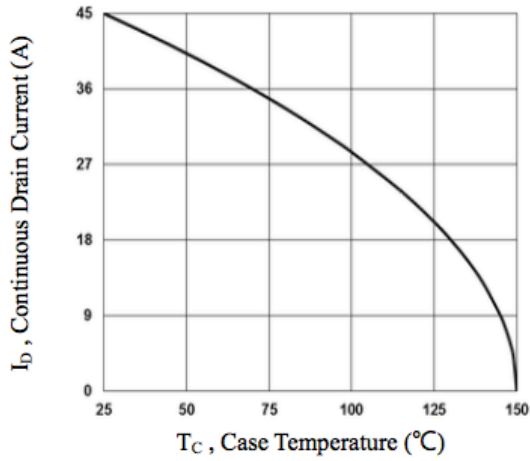
**ABSOLUTE MAXIMUM RATINGS** (Ta = 25°C Unless otherwise noted )

Parameter	Symbol	Typical	Unit
Drain-Source Voltage	VDSS	60	V
Gate-Source Voltage	VGSS	±20	V
Continuous Drain Current (TJ=150°C)	ID	20 14	A
TA=25°C TA=70°C			
Pulsed Drain Current	IDM	110	A
Continuous Source Current (Diode Conduction)	IS	4.5	A
Power Dissipation	PD	3.1 2.0	W
TA=25°C TA=70°C			
Operation Junction Temperature	TJ	150	°C
Storage Temperature Range	TSTG	-55/150	°C
Thermal Resistance-Junction to Ambient	RθJA	70	°C/W

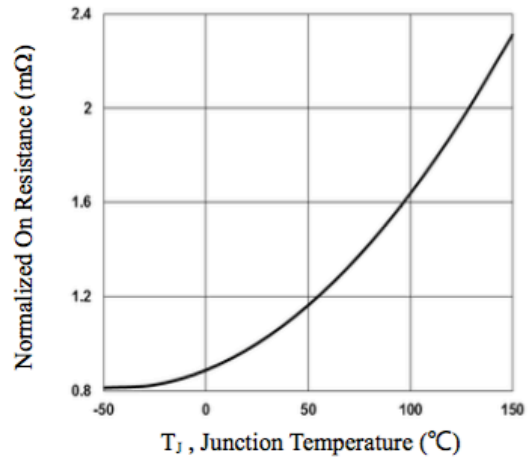
**ELECTRICAL CHARACTERISTICS** ( Ta = 25°C Unless otherwise noted )

Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\mu A$	60			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1.0		2.5	V
Gate Leakage Current	$I_{GSS}$	$V_{DS}=0V, V_{GS}=\pm 20V$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=60V, V_{GS}=0V$			1	uA
		$V_{DS}=60V, V_{GS}=0V$ $T_J=25^\circ C$			5	
Drain-source On-Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=10A$ $V_{GS}=4.5V, I_D=8A$		11.5 12.5	13 14	mΩ
Forward Transconductance	$g_{fs}$	$V_{DS}=10V, I_D=6A$		11.7		S
Diode Forward Voltage	$V_{SD}$	$I_S=1A, V_{GS}=0V$		0.8	1.0	V
<b>Dynamic</b>						
Total Gate Charge	$Q_g$	$V_{DS}=30V, V_{GS}=10V$ $I_D=10A$		40	58	nC
Gate-Source Charge	$Q_{gs}$			6	9	
Gate-Drain Charge	$Q_{gd}$			8.8	14	
Input Capacitance	$C_{iss}$	$V_{DS}=25V, V_{GS}=0V$ $F=1MHz$		2100		pF
Output Capacitance	$C_{oss}$			165		
Reverse Transfer Capacitance	$C_{rss}$			80		
Turn-On Time	$t_{d(on)}$ $t_r$	$V_{DD}=15V,$ $V_{GS}=10V, R_G=6\Omega$ $I_D=1A$		9.5	18	nS
				28	54	
Turn-Off Time	$t_{d(off)}$ $t_f$			45.3	86	
				80	120	

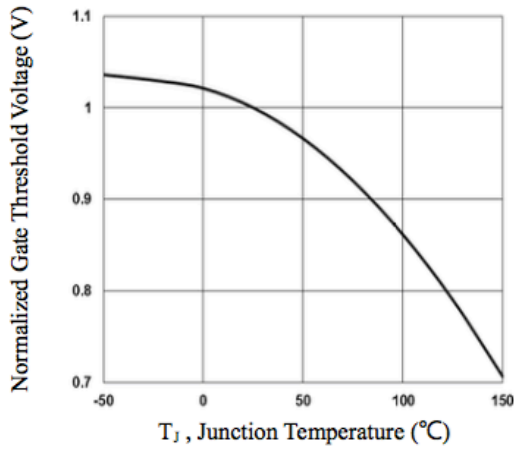
**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**



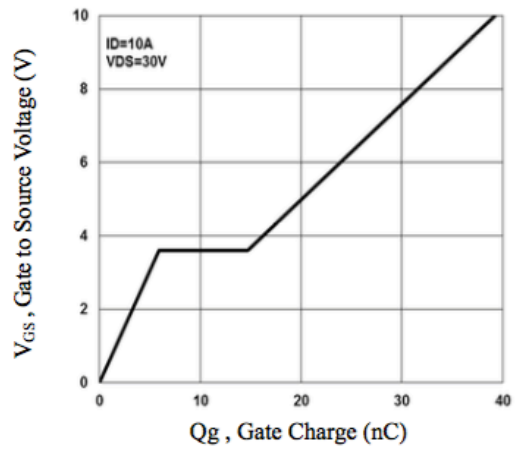
**Fig.1 Continuous Drain Current vs. T<sub>c</sub>**



**Fig.2 Normalized R<sub>DS(on)</sub> vs. T<sub>j</sub>**

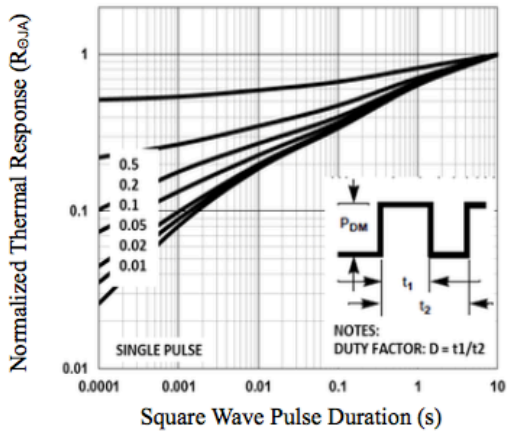


**Fig.3 Normalized V<sub>th</sub> vs. T<sub>j</sub>**

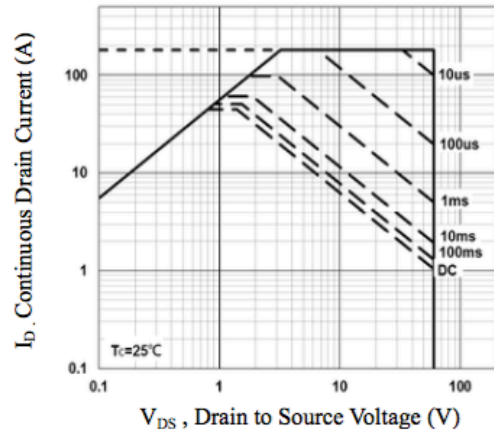


**Fig.4 Gate Charge Waveform**

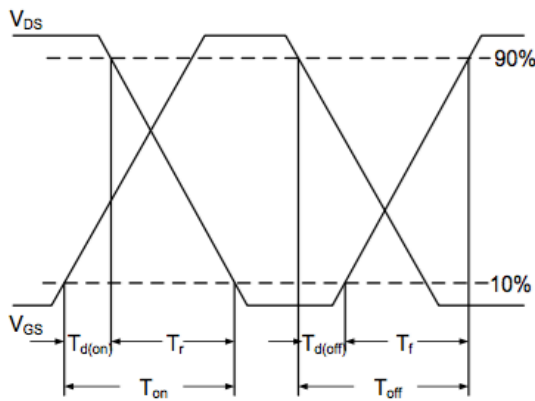
**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**



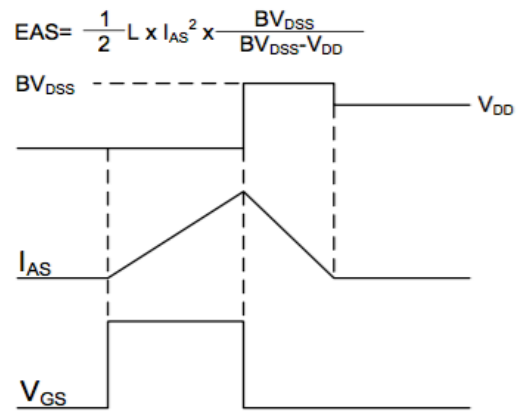
**Fig.5 Normalized Transient Response**



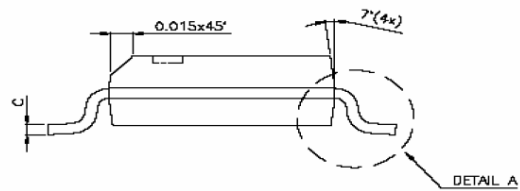
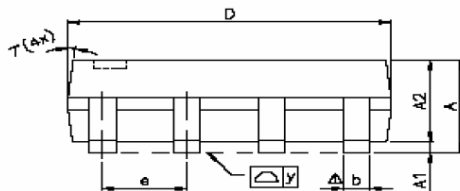
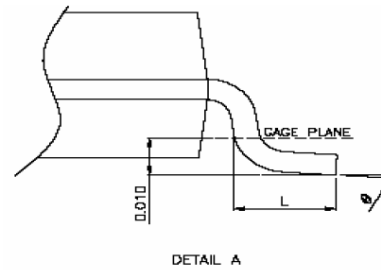
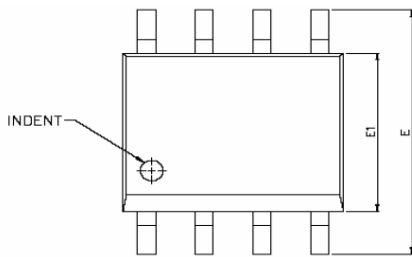
**Fig.6 Maximum Safe Operation Area**



**Fig.7 Switching Time Waveform**



**Fig.8 EAS Waveform**

**PACKAGE OUTLINE SOP-8P**


SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.47	1.60	1.73	0.058	0.063	0.068
A1	0.10	—	0.25	0.004	—	0.010
A2	—	1.45	—	—	0.057	—
b	0.33	0.41	0.51	0.013	0.016	0.020
C	0.19	0.20	0.25	0.0075	0.008	0.0098
D	4.80	4.85	4.95	0.189	0.191	0.195
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e	—	1.27	—	—	0.050	—
L	0.38	0.71	1.27	0.015	0.028	0.050
$\Delta$ y	—	—	0.076	—	—	0.003
$\varnothing$	0°	—	8°	0°	—	8°