STANSON

STN4426

N Channel Enhancement Mode MOSFET

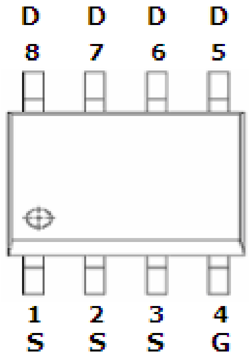
8.0A

DESCRIPTION

STN4426 is the N-Channel logic enhancement mode power field effect transistor which is produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application, notebook computer power management and other battery powered circuits where high-side switching.

PIN CONFIGURATION

SOP-8

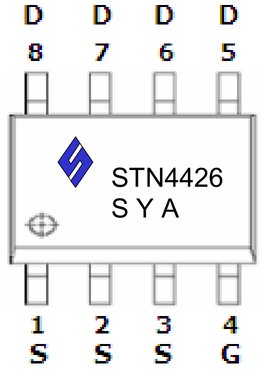


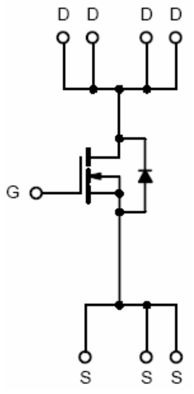
FEATURE

- 20V/8.0A, $R_{DS(ON)}$ = 28mΩ (Typ.) @V_{GS} = 4.5V
- 20V/7.0A, $R_{DS(ON)}$ = 36mΩ @V_{GS} = 2.5V
- 20V/3.0A, $R_{DS(ON)}$ = 42mΩ @V_{GS} = 1.8V
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- SOP-8 package design

PART MARKING

SOP-8





S: Subcontractor Y: Year Code
A: Process Code

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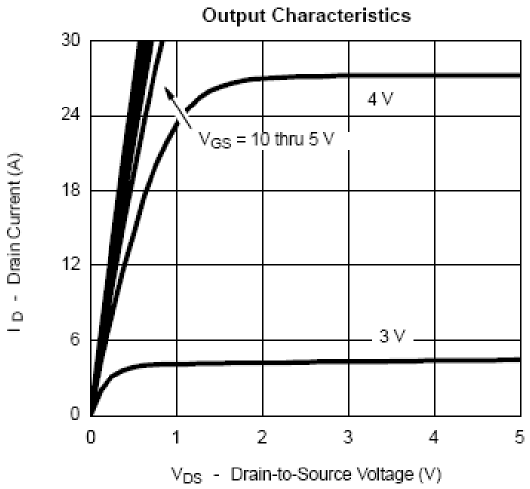
ABSOULTE MAXIMUM RATINGS (Ta = 25℃ Unless otherwise noted)

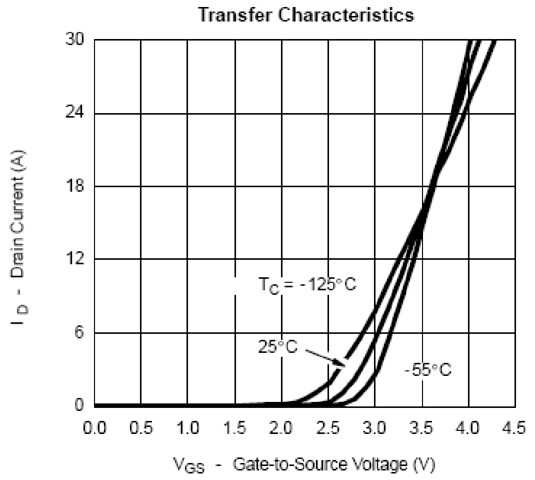
Parameter		**Symbol**	**Typical**	**Unit**
Drain-Source Voltage		VDSS	20	V
Gate-Source Voltage		VGSS	±12	V
Continuous Drain Current (TJ=150℃)	TA=25℃ TA=70℃	ID	7.4 6.0	A
Pulsed Drain Current		IDM	35	A
Continuous Source Current (Diode Conduction)		IS	2.3	A
Power Dissipation	TA=25℃ TA=70℃	PD	2.5 1.6	W
Operation Junction Temperature		TJ	-55/150	℃
Storgae Temperature Range		TSTG	-55/150	℃
Thermal Resistance-Junction to Ambient		RθJA	80	℃/W

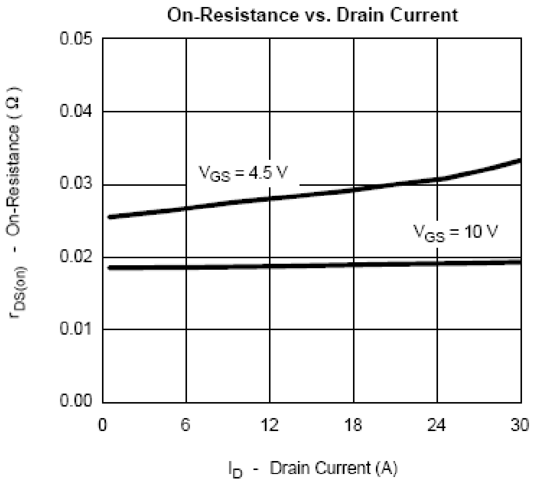
ELECTRICAL CHARACTERISTICS (Ta = 25℃ Unless otherwise noted)

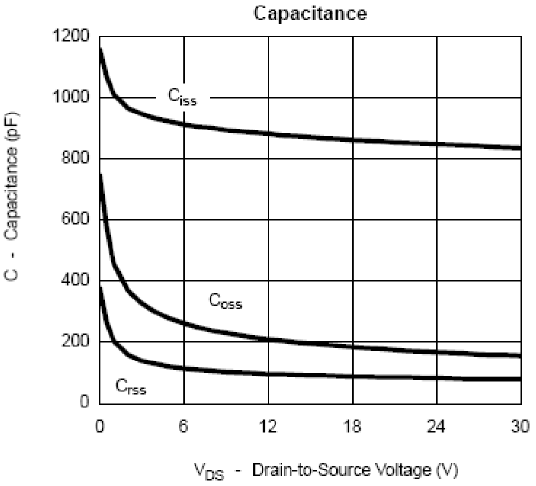
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V,ID=250uA	20			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},ID=250uA	0.4		1.0	V
Gate Leakage Current	I_{GSS}	V_{DS}=0V,V_{GS}=±12V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=20V,V_{GS}=0V			1	uA
		V_{DS}=20V,V_{GS}=0V T_J=85℃			10	
On-State Drain Current	$I_{D(on)}$	V_{DS}≧5V,V_{GS}=10V	6			A
Drain-source On-Resistance	$R_{DS(on)}$	V_{GS}=4.5V,I_D=8.0A V_{GS}=2.5V,I_D=7.0A V_{GS}=1.8V,I_D=3.0A		22 26 32	28 38 42	mΩ
Forward Transconductance	gfs	V_{DS}=15V,I_D=5.0AV		30		S
Diode Forward Voltage	V_{SD}	I_S=1.0A,V_{GS}=0V		0.8	1.2	V
Dynamic						
Total Gate Charge	Q_g	V_{DS}=10V,V_{GS}=4.5V I_D=5.0A		10	13	nC
Gate-Source Charge	Q_{gs}			1.4		
Gate-Drain Charge	Q_{gd}			2.1		
Input Capacitance	C_{iss}	V_{DS} ==10V,VGS=0V f=1MHz		600		pF
Output Capacitance	C_{oss}			120		
Reverse TransferCapacitance	C_{rss}			100		
Turn-On Time	$t_{d(on)}$	V_{DD}=10V,R_L=10Ω I_D=1A,V_{GEN}=4.5V R_G=6Ω		15	25	nS
	tr			40	60	
Turn-Off Time	$t_{d(off)}$			45	65	
	tf			30	40	

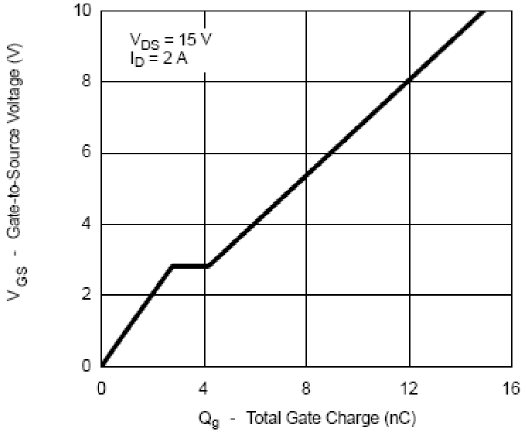
TYPICAL CHARACTERICTICS

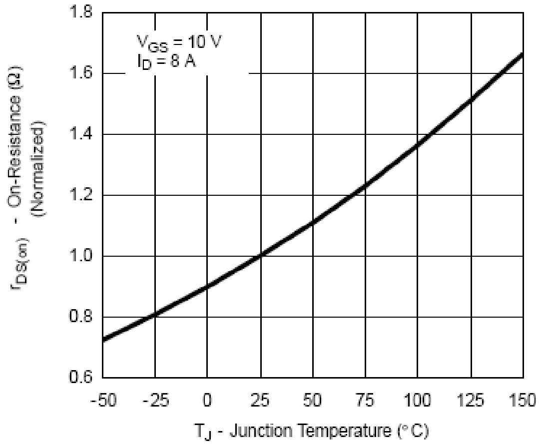






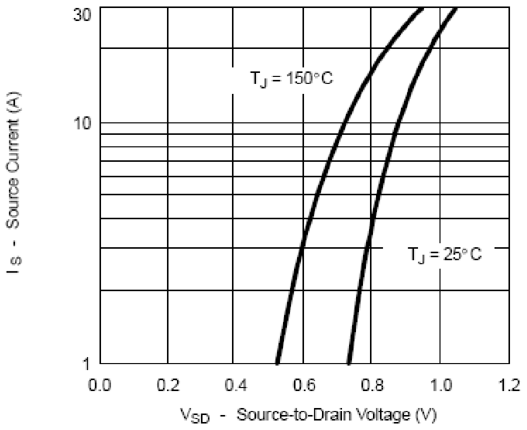




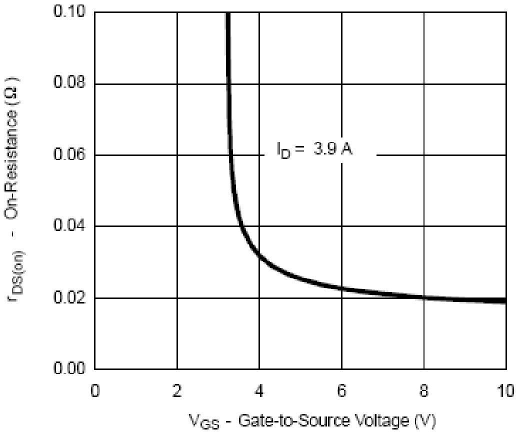


TYPICAL CHARACTERICTICS

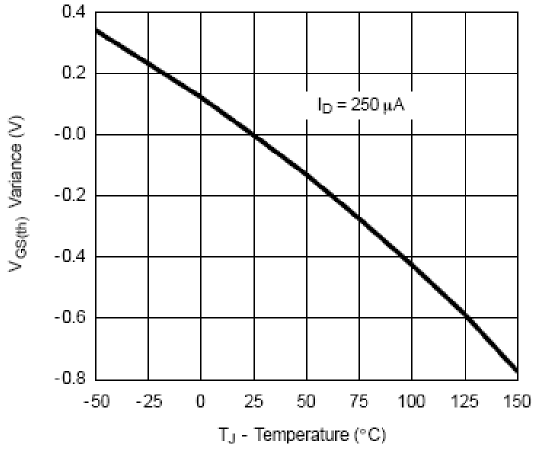
Source-Drain Diode Forward Voltage



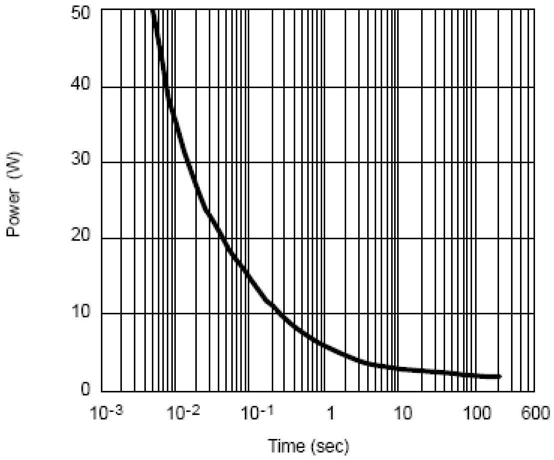
On-Resistance vs. Gate-to-Source Voltage



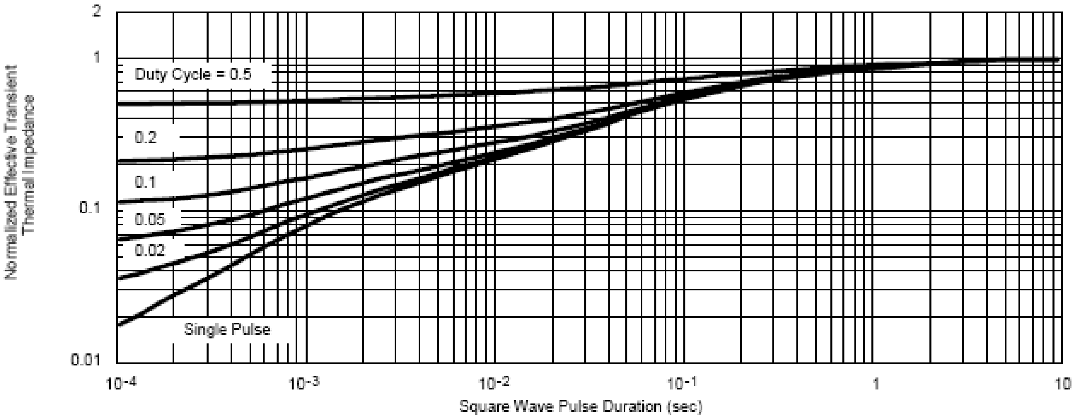
Threshold Voltage



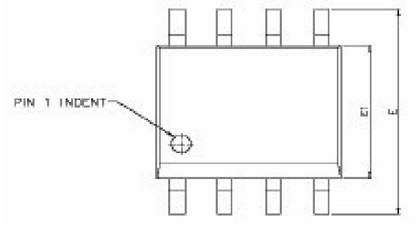
Single Pulse Power

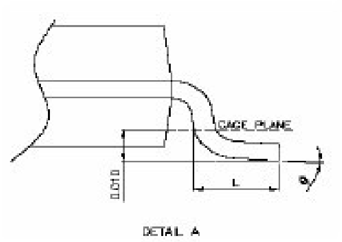


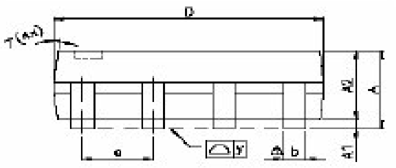
Normalized Thermal Transient Impedance, Junction-to-Foot

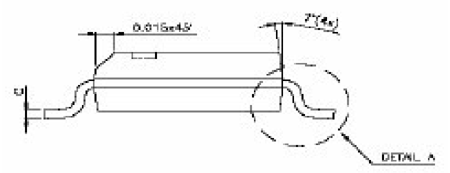


PACKAGE OUTLINE SOP-8P









SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.47	1.60	1.73	0.058	0.063	0.068
A1	0.10	——	0.25	0.004	——	0.010
A2	——	1.45	——	——	0.057	——
b	0.33	0.41	0.51	0.013	0.016	0.020
C	0.19	0.20	0.25	0.0075	0.008	0.0098
D	4.80	4.85	4.95	0.189	0.191	0.195
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e	——	1.27	——	——	0.050	——
L	0.38	0.71	1.27	0.015	0.028	0.050
△2 y	——	——	0.076	——	——	0.003
θ	0°	——	8°	0°	——	8°