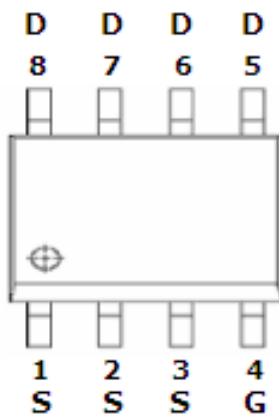


DESCRIPTION

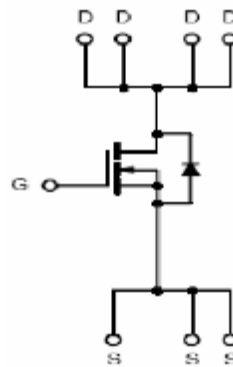
STN4438 is the N-Channel logic enhancement mode power field effect transistor which is produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as power management and other battery powered circuits where high-side switching.

**PIN CONFIGURATION
SOP-8**

PART MARKING


Y: Year Code A: Process Code

FEATURE

- I 60V/8.2A, $R_{DS(ON)} = 25m\Omega$ (Typ.) @ $V_{GS} = 10V$
- I 60V/7.6A, $R_{DS(ON)} = 30m\Omega$ @ $V_{GS} = 4.5V$
- I Super high density cell design for extremely low $R_{DS(ON)}$
- I Exceptional on-resistance and maximum DC current capability
- I SOP-8 package design



**STN4438**

N Channel Enhancement Mode MOSFET

8.2A**ABSOLUTE MAXIMUM RATINGS (Ta = 25°C Unless otherwise noted)**

Parameter	Symbol	Typical	Unit
Drain-Source Voltage	VDSS	60	V
Gate-Source Voltage	VGSS	±20	V
Continuous Drain Current (TJ=150°C)	ID	TA=25°C 8.2	A
		TA=70°C 6.6	
Pulsed Drain Current	IDM	40	A
Continuous Source Current (Diode Conduction)	IS	3.0	A
Power Dissipation	PD	TA=25°C 3.1	W
		TA=70°C 2.0	
Operation Junction Temperature	TJ	150	°C
Storage Temperature Range	TSTG	-55/150	°C
Thermal Resistance-Junction to Ambient	RθJA	70	°C/W

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ELECTRICAL CHARACTERISTICS (Ta = 25°C Unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\mu A$	60			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1.0		3.0	V
Gate Leakage Current	I_{GSS}	$V_{DS}=0V, V_{GS}=\pm 20V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=48V, V_{GS}=0V$			1	uA
		$V_{DS}=48V, V_{GS}=0V$ $T_J=5^\circ C$			5	
On-State Drain Current	$I_{D(on)}$	$V_{DS}\geq 5V, V_{GS}=10V$	40			A
Drain-source On-Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=10A$ $V_{GS}=4.5V, I_D=8A$		25 30	30 35	mΩ
Forward Transconductance	g_{fs}	$V_{DS}=5V, I_D=6.2AV$		24		S
Diode Forward Voltage	V_{SD}	$I_s=1A, V_{GS}=0V$		0.8	1.2	V
Dynamic						
Total Gate Charge	Q_g	$V_{DS}=30V, V_{GS}=10V$ $I_D=8.2A$		48	58	nC
Gate-Source Charge	Q_{gs}			24.2	30	
Gate-Drain Charge	Q_{gd}			14.5		
Input Capacitance	C_{iss}	$V_{DS} = = 30V, V_{GS}=0V$ $F = 1MHz$		1920		pF
Output Capacitance	C_{oss}			155		
Reverse Transfer Capacitance	C_{rss}			116		
Turn-On Time	$t_{d(on)}$	$V_{DS}=30V, R_L=3.6\Omega$ $V_{GEN}=3V$		8.5		nS
	t_r			6		
Turn-Off Time	$t_{d(off)}$			29		
	t_f			6		

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

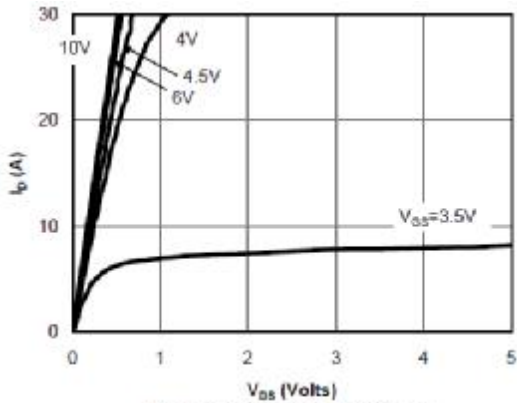


Fig 1: On-Region Characteristics

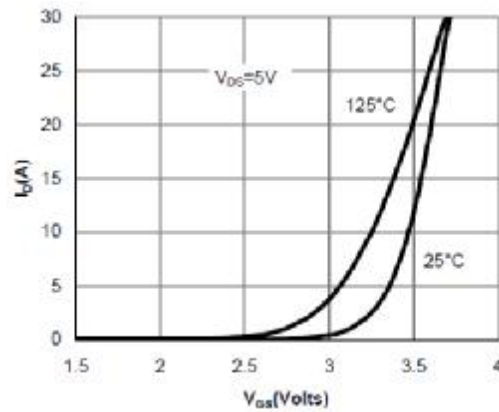


Figure 2: Transfer Characteristics

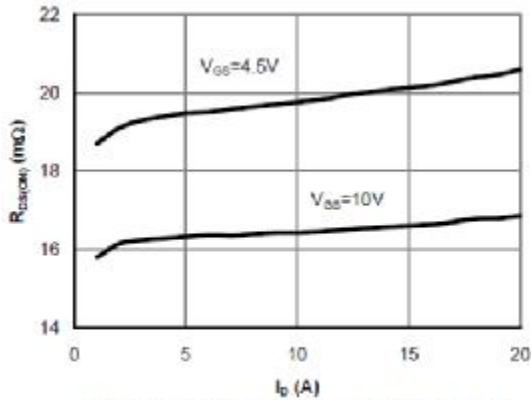


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

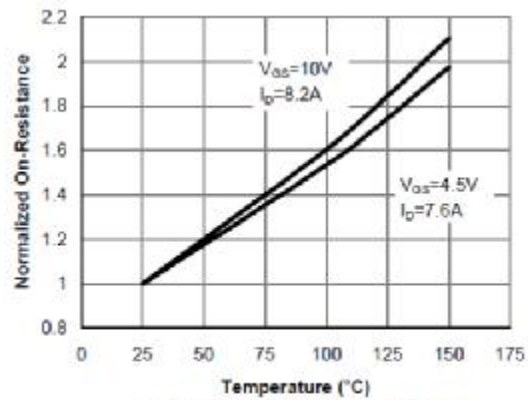


Figure 4: On-Resistance vs. Junction Temperature

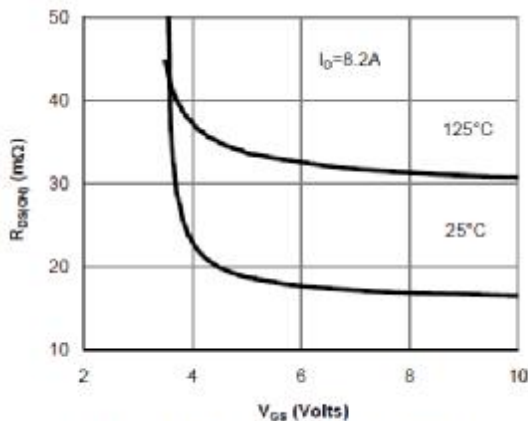


Figure 5: On-Resistance vs. Gate-Source Voltage

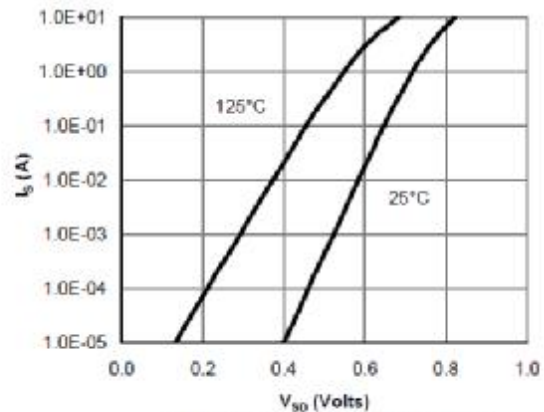


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

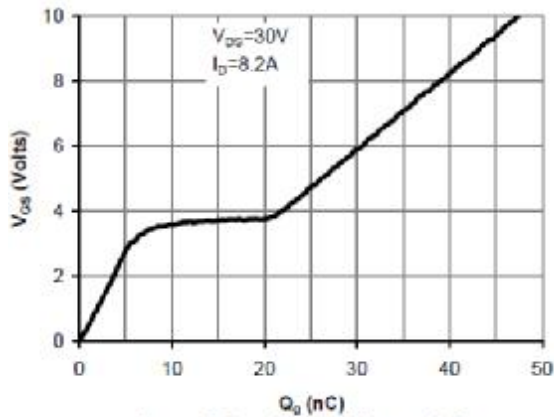


Figure 7: Gate-Charge Characteristics

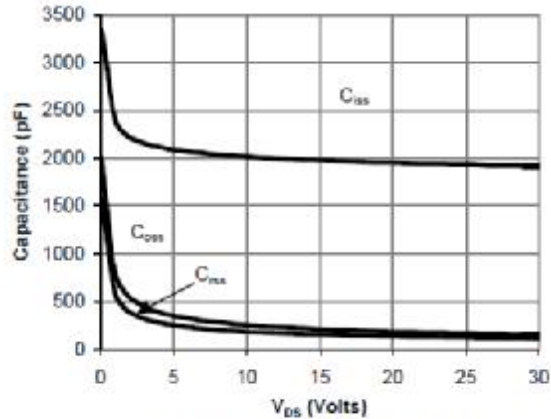


Figure 8: Capacitance Characteristics

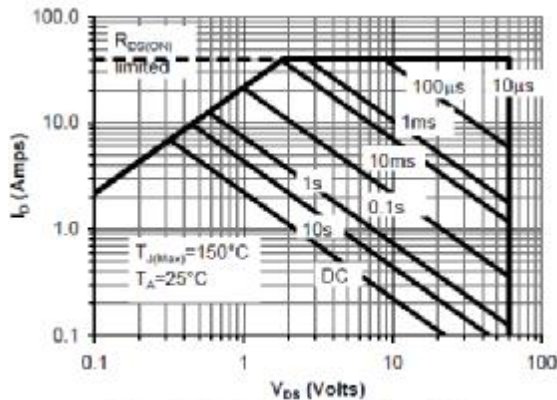


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

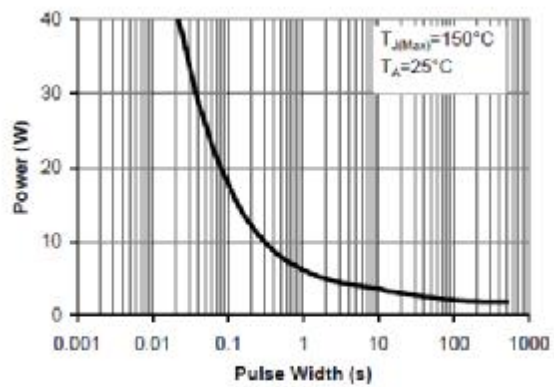


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

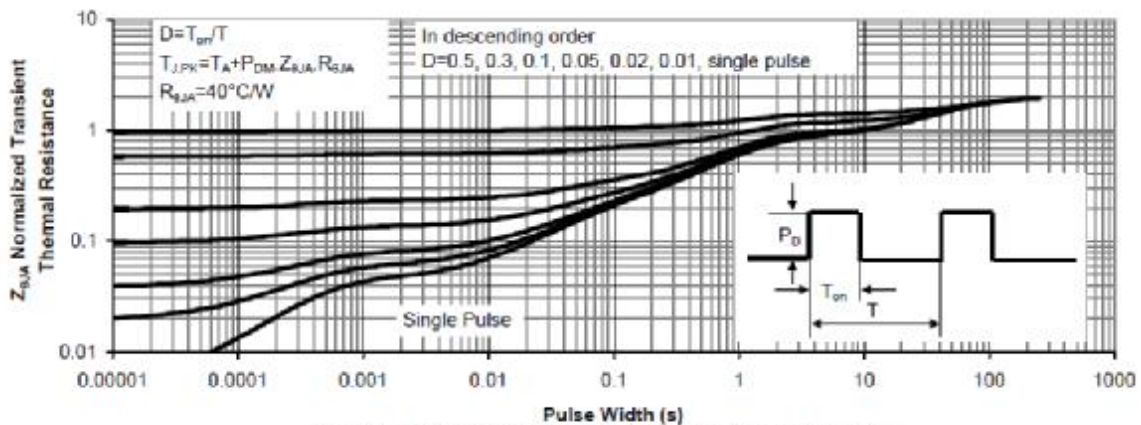
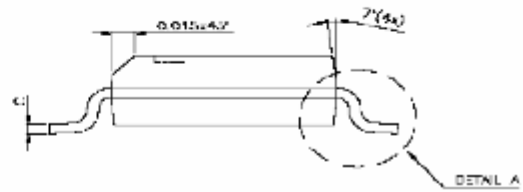
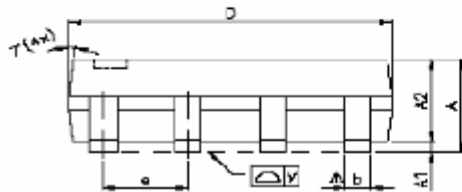
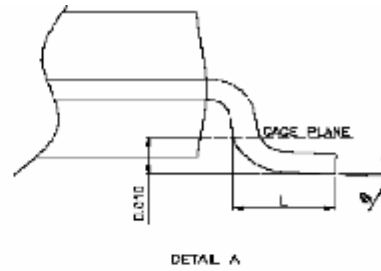
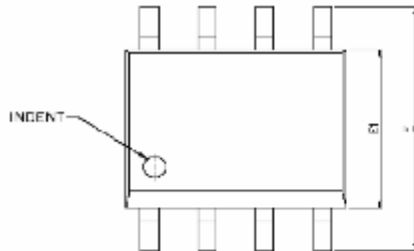


Figure 11: Normalized Maximum Transient Thermal Impedance

PACKAGE OUTLINE SOP-8P


SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.47	1.60	1.73	0.058	0.063	0.068
A1	0.10	—	0.25	0.004	—	0.010
A2	—	1.45	—	—	0.057	—
b	0.33	0.41	0.51	0.013	0.016	0.020
C	0.19	0.20	0.25	0.0075	0.008	0.0098
D	4.80	4.85	4.95	0.189	0.191	0.195
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e	—	1.27	—	—	0.050	—
L	0.38	0.71	1.27	0.015	0.028	0.050
Δ y	—	—	0.076	—	—	0.003
θ	0°	—	8°	0°	—	8°