STN4526

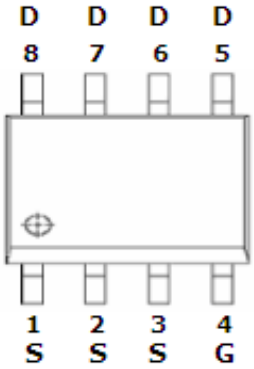
N Channel Enhancement Mode MOSFET

10.0A

DESCRIPTION

STN4526 is the N-Channel logic enhancement mode power field effect transistor which is produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as power management and other battery powered circuits where high-side switching.

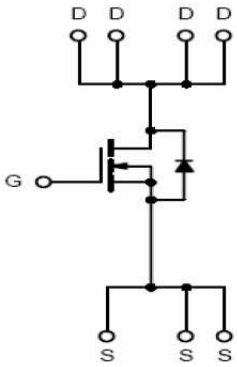
PIN CONFIGURATION
SOP-8



FEATURE

- 40V/10.0A, $R_{DS(ON)}$ = 25mΩ (Typ.) @V_{GS} = 10V
- 40V/8.0A, $R_{DS(ON)}$ = 31mΩ @V_{GS} = 4.5V
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- SOP-8 package design

PART MARKING



Y: Year Code A: Process Code

ORDERING INFORMATION

Part Number	Package	Part Marking
STN4526	SOP-8P	STN4526

※ Process Code : A ~ Z ; a ~ z

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ABSOULTE MAXIMUM RATINGS (Ta = 25℃ Unless otherwise noted)

Parameter		Symbol	Typical	Unit
Drain-Source Voltage		VDSS	40	V
Gate-Source Voltage		VGSS	±20	V
Continuous Drain Current (TJ=150℃)	TA=25℃ TA=70℃	ID	10.0 8.0	A
Pulsed Drain Current		IDM	30	A
Continuous Source Current (Diode Conduction)		IS	2.3	A
Power Dissipation	TA=25℃ TA=70℃	PD	2.5 1.6	W
Operation Junction Temperature		TJ	150	℃
Storgae Temperature Range		TSTG	-55/150	℃
Thermal Resistance-Junction to Ambient		RθJA	80	℃/W

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ELECTRICAL CHARACTERISTICS (Ta = 25℃ Unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V,ID=250uA	40			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},ID=250uA	1.0		3.0	V
Gate Leakage Current	I_{GSS}	V_{DS}=0V,V_{GS}=±20V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=40V,V_{GS}=0V			1	uA
		V_{DS}=40V,V_{GS}=0V T_J=85℃			10	
Drain-source On-Resistance	$R_{DS(on)}$	V_{GS}=10V,I_D=10A V_{GS}=4.5V,I_D=8A		25 31		mΩ
Forward Transconductance	gfs	V_{DS}=15V,I_D=6.2AV		13		S
Diode Forward Voltage	V_{SD}	I_S=2.3A,V_{GS}=0V		0.8	1.2	V
Dynamic						
Total Gate Charge	Q_g	V_{DS}=20V,V_{GS}=4.5 I_D≡5A		10	14	nC
Gate-Source Charge	Q_{gs}			2.8		
Gate-Drain Charge	Q_{gd}			3.2		
Input Capacitance	C_{iss}	V_{DS} =20V,VGS=0V F=1MHz		850		pF
Output Capacitance	C_{oss}			110		
Reverse TransferCapacitance	C_{rss}			75		
Turn-On Time	$t_{d(on)}$ tr	V_{DD}=20V,R_L= 4Ω I_D=5.0A,V_{GEN}=10V R_G=1Ω		6	12	nS
				10	20	
Turn-Off Time	$t_{d(off)}$ tf			20	36	
				6	12	

TYPICAL CHARACTERICTICS

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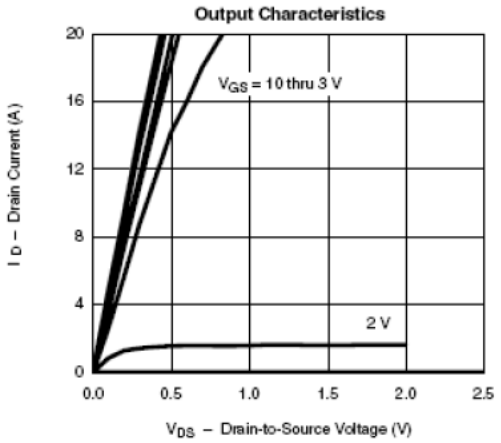

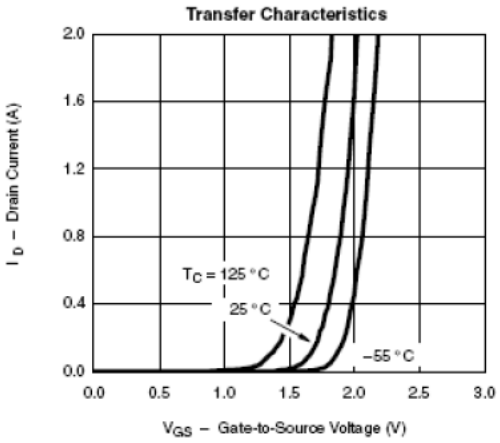

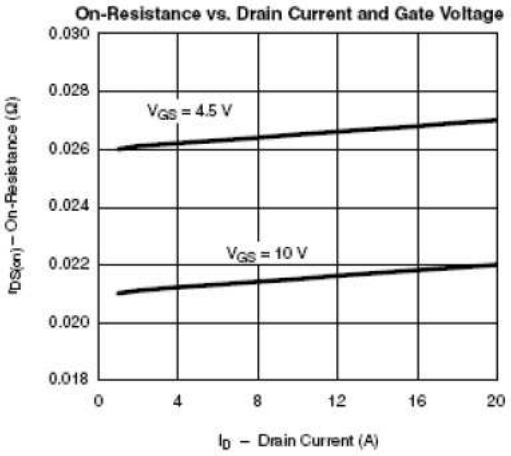

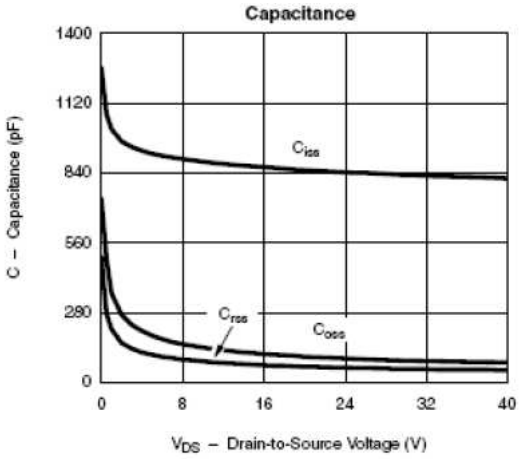

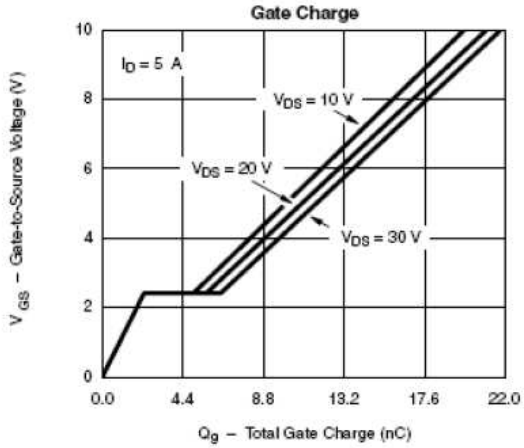

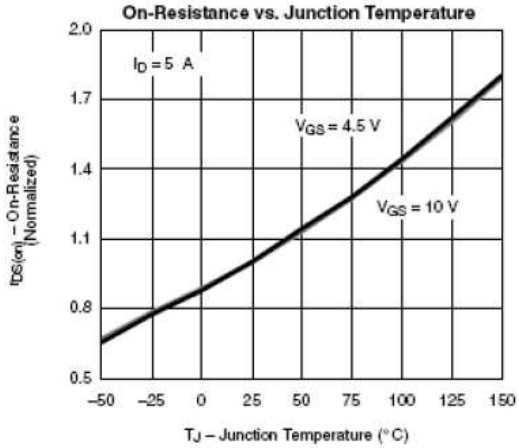

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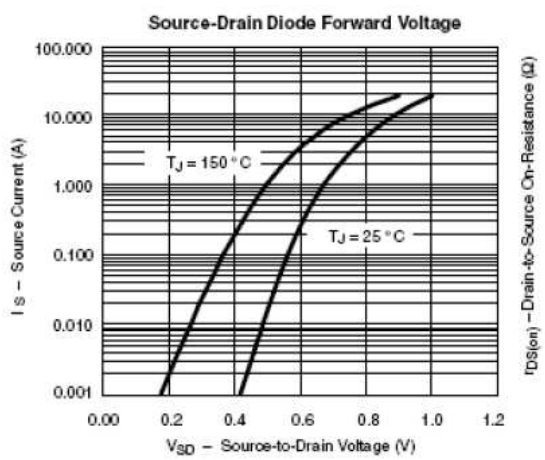

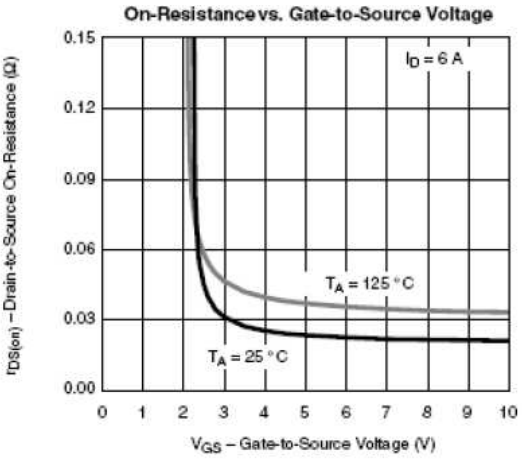

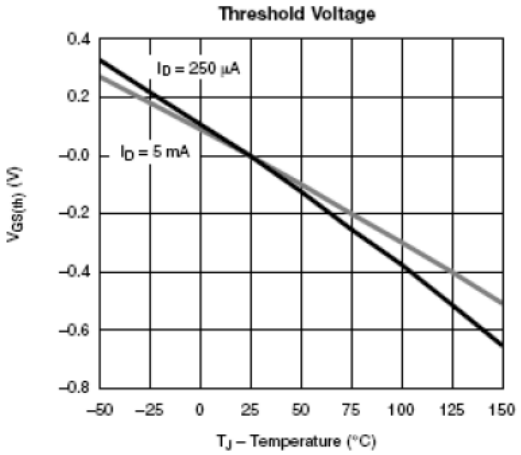

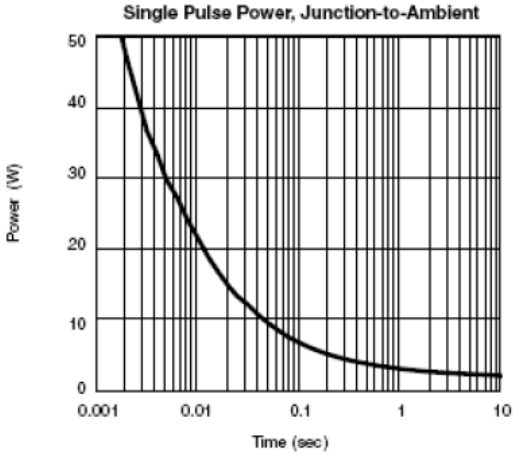

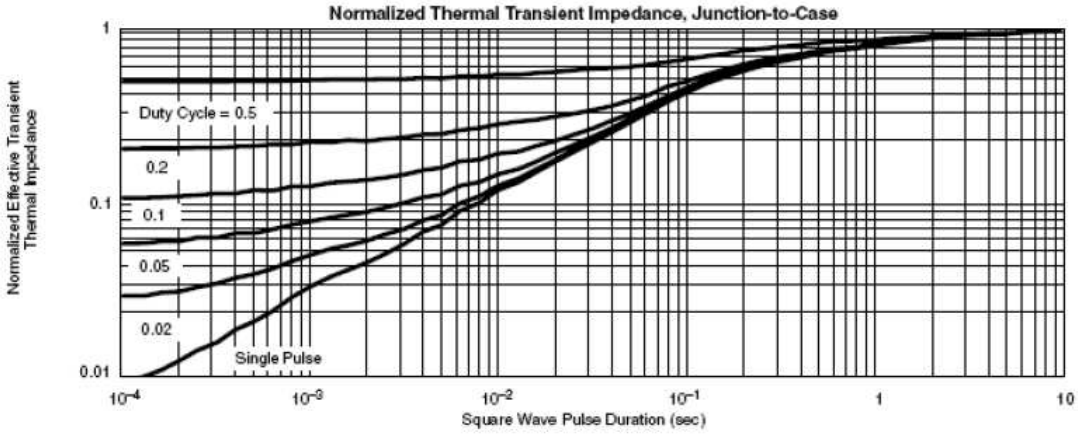

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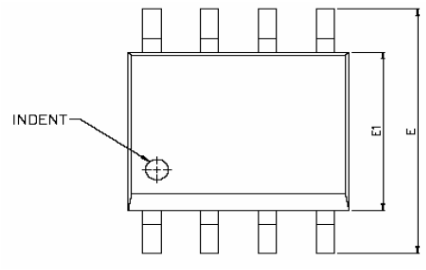
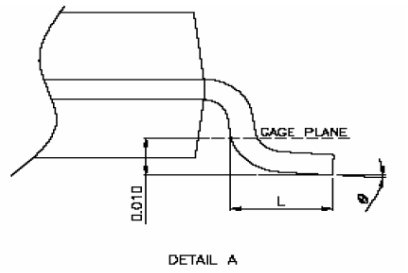
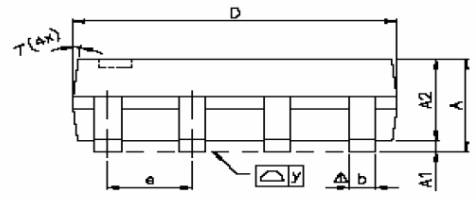
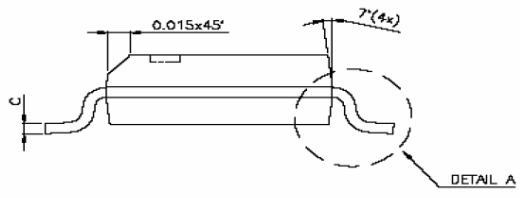
PACKAGE OUTLINE SOP-8P









SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.47	1.60	1.73	0.058	0.063	0.068
A1	0.10	——	0.25	0.004	——	0.010
A2	——	1.45	——	——	0.057	——
b	0.33	0.41	0.51	0.013	0.016	0.020
C	0.19	0.20	0.25	0.0075	0.008	0.0098
D	4.80	4.85	4.95	0.189	0.191	0.195
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e	——	1.27	——	——	0.050	——
L	0.38	0.71	1.27	0.015	0.028	0.050
② y	——	——	0.076	——	——	0.003
θ	0°	——	8°	0°	——	8°

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