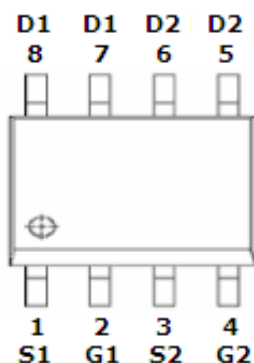


DESCRIPTION

The STN4826 is the Dual N-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application , notebook computer power management and other battery powered circuits where high-side switching .

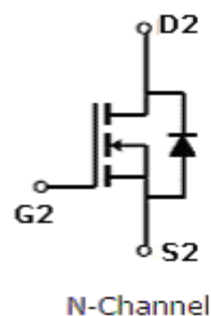
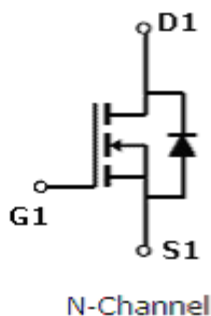
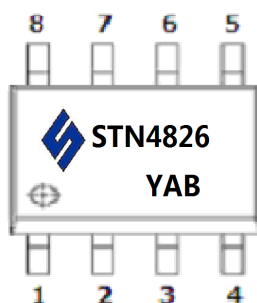
PIN CONFIGURATION SOP-8



FEATURE

- 60V/ 8.0A, $R_{DS(ON)} = 30m\Omega$ (Typ.) @VGS = 10V
- 60V/6.0A, $R_{DS(ON)} = 40m\Omega$ @VGS = 4.5V
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- SOP-8 package design

MARKING



Y: Year Code
A: Produce Code
B: Process Code



STN4826  Lead-free

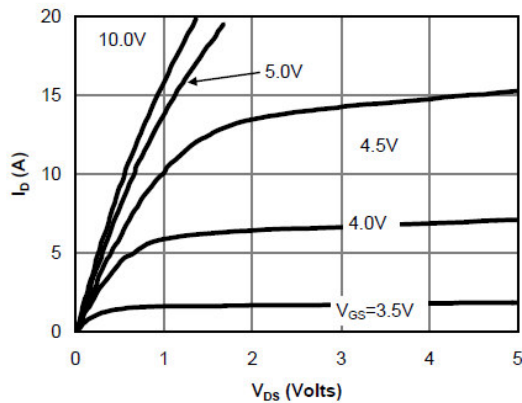
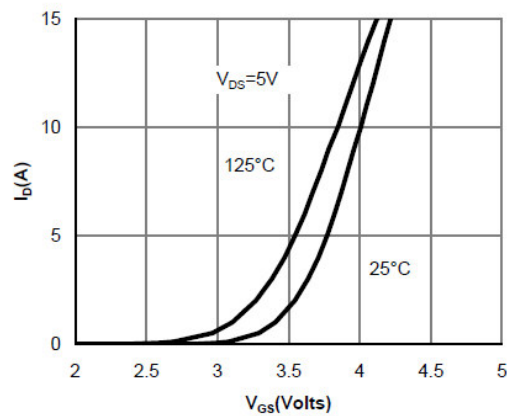
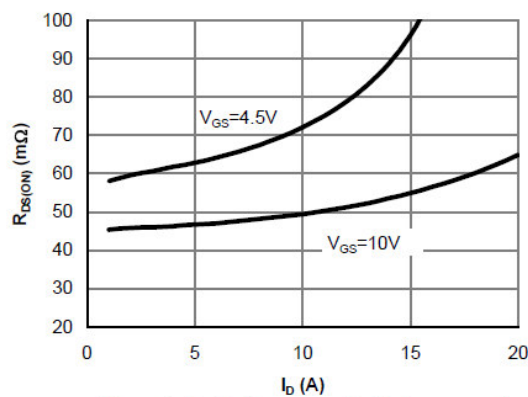
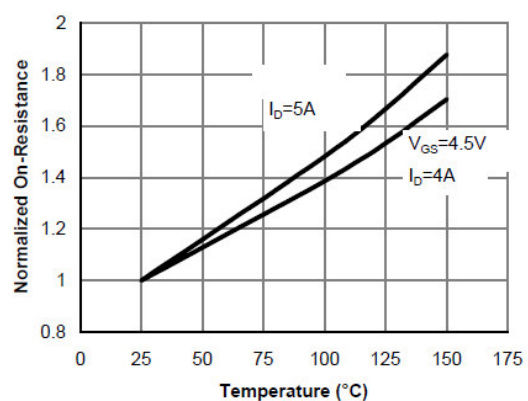
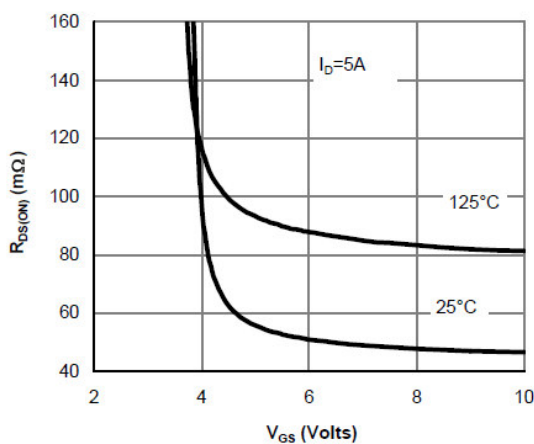
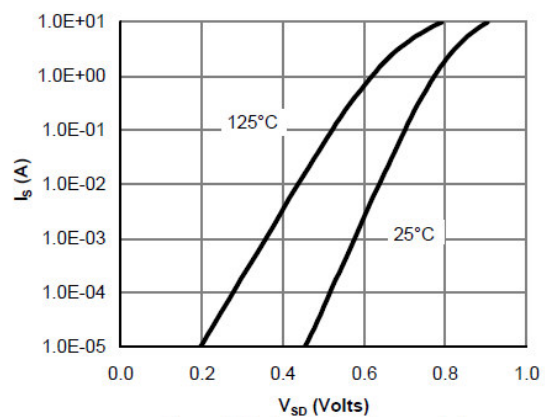
Dual N Channel Enhancement Mode MOSFET
8.0A

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C Unless otherwise noted)

Parameter		Symbol	Typical	Unit
Drain-Source Voltage		V _{DSS}	60	V
Gate-Source Voltage		V _{GSS}	±20	V
Continuous Drain Current (T _J =150°C)	T _A =25°C T _A =70°C	I _D	8.0 6.0	A
Pulsed Drain Current		I _{DM}	20	A
Continuous Source Current (Diode Conduction)		I _S	2.0	A
Power Dissipation	T _A =25°C T _A =70°C	P _D	2.0 1.3	W
Operation Junction Temperature		T _J	-55/150	°C
Storage Temperature Range		T _{STG}	-55/150	°C
Thermal Resistance-Junction to Ambient		R _{θJA}	75	°C/W

ELECTRICAL CHARACTERISTICS ($T_a = 25^{\circ}\text{C}$ Unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\mu A$	60			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\ \mu A$	0.8		2.5	V
Gate Leakage Current	I_{GSS}	$V_{DS}=0V, V_{GS}=\pm 20V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS} $T_J=55^{\circ}C$	$V_{DS}=48V, V_{GS}=0V$			1	uA
		$V_{DS}=48V, V_{GS}=0V$			5	
On-State Drain Current	$I_{D(on)}$	$V_{DS}\leq 5V, V_{GS}=4.5V$	20			A
Drain-source On-Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=8A$ $V_{GS}=4.5V, I_D=4A$		0.030 0.040	0.038 0.045	Ω
Forward Tran Conductance	g_{fs}	$V_{DS}=5.0V, I_D=5.3A$		11		S
Diode Forward Voltage	V_{SD}	$I_S=1.7A, V_{GS}=0V$		0.8	1.0	V
Dynamic						
Total Gate Charge	Q_g	$V_{DS}=15V, V_{GS}=10V$ $I_D\equiv 5.3A$		10		nC
Gate-Source Charge	Q_{gs}			3.5		
Gate-Drain Charge	Q_{gd}			3.6		
Input Capacitance	C_{iss}	$V_{DS}=15V, V_{GS}=0V$ $f=1MHz$		455		pF
Output Capacitance	C_{oss}			243		
Reverse TransferCapacitance	C_{rss}			45		
Turn-On Time	$t_{d(on)}^{tr}$	$V_{DD}=15V, R_L=15\Omega$ $I_D=1.4A, V_{GEN}=10V$ $R_G=6\Omega$		10	14	nS
				10	20	
Turn-Off Time	$t_{d(off)}^{tf}$			20	35	
				10	15	

TYPICAL CHARACTERISTICS (25°C Unless Note)

Fig 1: On-Region Characteristics

Figure 2: Transfer Characteristics

Figure 3: On-Resistance vs. Drain Current and Gate Voltage

Figure 4: On-Resistance vs. Junction Temperature

Figure 5: On-Resistance vs. Gate-Source Voltage

Figure 6: Body-Diode Characteristics

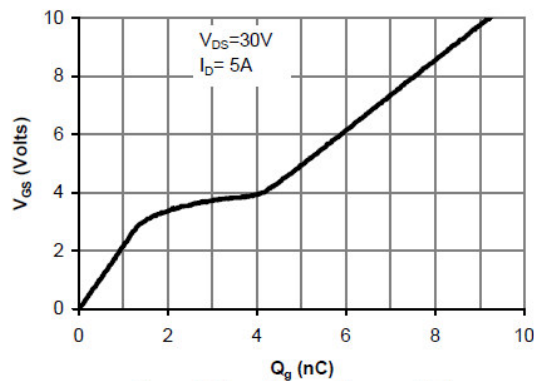


Figure 7: Gate-Charge Characteristics

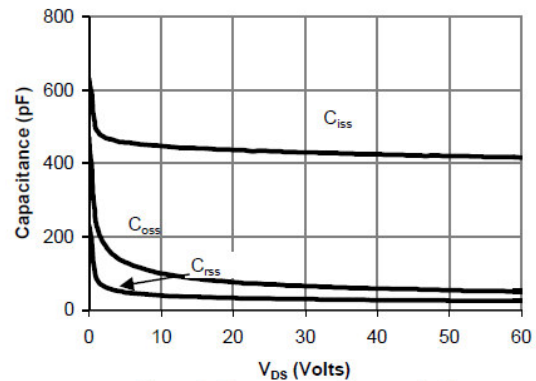


Figure 8: Capacitance Characteristics

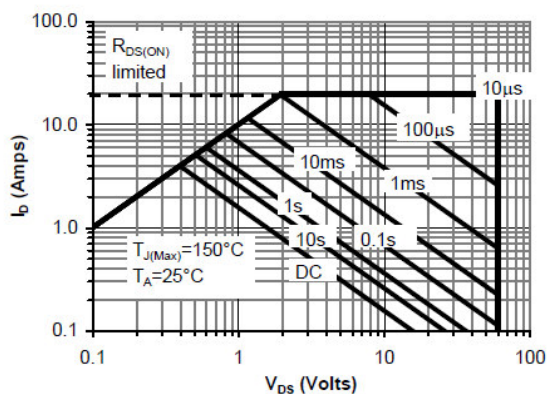


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

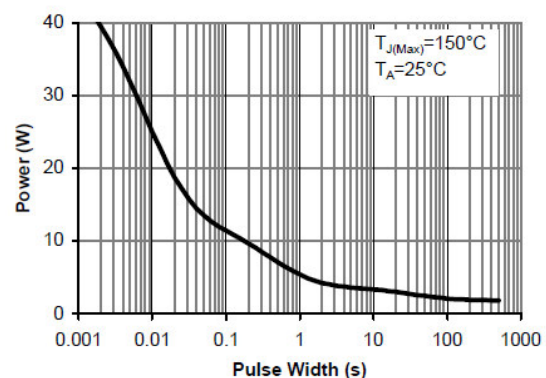


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

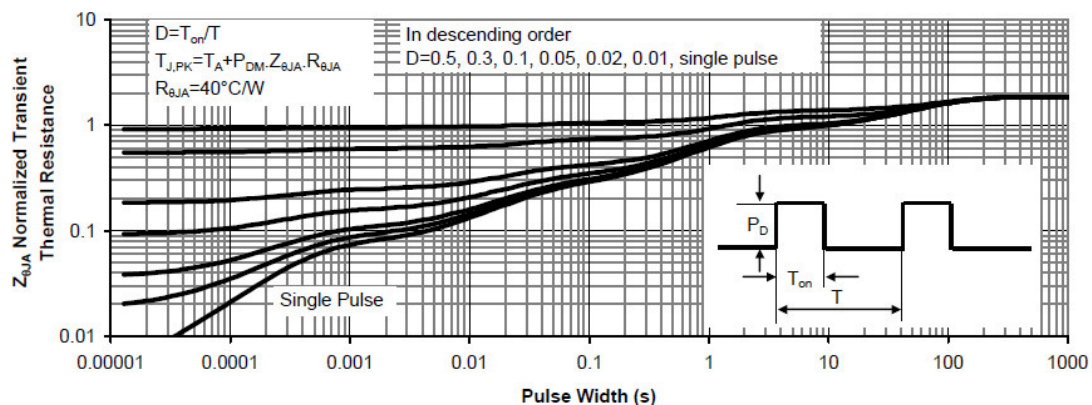
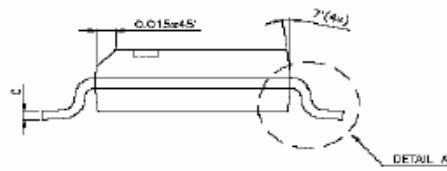
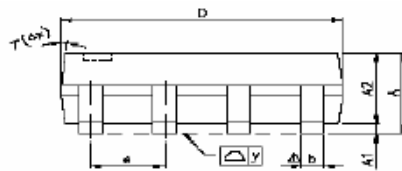
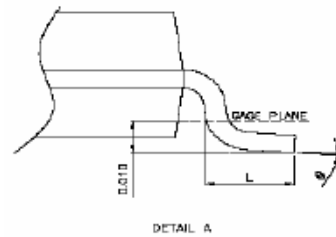
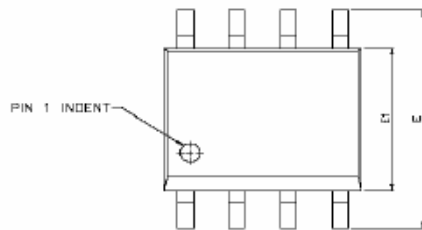


Figure 11: Normalized Maximum Transient Thermal Impedance

SOP-8 PACKAGE OUTLINE


SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.47	1.60	1.73	0.058	0.063	0.068
A1	0.10	—	0.25	0.004	—	0.010
A2	—	1.45	—	—	0.057	—
b	0.33	0.41	0.51	0.013	0.016	0.020
C	0.19	0.20	0.25	0.0075	0.008	0.0098
D	4.80	4.85	4.95	0.189	0.191	0.195
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e	—	1.27	—	—	0.050	—
L	0.38	0.71	1.27	0.015	0.028	0.050
y	—	—	0.076	—	—	0.003
θ	0°	—	8°	0°	—	8°