SemTron Microtech Corporation

STN4842

30V Dual N-Channel Enhancement Mode MOSFET

Dual N-Channel Enhancement Mode

DESCRIPTION

The STN4842 is the Dual N-Channel logic enhancement mode power field effect transistor is produced using high cell density. advanced trench technology to provide excellent $R_{DS(ON)}$.
This device is suitable for use as a load switch or in PWM and gate charge for most of the synchronous buck converter applications.

STN4842M-TRG ROHS Compliant This is Halogen Free

FEATURE

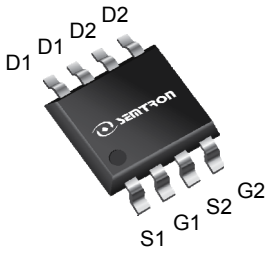
- ***30V / 7.8A, $R_{DS(ON)}$ =16mΩ(typ.)@V_{GS} =10V***
- ***30V / 5.8A, $R_{DS(ON)}$ =24mΩ(typ.)@V_{GS} =4.5V***
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and Maximum DC current capability

APPLICATIONS

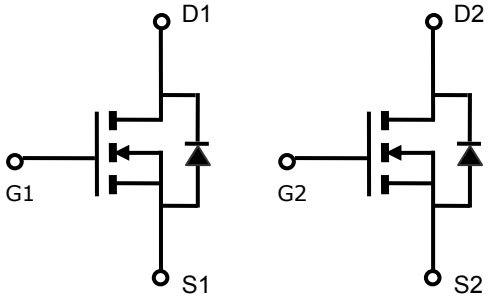
- High Frequency Point-of-Load Synchronous
- Newworking DC-DC Power System
- Load Switch

Green Product

PIN CONFIGURATION



SOP-8
Top View



PART NUMBER INFORMATION

ST N 4842 M - TR G a b c d e f	**a : Company name.** **b : Channel type.** **c : Product Serial number.** **d : Package code** **e : Handling code** **f : Green product code**

■ ORDERING INFORMATION

Part Number	Package Code	Handling Code	Shipping
STN4842M-TRG	M : SOP-8	TR : Tape&Reel	2.5K/Reel

※ Year Code : 00 ~ 90, 2010 : 00
※ Week Code : 01 ~ 54
※ SOP-8 : Only available in tape and reel packaging.

■ ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless otherwise noted)

Symbol	Parameter		Typical	Unit
V_{DSS}	Drain-Source Voltage		30	V
V_{GSS}	Gate-Source Voltage		±20	V
I_D	Continuous Drain Current, V_{GS}=10V[A]	T_A=25°C	7.8	A
		T_A=70°C	6.5	
I_{DM}	Pulsed Drain Current[B]		25	A
E_{AS}	Single Pulse Avalanche energy L=0.1mH [C]		27	mJ
I_{AS}	Avalanche Current		14	A
P_D	Power Dissipation	T_A=25°C T_A=70°C	2.0 1.4	W
T_J	Operation Junction Temperature		-55/150	°C
T_{STG}	Storage Temperature Range		-55/150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.
Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ THERMAL DATA

Symbol	Parameter		Min	Typ	Max	Unit
$R_{\theta JA}$	Thermal Resistance-Junction to Ambient[A]	Steady-State			85	°C/W
$R_{\theta JC}$	Thermal Resistance Junction to Lead[A]	Steady-State			50	°C/W

■ELECTRICAL CHARACTERISTICS(T_A = 25°C Unless otherwise noted)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Static Parameters						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS} =0V,I_D =250μA	30			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} =V_{GS},I_D =250μA	1.0		2.5	V
I_{GSS}	Gate Leakage Current	V_{DS} =0V,V_{GS}=±20V			±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} =24V,V_{GS} =0V T_J =25°C			1	μA
		V_{DS} =24V,V_{GS} =0V T_J =55°C			5	
$R_{DS(ON)}$	Drain-source On-Resistance[B]	V_{GS} =10V,I_D=7.8A V_{GS} =4.5V, I_D=5.8A		16 24	20 30	mΩ
G_{fs}	Forward Transconductance	V_{DS} =10V,I_D =6A		5.6		S
Source-Drain Doide						
V_{SD}	Diode Forward Voltage[B]	I_S=1.7A,V_{GS}=0V		0.75	1.0	V
I_S	Continuous Source Current[AD]				5.8	A
Dynamic Parameters						
Q_g (4.5V)	Total Gate Charge	V_{DS} =15V,V_{GS} =4.5V I_D =5.8A		5	7.2	nC
Q_{gs}	Gate-Source Charge			1.6		
Q_{gd}	Gate-Drain Charge			1.9		
C_{iss}	Input Capacitance	V_{DS} =15V,V_{GS} =0V f =1MHz		420	586	pF
C_{oss}	Output Capacitance			65		
C_{rss}	Reverse Transfer Capacitance			52		
$t_{d(on)}$	Turn-On Time	V_{DD}=15V, V_{GEN}=10V, R_G=3.3Ω,		2.2	4.4	nS
t_r				38.7	68.8	
$t_{d(off)}$	Turn-Off Time			12.5	25	
t_f				4.8	9.6	

Note:

A. The value of R $_{\theta JA}$ is measured with the device mounted on 1in 2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C.

B. The data tested by pulsed , pulse width ≦ 300uS , duty cycle ≦ 2%

C. The EAS data shows Max. rating . The test condition is V_{DD}=25V,V_{GS}=10V,L=0.1mH.

D. The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

The products and product specifications contained herein are subject to change without notice to improve performance characteristics. Consult us, or our representatives before use, to confirm that the information in this datasheet is up to date

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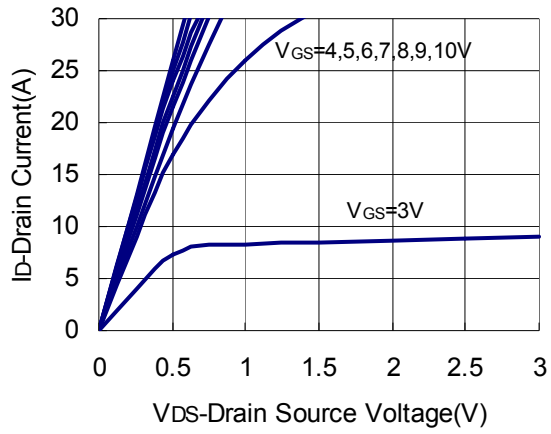
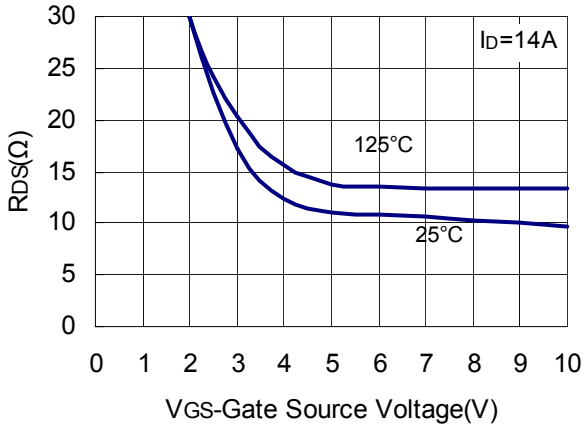
TYPICAL CHARACTERISTICS

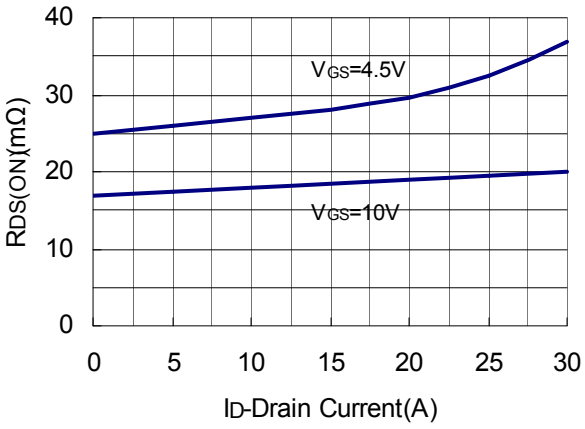
Output Characteristics



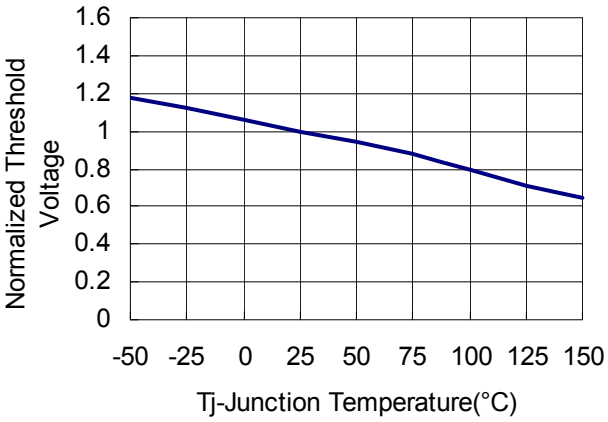
On Resistance VS Gate Source Voltage



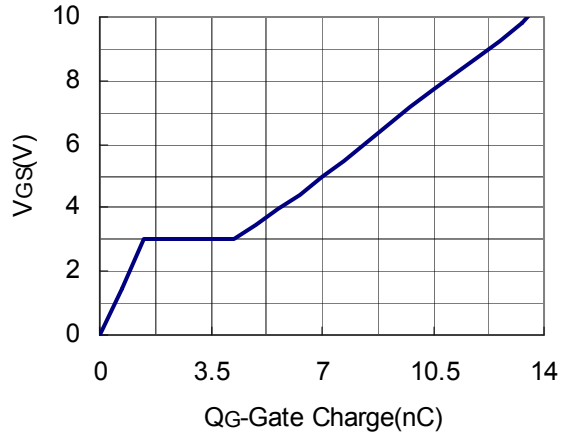
Drain Source On Resistance



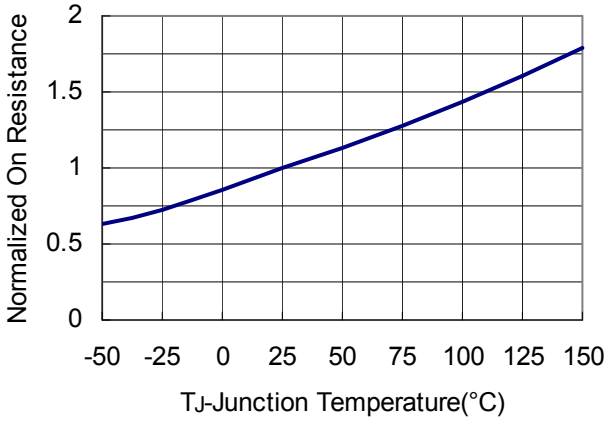
Gate Threshold Voltage



Gate Charge

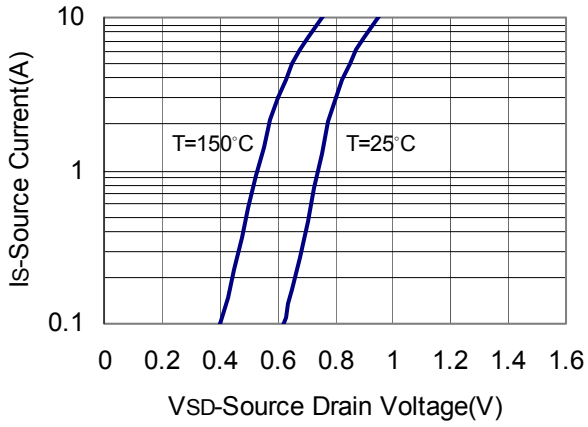


Drain Source On Resistance

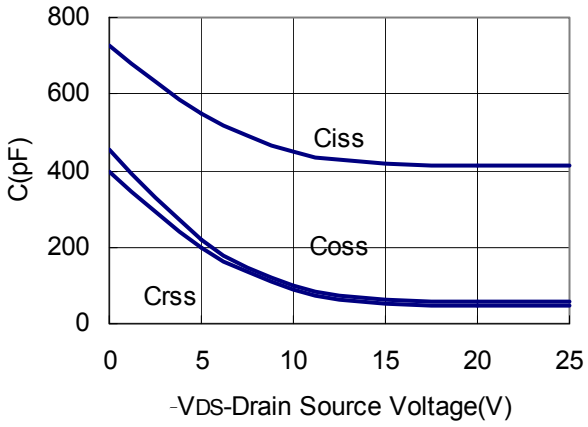


TYPICAL CHARACTERISTICS

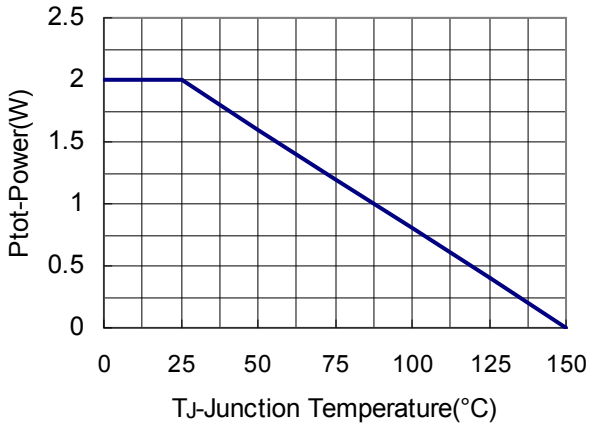
Source Drain Diode Forward



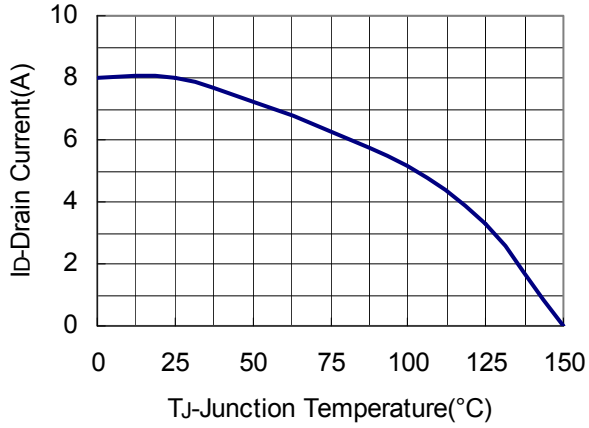
Capacitance



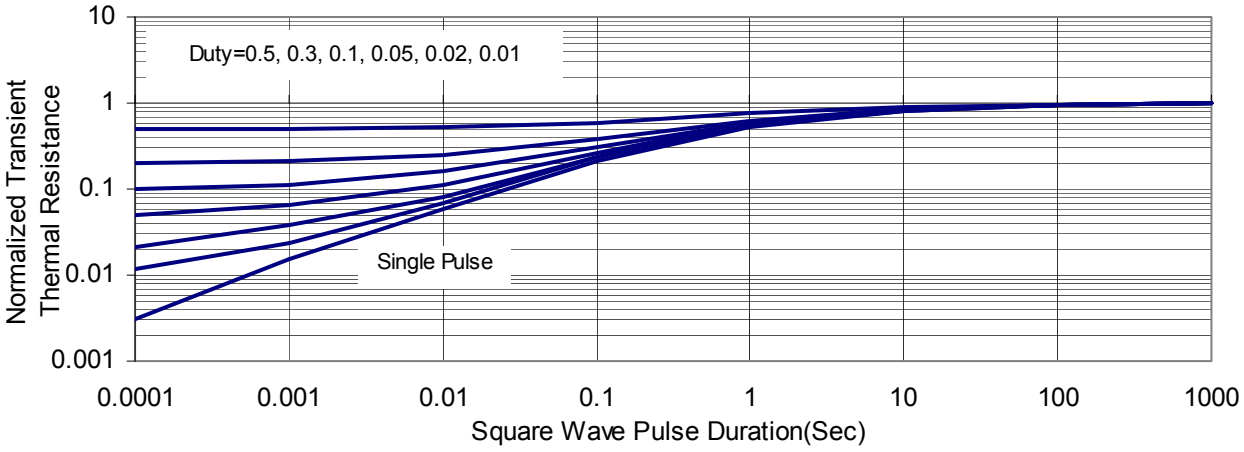
Power Dissipation



Drain Current



Thermal Transient Impedance



SOP-8 PACKAGE DIMENSIONS

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.040	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 BSC		0.050 BSC	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°