



STN484D



N Channel Enhancement Mode MOSFET

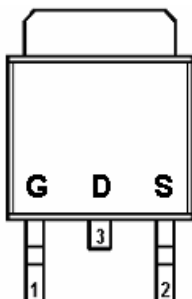
30.0A

DESCRIPTION

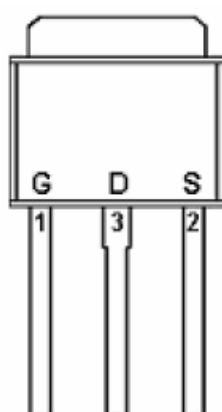
STN484D is the N-Channel logic enhancement mode power field effect transistor which is produced using high cell density, DMOS trench technology. The STN484D has been designed specially to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low $R_{DS(ON)}$ and fast switching speed.

PIN CONFIGURATION

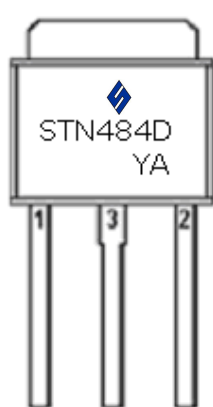
TO-252



TO-251

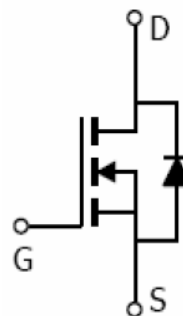


PART MARKING



FEATURE

- 30V/20.0A, $R_{DS(ON)} = 8m\Omega$ (Typ.)
@ $V_{GS} = 10V$
- 30V/15.0A, $R_{DS(ON)} = 12m\Omega$
@ $V_{GS} = 4.5V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- TO-252, TO-251 package design



Y: Year Code A: Process Code

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ABSOLUTE MAXIMUM RATINGS (Ta = 25°C Unless otherwise noted)

Parameter		Symbol	Typical	Unit
Drain-Source Voltage		VDSS	30	V
Gate-Source Voltage		VGSS	±20	V
Continuous Drain Current (TJ=150°C)	TA=25°C TA=70°C	ID	30.0 20.0	A
Pulsed Drain Current		IDM	80	A
Continuous Source Current (Diode Conduction)		IS	21	A
Power Dissipation	TA=25°C TA=70°C	PD	50 25	W
Operation Junction Temperature		TJ	150	°C
Storage Temperature Range		TSTG	-55/150	°C
Thermal Resistance-Junction to Ambient		RθJA	60	°C/W


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ELECTRICAL CHARACTERISTICS (Ta = 25°C Unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\mu A$	30			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1.0		2.5	V
Gate Leakage Current	I_{GSS}	$V_{DS}=0V, V_{GS}=\pm 20V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=24V, V_{GS}=0V$			1	uA
		$V_{DS}=24V, V_{GS}=0V$ $T_J=55^{\circ}C$			5	
On-State Drain Current	$I_{D(on)}$	$V_{DS}\geq 5V, V_{GS}=10V$	80			A
Drain-source On-Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=20A$ $V_{GS}=4.5V, I_D=15A$		8 12	13 18	mΩ
Forward Transconductance	gfs	$V_{DS}=5V, I_D=12A$		25		S
Diode Forward Voltage	V_{SD}	$I_S=1.0A, V_{GS}=0V$			1.2	V
Dynamic						
Total Gate Charge	Q_g	$V_{DS}=10V, V_{DS}=15V$ $I_D=20A$		19	22	nC
Gate-Source Charge	Q_{gs}			3.2		
Gate-Drain Charge	Q_{gd}			4.5		
Input Capacitance	C_{iss}	$V_{DS}=20V, V_{GS}=0V$ $F=1MHz$		950		pF
Output Capacitance	C_{oss}			145		
Reverse TransferCapacitance	C_{rss}			99		
Turn-On Time	$t_{d(on)}$ t_r	$V_{DD}=20V, R_L=4\Omega$ $I_D=5.0A, V_{GEN}=10V$ $R_G=1\Omega$		6		nS
Turn-Off Time	$t_{d(off)}$ t_f			12		
				20		
				6		



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TYPICAL CHARACTERISTICS

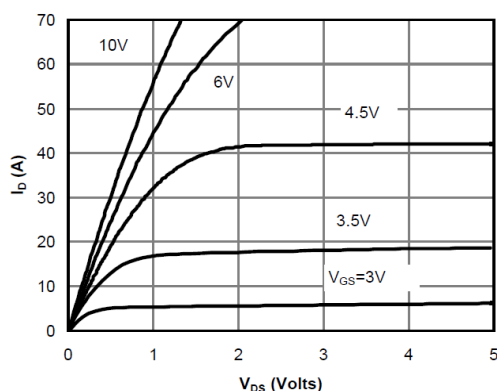


Figure 1: On-Region Characteristics

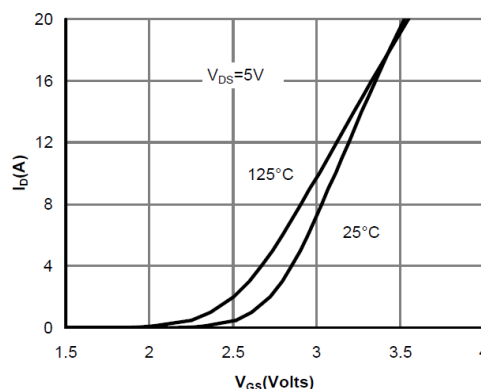


Figure 2: Transfer Characteristics

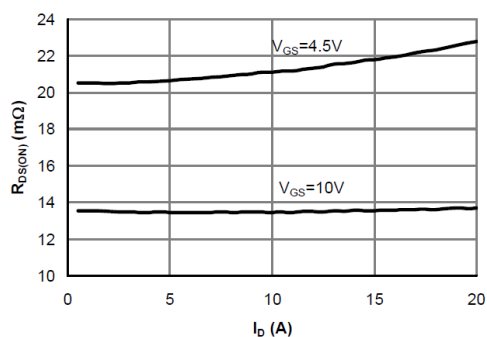


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

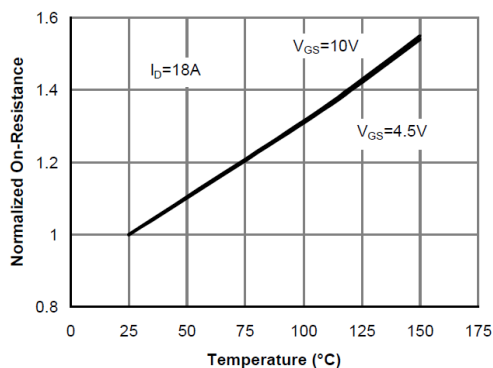


Figure 4: On-Resistance vs. Junction Temperature

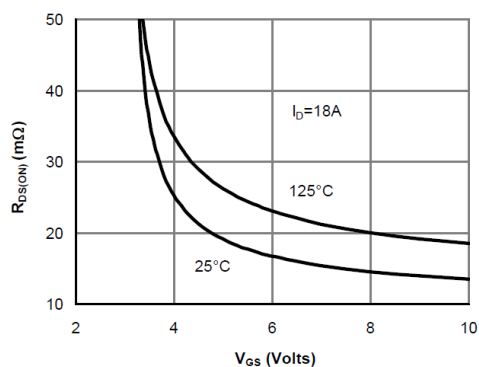


Figure 5: On-Resistance vs. Gate-Source Voltage

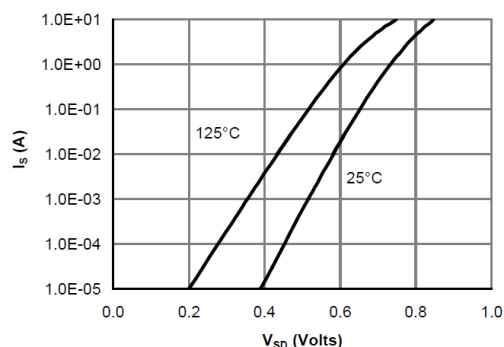


Figure 6: Body-Diode Characteristics



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TYPICAL CHARACTERISTICS

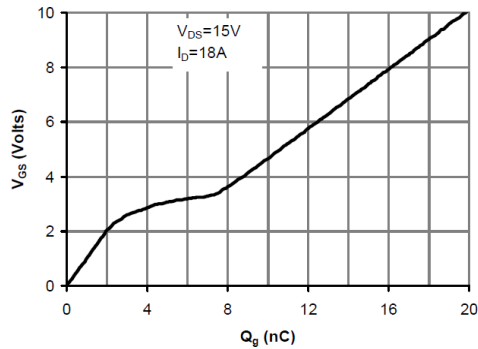


Figure 7: Gate-Charge Characteristics

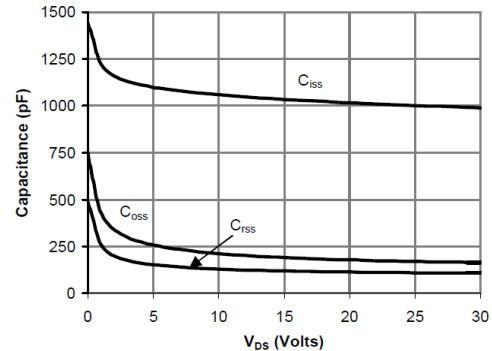


Figure 8: Capacitance Characteristics

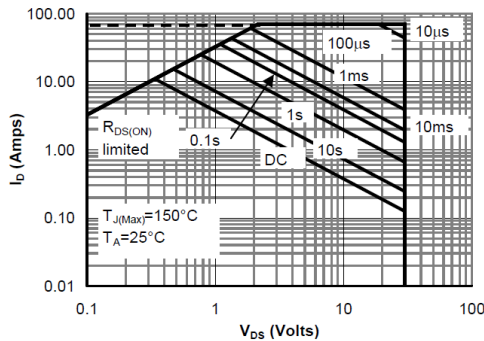


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

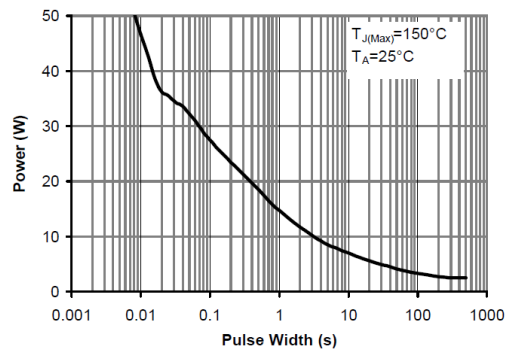


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note F)

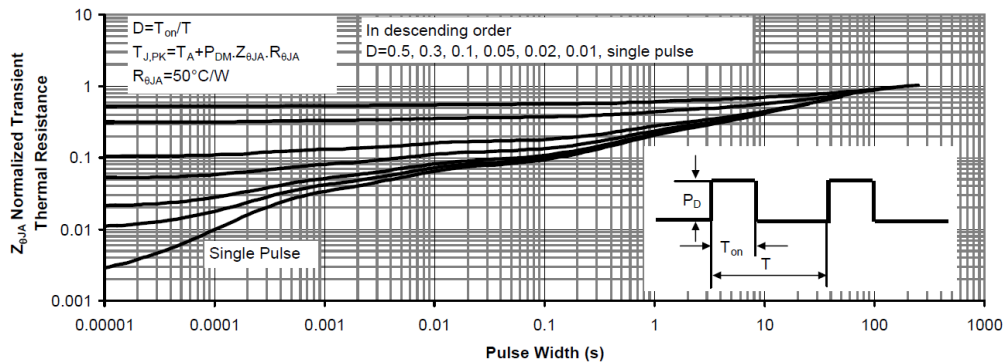


Figure 11: Normalized Maximum Transient Thermal Impedance

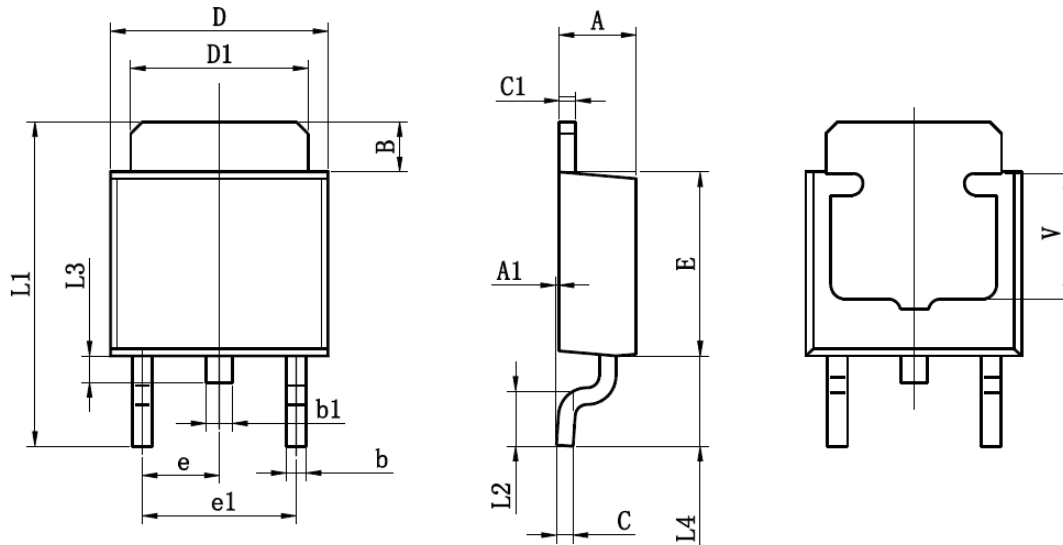


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TO-252-2L PACKAGE OUTLINE SOP-8P



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	2.200	2.400	0.087	0.094
A1	0.000	0.127	0.000	0.005
B	1.350	1.650	0.053	0.065
b	0.500	0.700	0.020	0.028
b1	0.700	0.900	0.028	0.035
c	0.430	0.580	0.017	0.023
c1	0.430	0.580	0.017	0.023
D	6.350	6.650	0.250	0.262
D1	5.200	5.400	0.205	0.213
E	5.400	5.700	0.213	0.224
e	2.300TYP		0.091TYP	
e1	4.500	4.700	0.177	0.185
L1	9.500	9.900	0.374	0.390
L2	1.400	1.780	0.055	0.070
L3	0.650	0.950	0.026	0.037
L4	2.550	2.900	0.100	0.114
V	3.80REF		0.150REF	

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