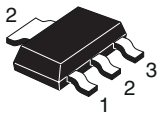
STN5PF02V

P-channel 20V - 0.065Ω - 4.2A - SOT-223
2.5V - Drive STripFET™ II Power MOSFET

General features

Type	V_{DSS}	$R_{DS(on)}$	I_D
STN5PF02V	20V	<0.080Ω	4.2A

- Ultra low threshold gate drive (2.5V)
- Standard outline for easy automated surface mount assembly

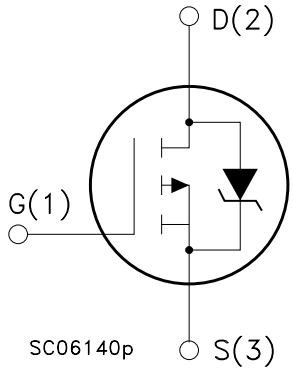


SOT-223

Description

This Power MOSFET is the latest development of STMicroelectronics unique “single feature size™” strip-based process. The resulting transistor shows extremely extremely low on-resistance when driven at 2.5V.

Internal schematic diagram



Applications

- Switching application

Order codes

Part number	Marking	Package	Packaging
STN5PF02V	N5PF02V	SOT-223	Tape & reel

Contents

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage (V_{GS} = 0)	20	V
V_{GS}	Gate- source voltage	± 8	V
I_D	Drain current (continuous) at T_C = 25°C	4.2	A
I_D	Drain current (continuous) at T_C = 100°C	2.6	A
I_{DM} (1)	Drain current (pulsed)	17	A
P_{TOT}	Total dissipation at T_C = 25°C	2.5	W
T_j T_{stg}	Max. operating junction temperature Storage temperature	–55 to 150	°C

1. Pulse width limited by safe operating area

Note: For the p-channel Power MOSFET actual polarity of voltages and current has to be reversed

Table 2. Thermal resistance

Symbol	Parameter	Max value	Unit
Rthj-pcb (1)	Thermal resistance junction-pc board	50	°C/W
Rthj-amb	Thermal resistance junction-ambient	90	°C/W

1. When mounted on FR-4 board of 1inch² pad, 2oz Cu and tc< 10sec

2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Table 3. On/off states

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 250µA, V_{GS} = 0	20			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max rating V_{DS} = Max rating,@125°C			1 10	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 8V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250µA	0.45			V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 4.5V, I_D = 2.1A V_{GS} = 2.5V, I_D = 2.1A		0.065 0.085	0.080 0.10	Ω Ω

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
g_{fs} (1)	Forward transconductance	V_{DS} = 15V , I_D = 2.5A		6.6		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 15V, f = 1 MHz, V_{GS} = 0		412 179 42.5		pF pF pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 10V, I_D = 4.2A, V_{GS} = 2.5V *(see Figure 13)*		4.5 0.73 1.75	6	nC nC nC

1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %

Table 5. Switching times

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on delay time Rise time Turn-off-delay time Fall time	V_{DD} = 10V, I_D = 2.1A R_G = 4.7Ω , V_{GS} = 2.5V *(see Figure 12)*		11 47 38 20		ns ns ns ns

Table 6. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
I_{SD} I_{SDM} (1)	Source-drain current Source-drain current (pulsed)				4.2 17	A A
V_{SD} (2)	Forward on voltage	I_{SD} = 4.2A, V_{GS} = 0			1.2	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 4.2A, di/dt=100A/µs, V_{DD} = 16V, T_j = 150°C *(see Figure 14)*		32 12.8 0.8		ns nC A

1. Pulse width limited by safe operating area
2. Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

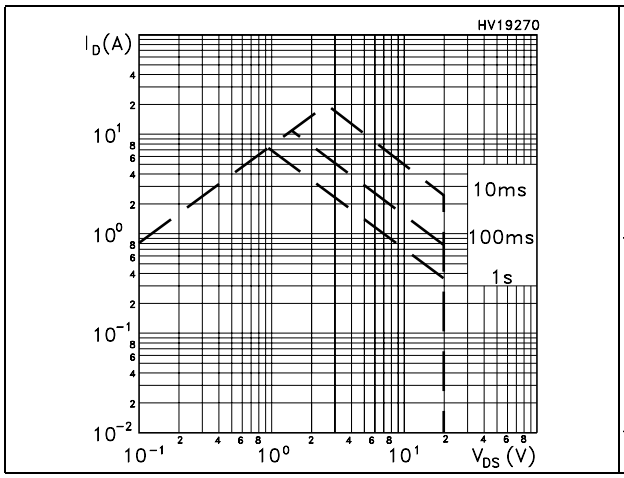


Figure 2. Thermal inpedance

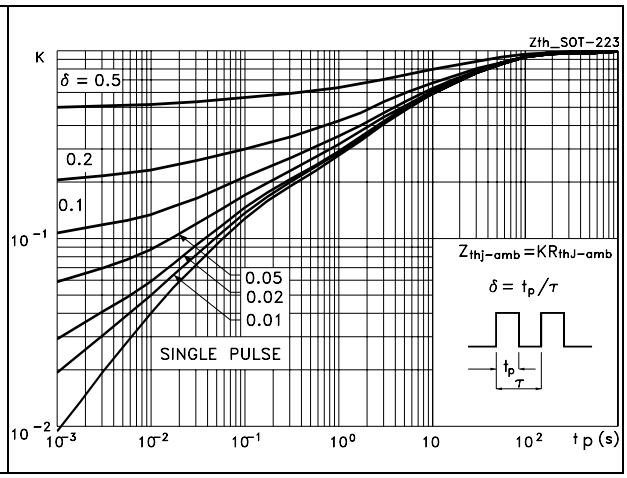


Figure 3. Output characteristics

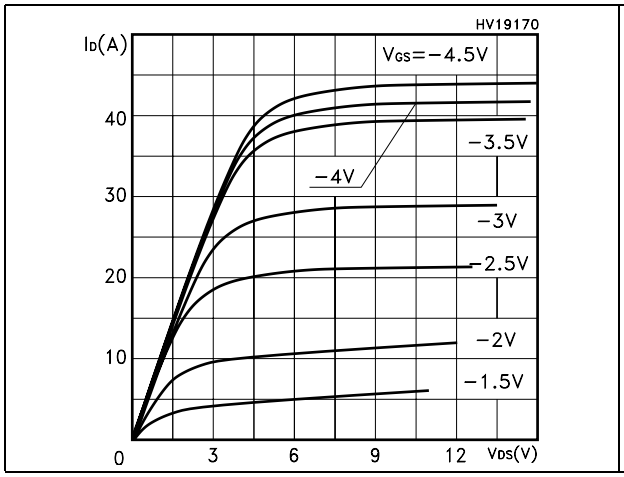


Figure 4. Transfer characteristics

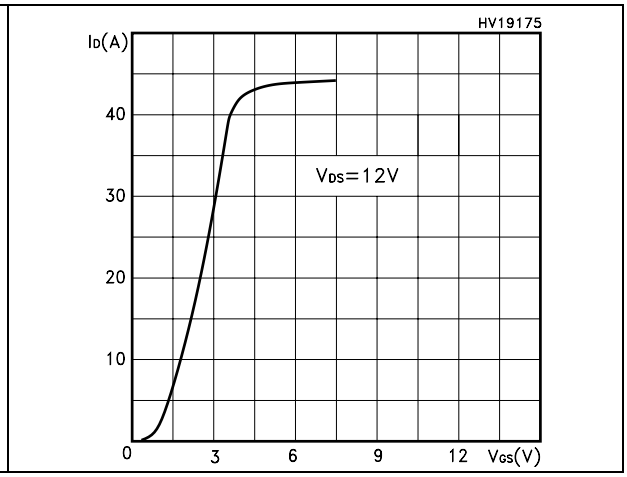


Figure 5. Transconductance

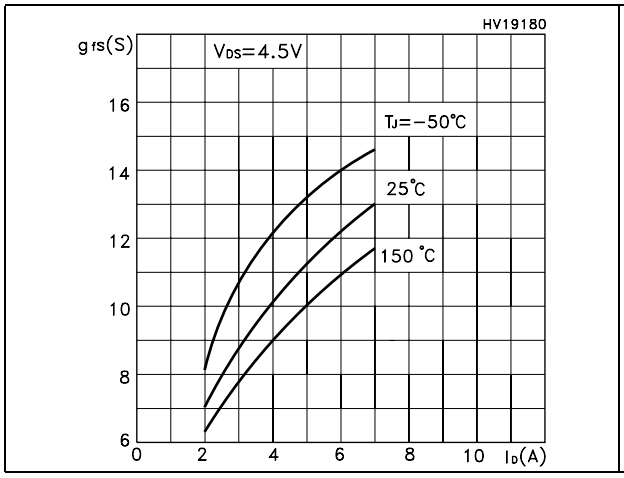


Figure 6. Static drain-source on resistance

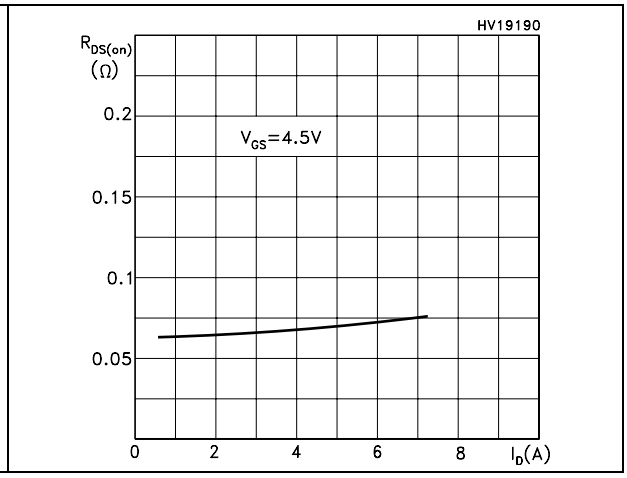


Figure 7. Gate charge vs gate-source voltage

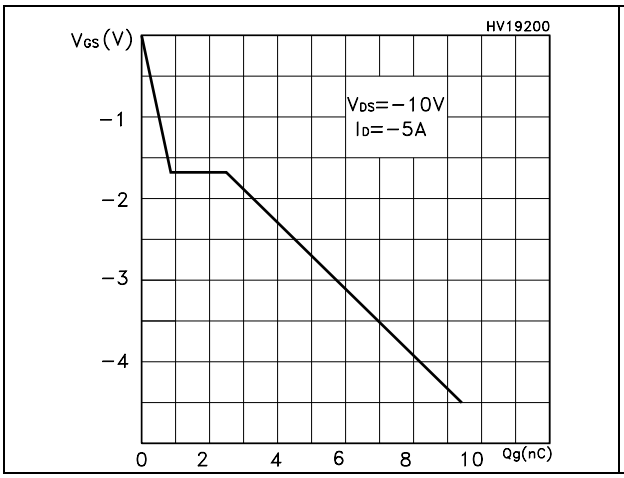


Figure 8. Capacitance variations

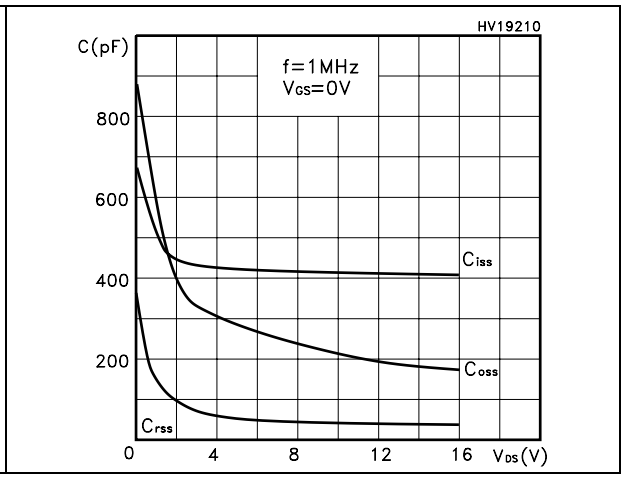


Figure 9. Normalized gate threshold voltage vs temperature

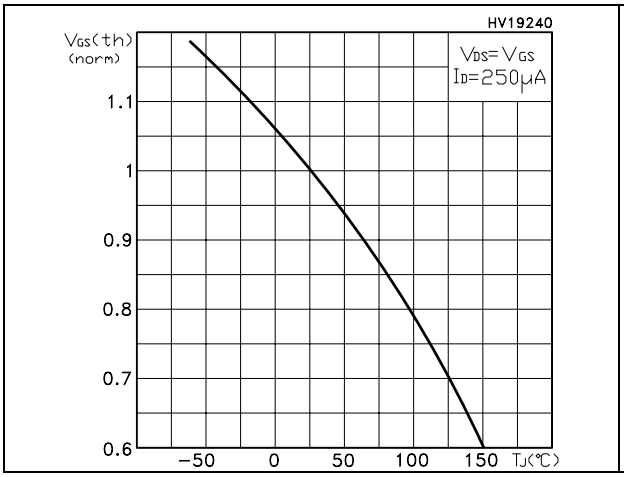


Figure 10. Normalized on resistance vs temperature

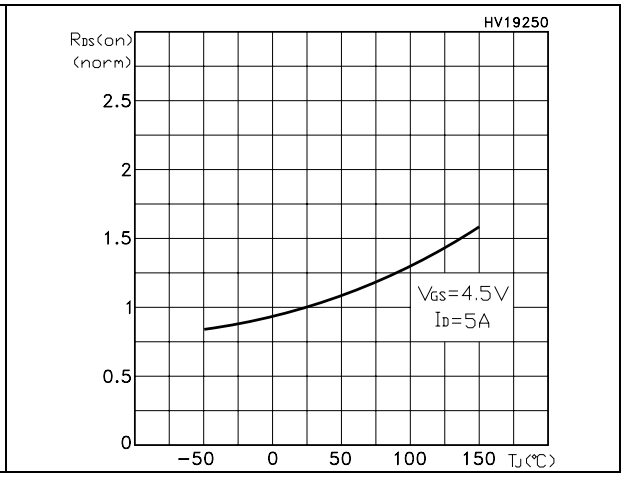
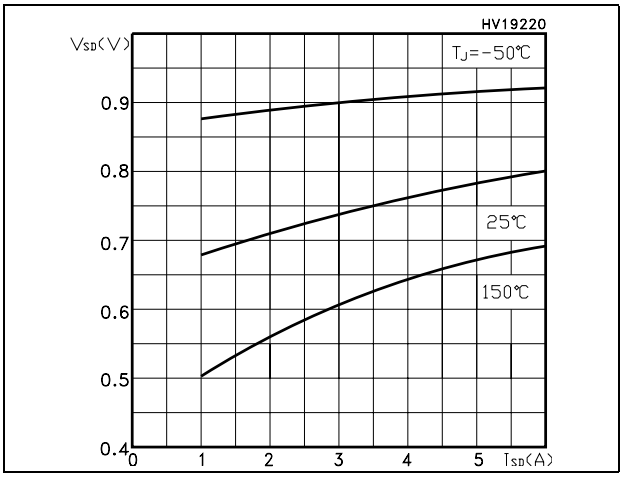


Figure 11. Source-drain diode forward characteristics



3 Test circuit

Figure 12. Switching times test circuit for resistive load

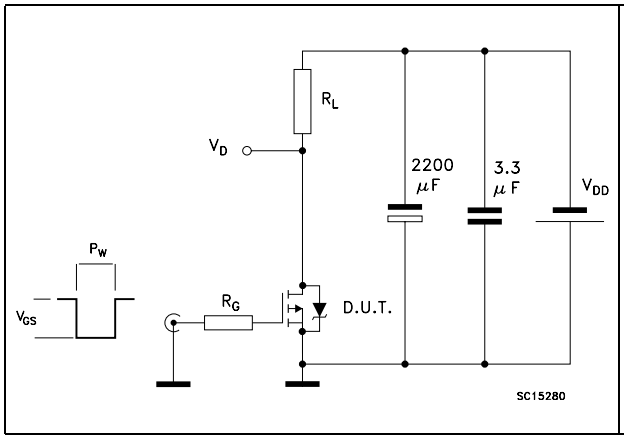


Figure 13. Gate charge test circuit

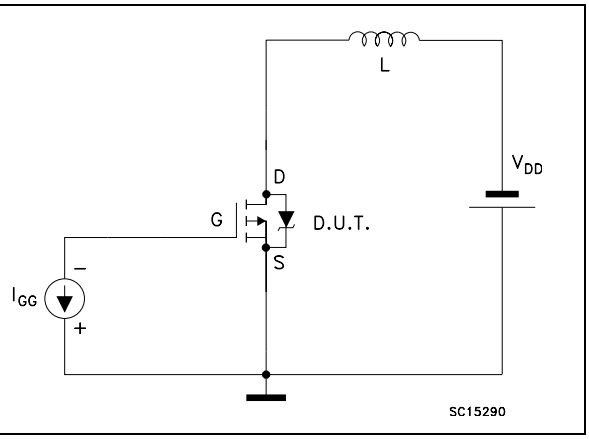
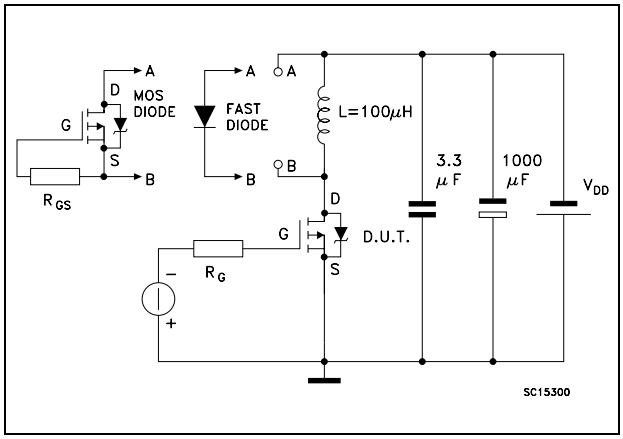


Figure 14. Test circuit for diode recovery behaviour

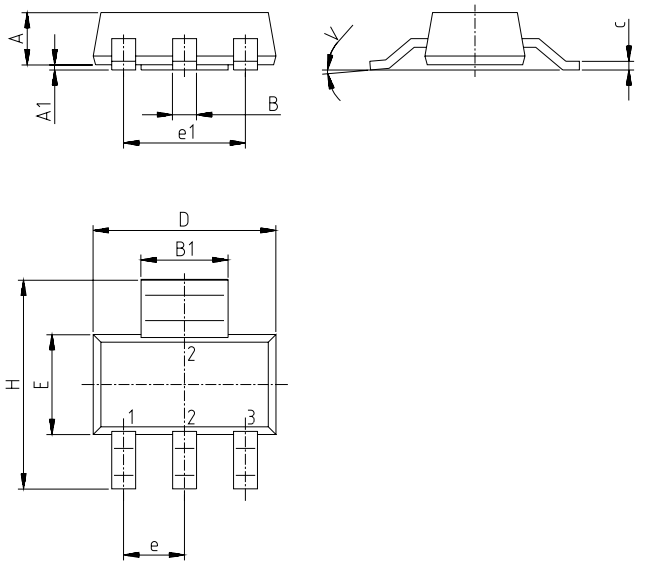


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: *www.st.com*

SOT-223 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.80			0.071
B	0.60	0.70	0.80	0.024	0.027	0.031
B1	2.90	3.00	3.10	0.114	0.118	0.122
c	0.24	0.26	0.32	0.009	0.010	0.013
D	6.30	6.50	6.70	0.248	0.256	0.264
e		2.30			0.090	
e1		4.60			0.181	
E	3.30	3.50	3.70	0.130	0.138	0.146
H	6.70	7.00	7.30	0.264	0.276	0.287
V			10^{o}			10^{o}
A1		0.02				



P008B

5 Revision history

Table 7. Revision history

Date	Revision	Changes
20-Jun-2005	1	First release
13-Dec-2005	2	Final version
04-Aug-2006	3	New template

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