STN8205A

Lead-free

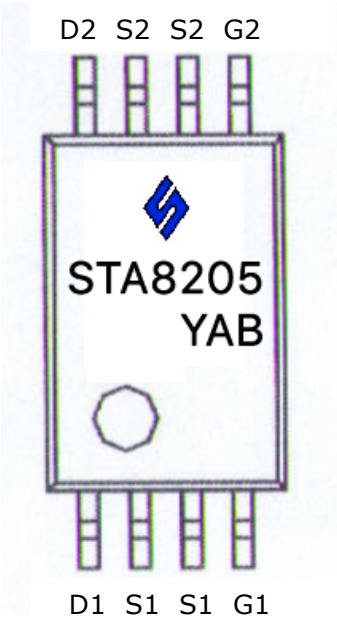
Dual N Channel Enhancement Mode MOSFET

5.0A

DESCRIPTION

STN8205A is the dual N-Channel enhancement mode power field effect transistor which is produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application, such as notebook computer power management and other battery powered circuits, where high-side switching is required.

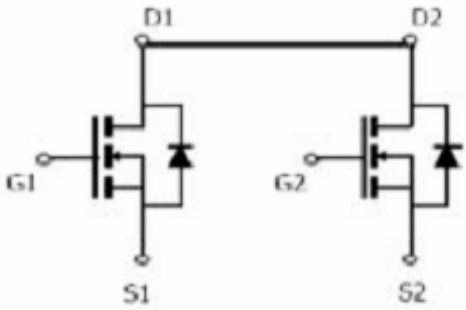
PIN CONFIGURATION
TSSOP-8



Y: Year Code
A: Date Code
B: Process Code

FEATURE

- 20V/5.0A, $R_{DS(ON)}$ = 21m-ohm (Typ.) @V_{GS} =4.5V
- 20V/3.0A, $R_{DS(ON)}$ =27m-ohm @V_{GS} =2.5V
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional low on-resistance and maximum DC current capability
- TSSOP-8 package design



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ABSOULTE MAXIMUM RATINGS (Ta = 25℃ unless otherwise noted)

Parameter		Symbol	Typical	Unit
Drain-Source Voltage		V_{DSS}	20	V
Gate-Source Voltage		V_{GSS}	+/-20	V
Continuous Drain Current (T_J=150℃)	T_A=25℃	I_D	5.0	A
	T_A=70℃		3.4	
Pulsed Drain Current		I_{DM}	30	A
Continuous Source Current (Diode Conduction)		I_S	2	A
Power Dissipation	T_A=25℃	P_D	2.0	W
	T_A=70℃		1.2	
Operation Junction Temperature		T_J	-40/140	℃
Storage Temperature Range		T_{STG}	-55/150	℃
Thermal Resistance-Junction to Ambient		$R_{\theta JA}$	105	℃/W

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ELECTRICAL CHARACTERISTICS (Ta = 25℃ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V,I_D=250uA	20			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=VGS,I_D=250uA	0.6		1.2	V
Gate Leakage Current	I_{GSS}	V_{DS}=0V,V_{GS}=+/-20V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=20V,V_{GS}=0V			1	uA
		V_{DS}=20V,V_{GS}=0V T_J=85℃			5	
Drain-source On-Resistance	$R_{DS(on)}$	V_{GS}=4.5V,I_D=5.0A		0.021	0.27	Ω
		V_{GS}=2.5V,I_D=3.0A		0.024	0.030	
Forward Transconductance	g_{fs}	V_{DS}=5V,I_D=3.6A		10		S
Diode Forward Voltage	V_{SD}	I_S=1.0A,V_{GS}=0V		0.8	1.0	V
Dynamic						
Total Gate Charge	Q_g	V_{DS}=10V,V_{GS}=4.5V,V_{DS}=4A		10.5		nC
Gate-Source Charge	Q_{gs}			2.5		
Gate-Drain Charge	Q_{gd}			2.1		
Input Capacitance	C_{iss}	V_{DS}=8V,V_{GS}=0V f=1MHz		805		pF
Output Capacitance	C_{oss}			155		
Reverse Transfer Capacitance	C_{rss}			122		
Turn-On Time	$T_{d(on)}$	V_{DD}=10V, RL=10Ω, I_D=1.0A, V_{GEN}=4.5V, RG=10Ω		14		nS
	t_r			6		
Turn-Off Time	$T_{d(off)}$			45		
	t_f			20		

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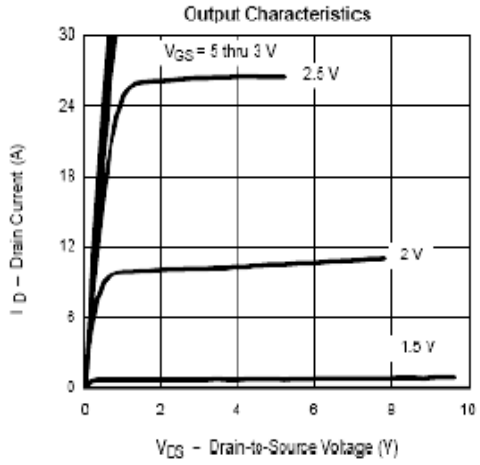
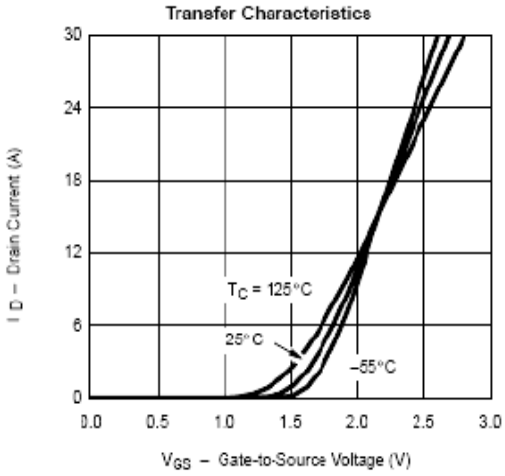
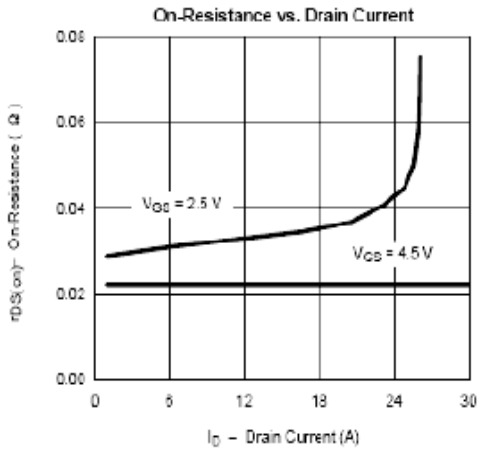
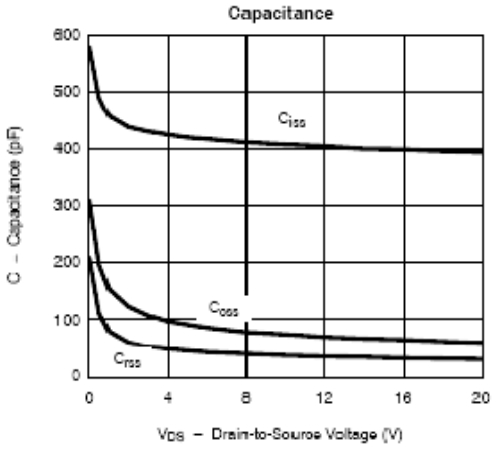
TYPICAL CHARACTERICTICS









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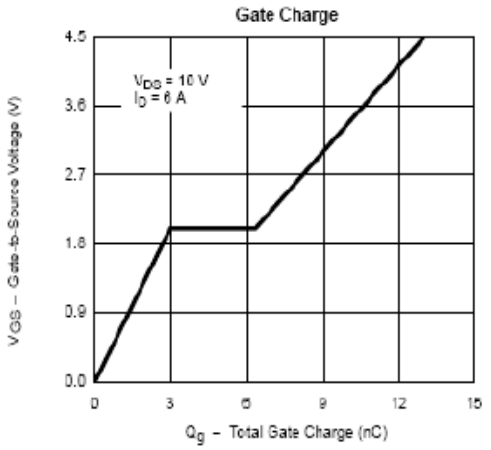

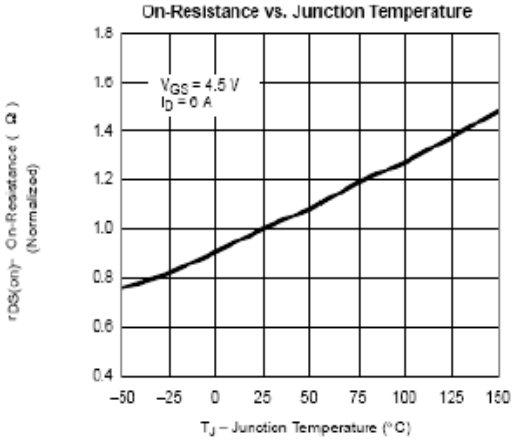

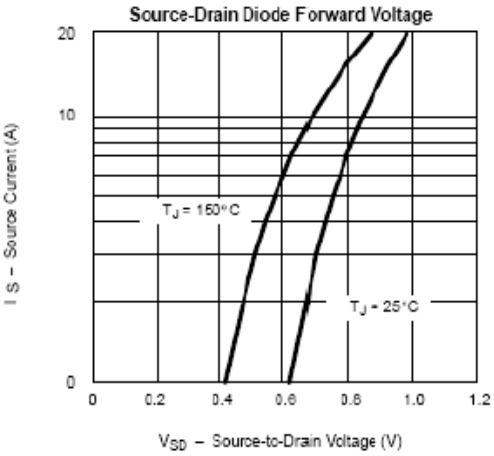

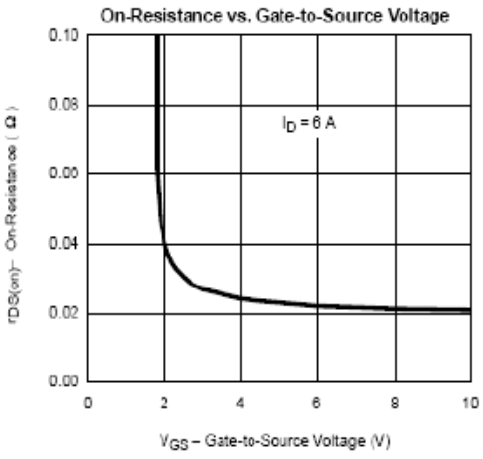

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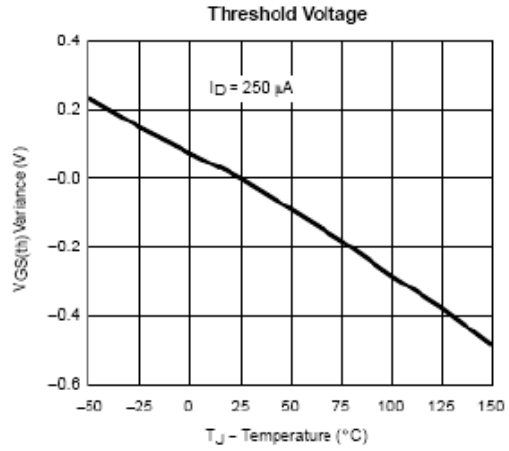

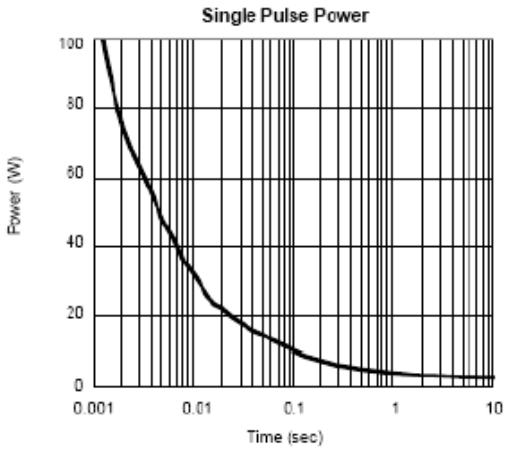

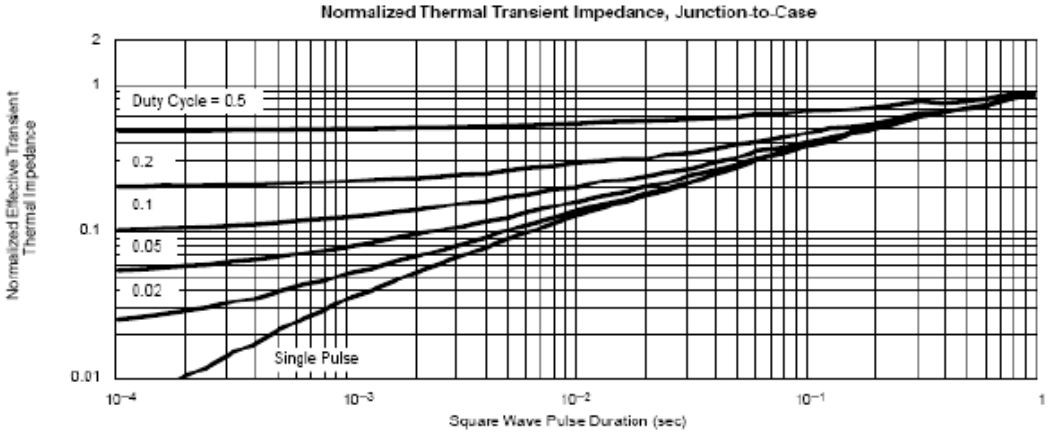

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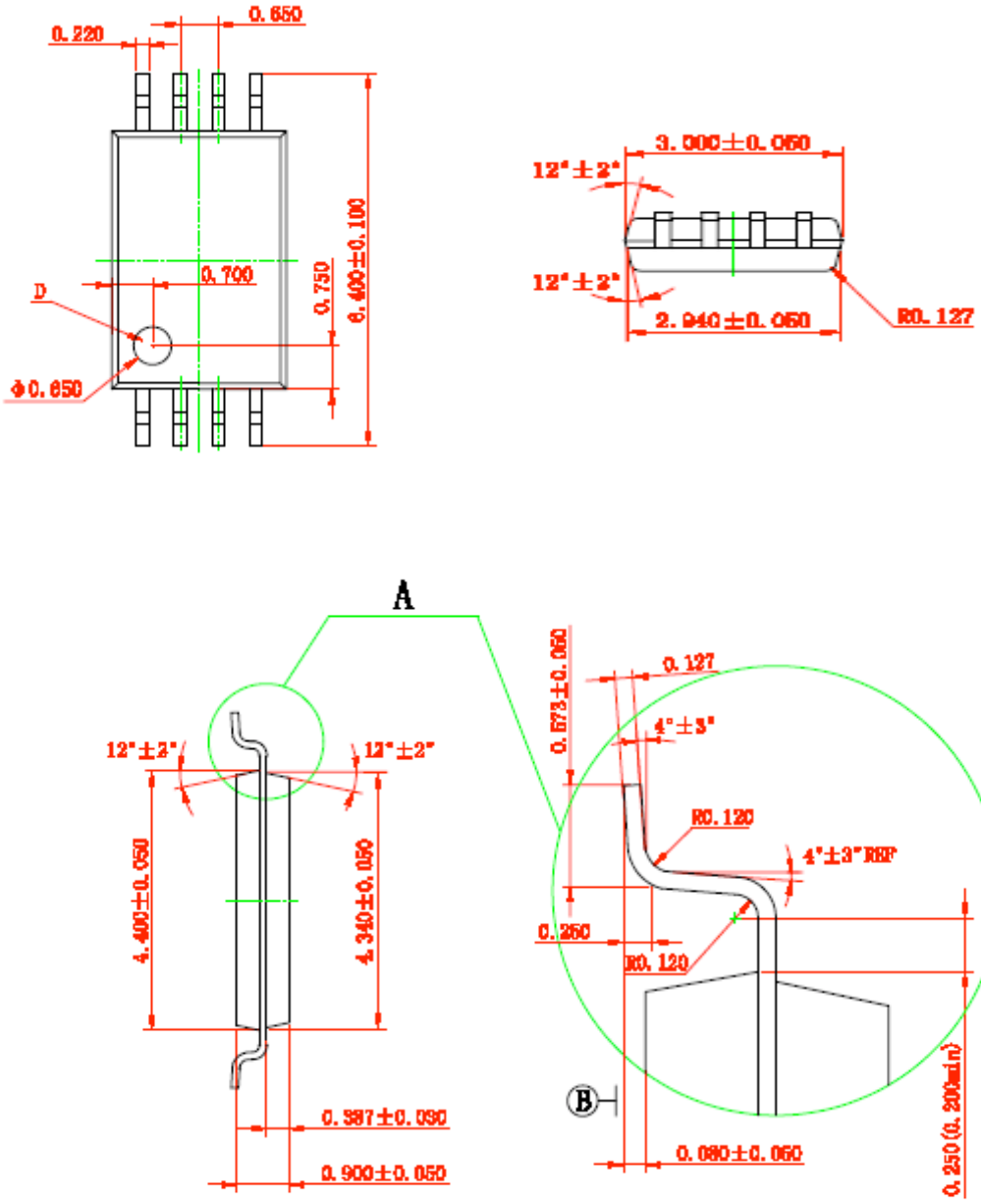
TSSOP-8 PACKAGE OUTLINE



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