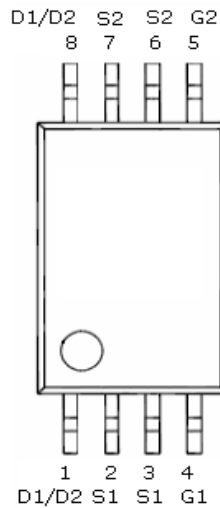
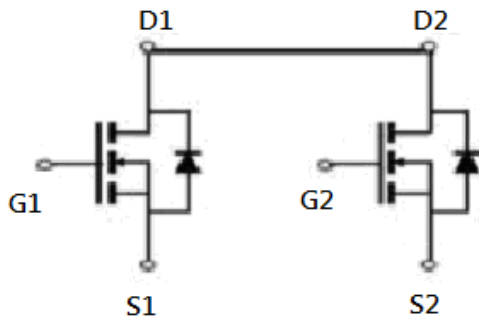


**DESCRIPTION**

STN8822 is the dual N-Channel enhancement mode power field effect transistor which is produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application, such as notebook computer power management and other battery powered circuits, where high-side switching is required.

**PIN CONFIGURATION**  
**TSSOP-8**

**FEATURE**

- 20V/8.0A,  $R_{DS(ON)} = 20\text{m-ohm}$  (Typ.) @ $V_{GS} = 4.5\text{V}$
- 20V/7.0A,  $R_{DS(ON)} = 24\text{m-ohm}$  @ $V_{GS} = 2.5\text{V}$
- 20V/3.0A,  $R_{DS(ON)} = 32\text{m-ohm}$  @ $V_{GS} = 1.8\text{V}$
- Super high density cell design for extremely low  $R_{DS(ON)}$
- Exceptional low on-resistance and maximum DC current capability
- TSSOP-8 package design





**STN8822** 

Dual N Channel Enhancement Mode MOSFET

**8.0A**

**ABSOLUTE MAXIMUM RATINGS** (Ta = 25°C unless otherwise noted )

Parameter		Symbol	Typical	Unit
Drain-Source Voltage		V <sub>DSS</sub>	20	V
Gate-Source Voltage		V <sub>GSS</sub>	+/-12	V
Continuous Drain Current (T <sub>J</sub> =150°C)	T <sub>A</sub> =25°C	I <sub>D</sub>	7.4	A
	T <sub>A</sub> =70°C		6.0	
Pulsed Drain Current		I <sub>DM</sub>	30	A
Continuous Source Current (Diode Conduction)		I <sub>S</sub>	1.5	A
Power Dissipation	T <sub>A</sub> =25°C	P <sub>D</sub>	2.0	W
	T <sub>A</sub> =70°C		1.2	
Operation Junction Temperature		T <sub>J</sub>	-40/140	°C
Storage Temperature Range		T <sub>STG</sub>	-55/150	°C
Thermal Resistance-Junction to Ambient		R <sub>θJA</sub>	105	°C/W



**STN8822** 

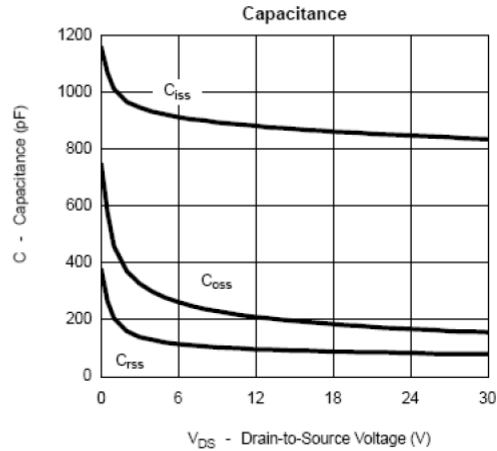
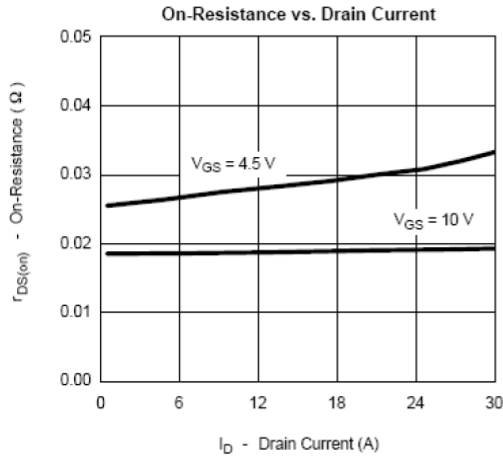
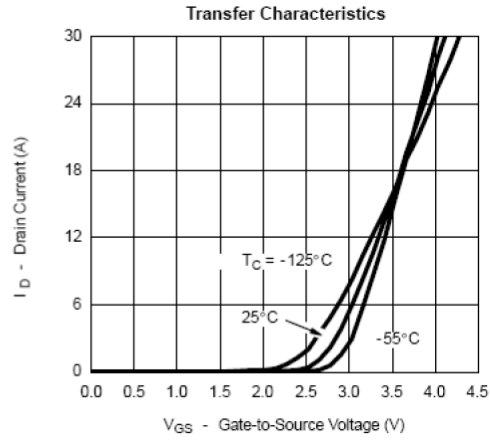
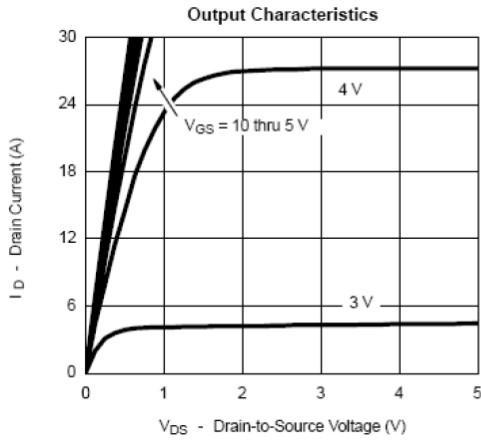
Dual N Channel Enhancement Mode MOSFET

**8.0A**

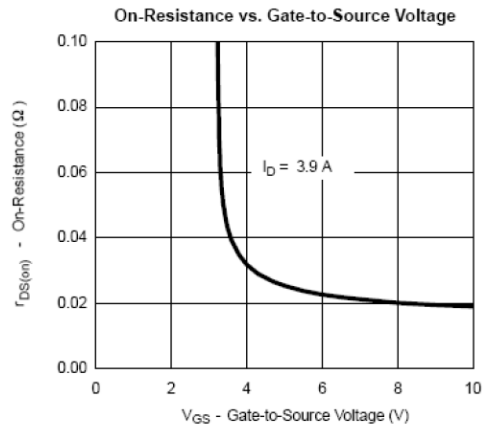
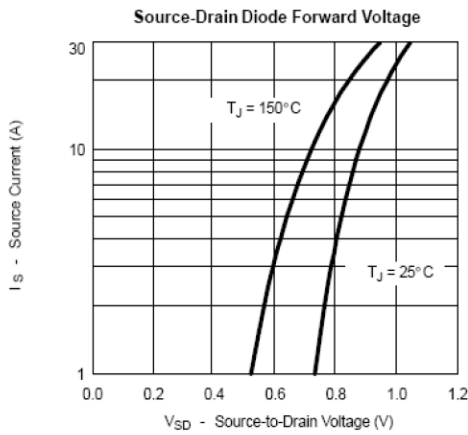
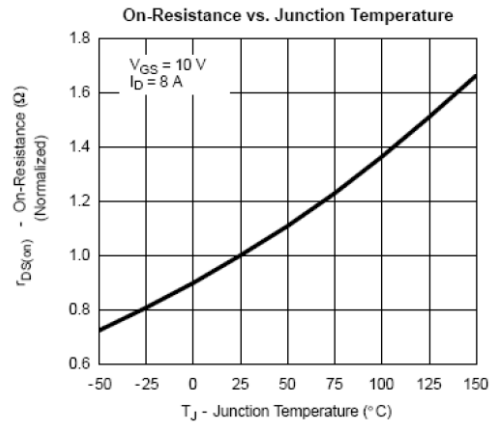
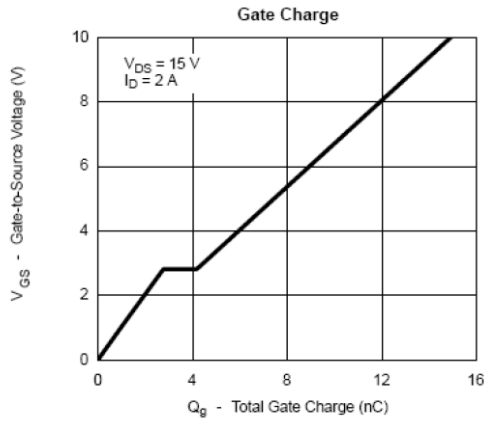
**ELECTRICAL CHARACTERISTICS** ( Ta = 25°C unless otherwise noted )

Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\mu A$	20			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	0.4		1.0	V
Gate Leakage Current	$I_{GSS}$	$V_{DS}=0V, V_{GS}=+/-20V$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=20V, V_{GS}=0V$			1	uA
		$V_{DS}=20V, V_{GS}=0V$ $T_J=85^\circ C$			5	
On-State Drain Current	$I_{D(on)}$	$V_{DS} \leq 5V, V_{GS}=4.5V$	6			A
Drain-source On-Resistance	$R_{DS(on)}$	$V_{GS}=4.5V, I_D=8.0A$		0.020	0.024	$\Omega$
		$V_{GS}=2.5V, I_D=7.0A$		0.024	0.032	
		$V_{GS}=1.8V, I_D=3.0A$		0.032	0.042	
Forward Transconductance	$g_{fs}$	$V_{DS}=5V, I_D=3.6A$		30		S
Diode Forward Voltage	$V_{SD}$	$I_S=1.7A, V_{GS}=0V$		0.8	1.2	V
<b>Dynamic</b>						
Total Gate Charge	$Q_g$	$V_{DS}=10V, V_{GS}=4.5V, I_D=6.0A$		2		nC
Gate-Source Charge	$Q_{gs}$			2.5		
Gate-Drain Charge	$Q_{gd}$			2.1		
Input Capacitance	$C_{iss}$	$V_{DS}=8V, V_{GS}=0V$ $f=1MHz$		575		pF
Output Capacitance	$C_{oss}$			120		
Reverse Transfer Capacitance	$C_{rss}$			100		
Turn-On Time	$T_{d(on)}$	$V_{DD}=10V, R_L=10\Omega,$ $I_D=1.0A, V_{GEN}=4.5V,$ $R_G=10\Omega$		14		nS
	$t_r$			40		
Turn-Off Time	$T_{d(off)}$			45		
	$t_f$			30		

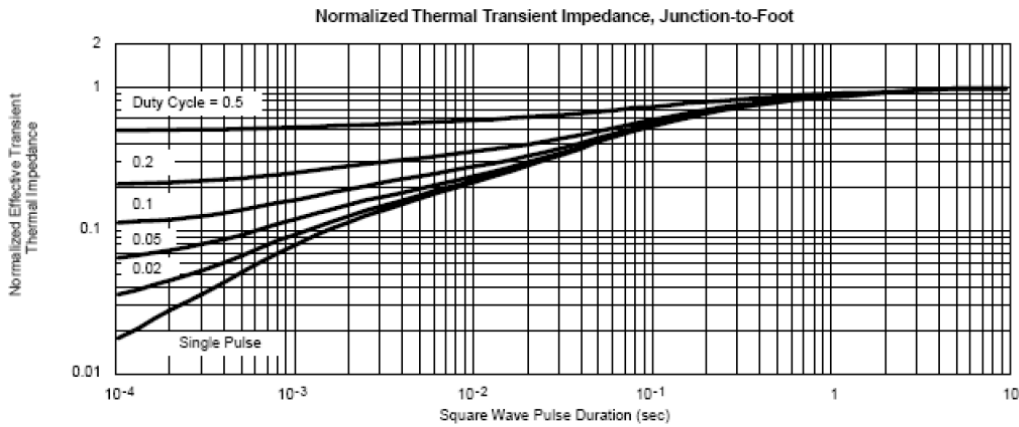
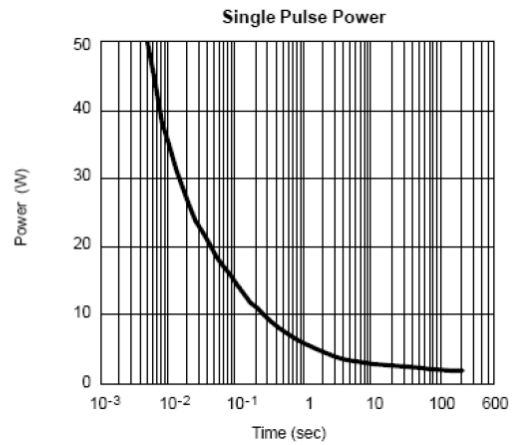
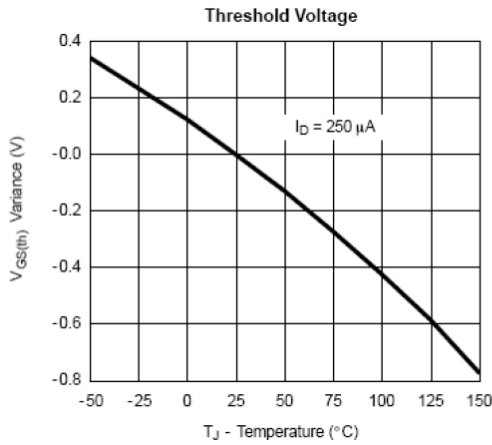
**TYPICAL CHARACTERISTICS**

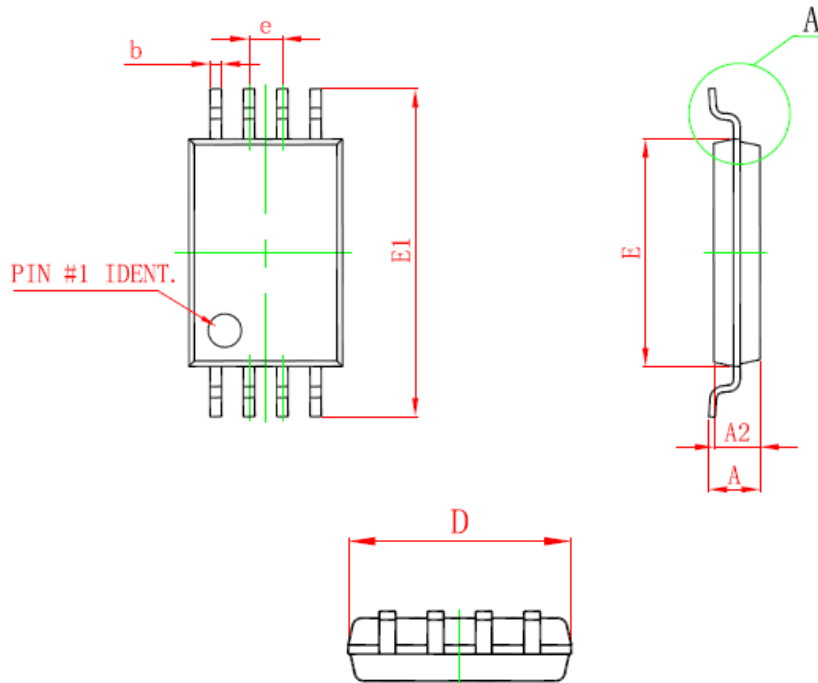


**TYPICAL CHARACTERISTICS**



**TYPICAL CHARACTERISTICS**



**TSSOP-8 PACKAGE OUTLINE**


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
D	2.900	3.100	0.114	0.122
E	4.300	4.500	0.169	0.177
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
E1	6.250	6.550	0.246	0.258
A		1.100		0.043
A2	0.800	1.000	0.031	0.039
A1	0.020	0.150	0.001	0.006
e	0.65 (BSC)		0.026 (BSC)	
L	0.500	0.700	0.020	0.028
H	0.25 (TYP)		0.01 (TYP)	
$\theta$	1°	7°	1°	7°