STD10NM60ND, STF10NM60ND, STP10NM60ND

N-channel 600 V, 0.57 Ω typ., 8 A, FDmesh™ II Power MOSFETs in DPAK, TO-220FP and TO-220 packages

Datasheet - production data

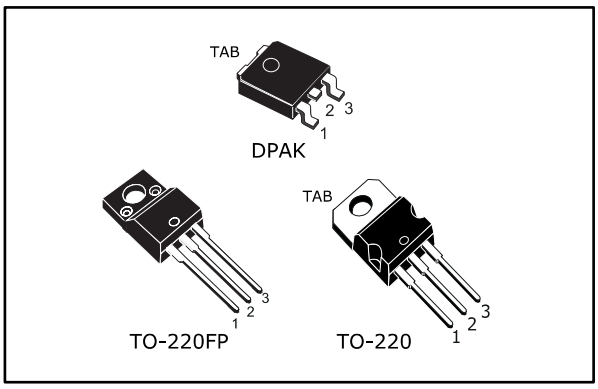
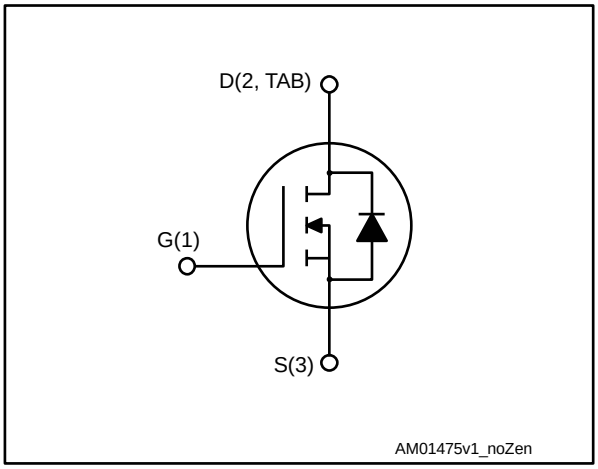


Figure 1: Internal schematic diagram



Features

Order code	V_{DS} @ $T_{jmax.}$	$R_{DS(on)}$ max.	I_D	P_{TOT}
STD10NM60ND	650 V	0.60 Ω	8 A	70 W
STF10NM60ND				25 W
STP10NM60ND				70 W

- Fast-recovery body diode
- Low gate charge and input capacitance
- Low on-resistance $R_{DS(on)}$
- 100% avalanche tested
- High dv/dt ruggedness

Applications

- Switching applications

Description

These FDmesh™ II Power MOSFETs with fast-recovery body diode are produced using MDmesh™ II technology. Utilizing a new strip-layout vertical structure, these devices feature low on-resistance and superior switching performance. They are ideal for bridge topologies and ZVS phase-shift converters.

Table 1: Device summary

Order code	Marking	Package	Packing
STD10NM60ND	10NM60ND	DPAK	Tape and reel
STF10NM60ND		TO-220FP	Tube
STP10NM60ND		TO-220	

Contents

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value			Unit
		DPAK	TO-220FP	TO-220	
V_{DS}	Drain-source voltage	600			V
V_{GS}	Gate-source voltage	±25			V
I_D	Drain current (continuous) at T_C = 25 °C	8	8 (1)	8	A
I_D	Drain current (continuous) at T_C = 100 °C	5	5 (1)	5	A
I_{DM} (2)	Drain current (pulsed)	32			A
P_{TOT}	Total dissipation at T_C = 25 °C	70	25	70	W
dv/dt (3)	Peak diode recovery voltage slope	40			V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat-sink (t = 1 s; T_C = 25 °C)			2500	V
T_{stg}	Storage temperature range	- 55 to 150			°C
T_j	Operating junction temperature range				

Notes:

(1)Limited by maximum junction temperature.

(2)Pulse width limited by safe operating area.

(3)I_{SD} ≤ 8 A, di/dt ≤ 400 A/µs; $V_{DS(peak)}$ < $V_{(BR)DSS}$, V_{DD} = 80% $V_{(BR)DSS}$.

Table 3: Thermal data

Symbol	Parameter	Value			Unit
		DPAK	TO-220FP	TO-220	
$R_{thj\text{-}case}$	Thermal resistance junction-case	1.79	5	1.79	°C/W
$R_{thj\text{-}pcb}$	Thermal resistance junction-pcb(1)	50			°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient		62.5		°C/W

Notes:

(1)When mounted on 1 inch² FR-4, 2 Oz copper board.

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AS}(1)	Single pulse avalanche current	2.5	A
E_{AS}(2)	Single pulse avalanche energy	130	mJ

Notes:

(1) Pulse width limited by T_{jmax}.

(2) starting T_j = 25 °C, I_D = I_{AS}, V_{DD} = 50 V.

2 Electrical characteristics

(T_{case} = 25 °C unless otherwise specified)

Table 5: Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	600			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 600 V			1	µA
		V_{GS} = 0 V, V_{DS} = 600 V, T_C = 125 °C (1)			100	
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±25 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 4 A		0.57	0.60	Ω

Notes:

(1)Defined by design, not subject to production test.

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 50 V, f = 1 MHz, V_{GS} = 0 V	-	577	-	pF
C_{oss}	Output capacitance		-	32.4	-	
C_{rss}	Reverse transfer capacitance		-	1.76	-	
$C_{oss\ eq.}$ (1)	Equivalent output capacitance	V_{DS} = 0 to 480 V, V_{GS} = 0 V	-	138	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz, I_D=0 A	-	6	-	Ω
Q_g	Total gate charge	V_{DD} = 480 V, I_D = 8 A, V_{GS} = 0 to 10 V (see *Figure 19: "Test circuit for gate charge behavior"*)	-	20	-	nC
Q_{gs}	Gate-source charge		-	4.3	-	
Q_{gd}	Gate-drain charge		-	11.6	-	

Notes:

(1)$C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 300 V, I_D = 4 A, R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 18: "Test circuit for resistive load switching times"* and *Figure 23: "Switching time waveform"*)	-	9.2	-	ns
t_r	Rise time		-	10	-	
$t_{d(off)}$	Turn-off delay time		-	32	-	
t_f	Fall time		-	9.8	-	

Table 8: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		8	A
I_{SDM}(1)	Source-drain current (pulsed)		-		32	A
V_{SD}(2)	Forward on voltage	V_{GS} = 0 V, I_{SD} = 8 A	-		1.5	V
t_{rr}	Reverse recovery time	I_{SD} = 8 A, di/dt = 100 A/µs, V_{DD} = 60 V (see *Figure 20: "Test circuit for inductive load switching and diode recovery times"*)	-	118		ns
Q_{rr}	Reverse recovery charge		-	680		nC
I_{RRM}	Reverse recovery current		-	11		A
t_{rr}	Reverse recovery time	I_{SD} = 8 A, di/dt = 100 A/µs, V_{DD} = 60 V, T_j = 150 °C (see *Figure 20: "Test circuit for inductive load switching and diode recovery times"*)	-	150		ns
Q_{rr}	Reverse recovery charge		-	918		nC
I_{RRM}	Reverse recovery current		-	12		A

Notes:

(1) Pulse width is limited by safe operating area.

(2) Pulse test: pulse duration = 300 µs, duty cycle 1.5%.

2.1 Electrical characteristics (curves)

Figure 2: Safe operating area for DPAK

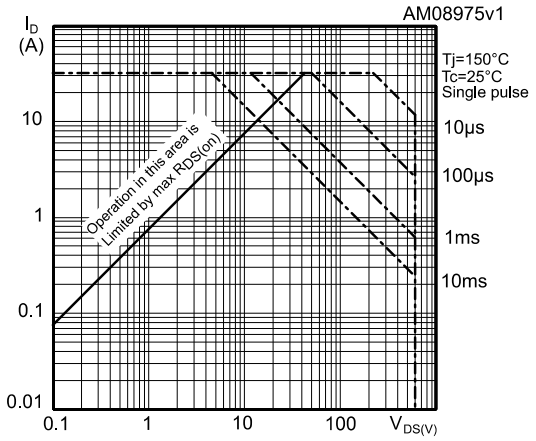


Figure 3: Thermal impedance for DPAK

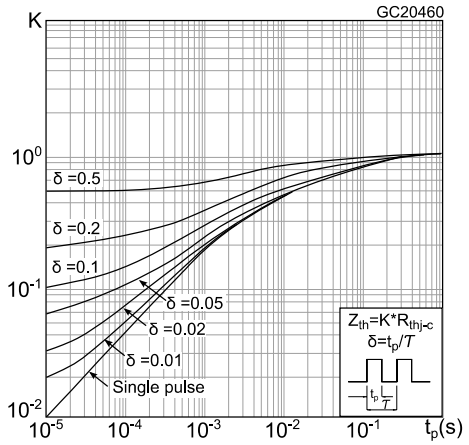


Figure 4: Safe operating area for TO-220FP

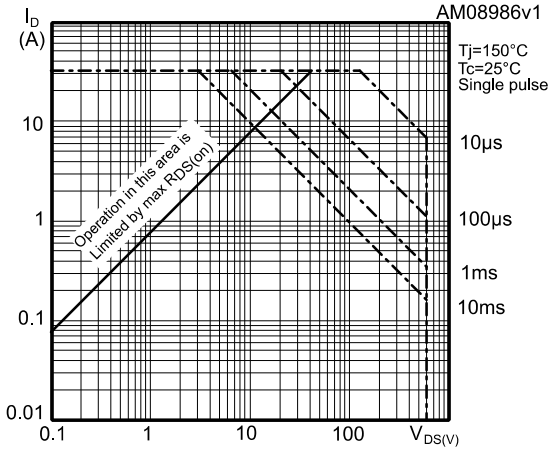


Figure 5: Thermal impedance for TO-220FP

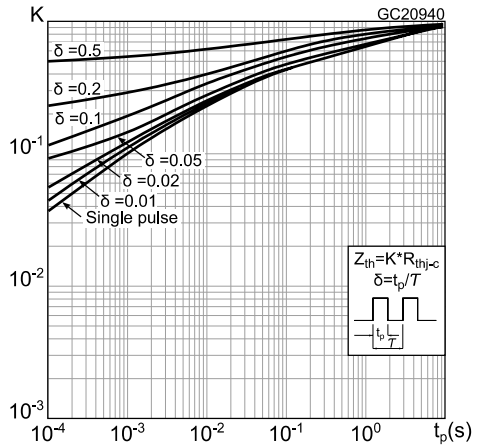


Figure 6: Safe operating area for TO-220

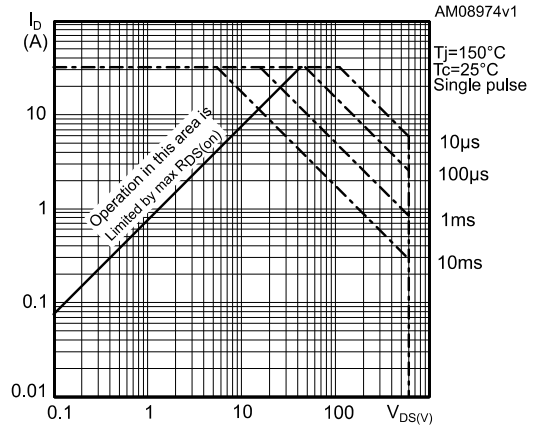


Figure 7: Thermal impedance for TO-220

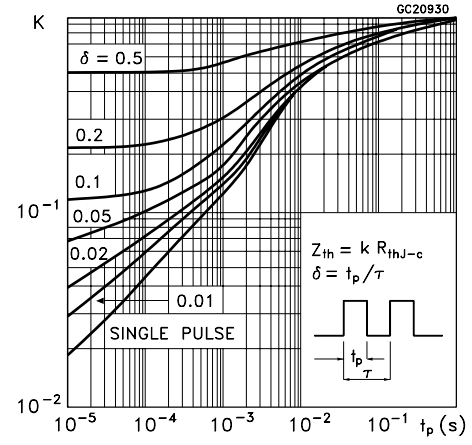


Figure 8: Output characteristics

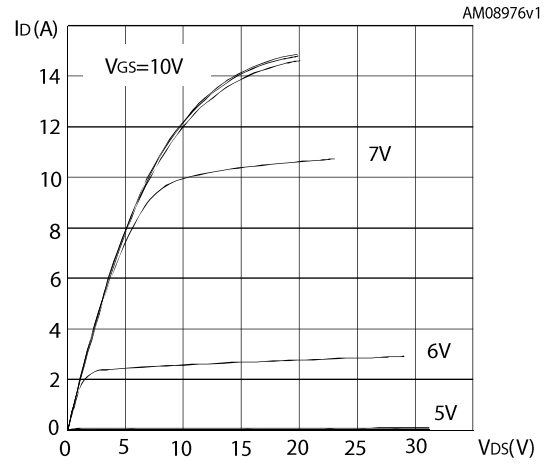


Figure 9: Transfer characteristics

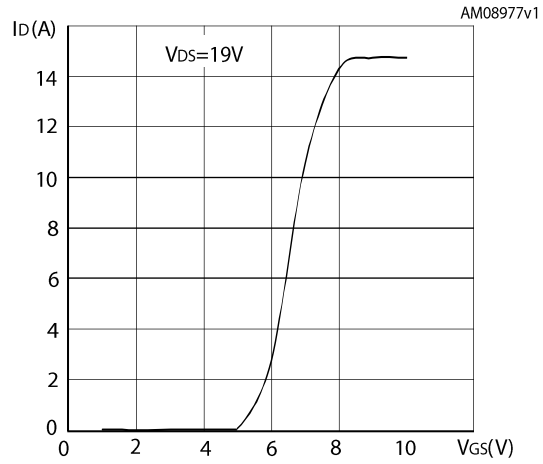


Figure 10: Gate charge vs gate-source voltage

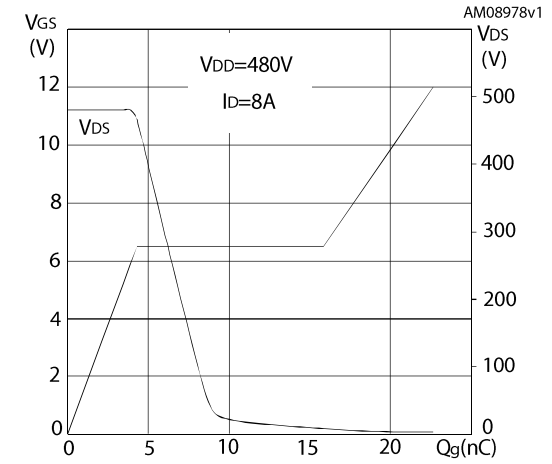


Figure 11: Static drain-source on-resistance

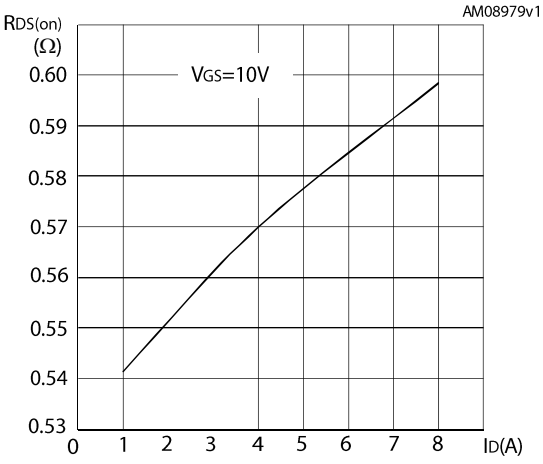


Figure 12: Capacitance variations

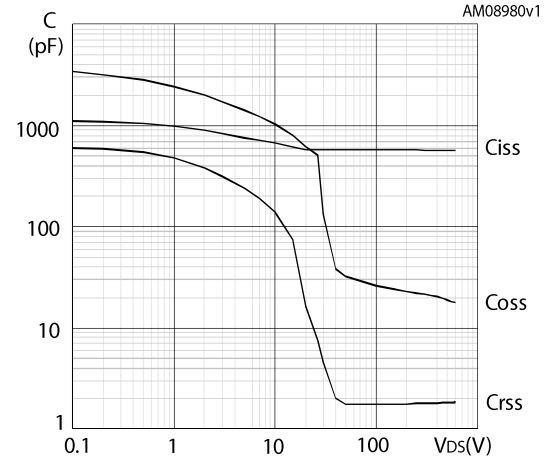


Figure 13: Output capacitance stored energy

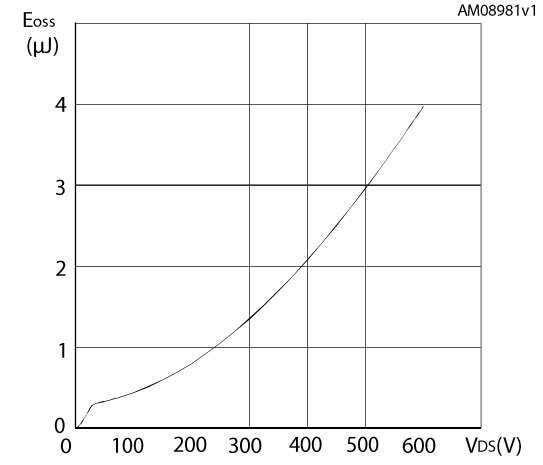


Figure 14: Normalized gate threshold voltage vs temperature

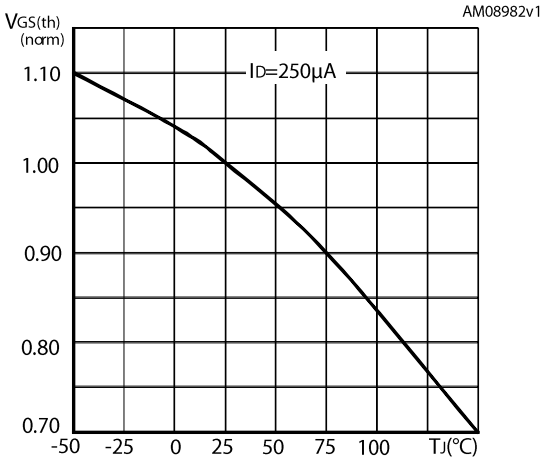


Figure 15: Normalized on-resistance vs temperature

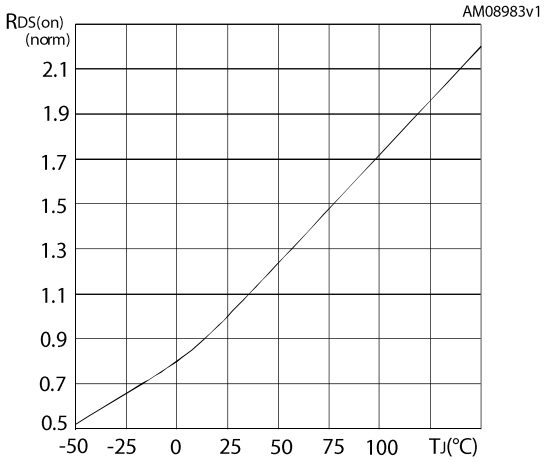


Figure 16: Normalized $V_{(BR)DSS}$ vs temperature

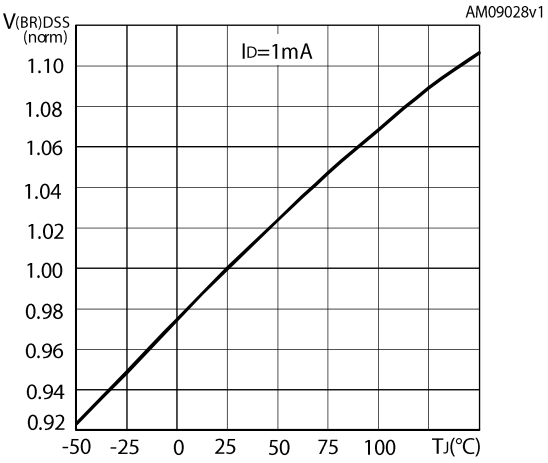
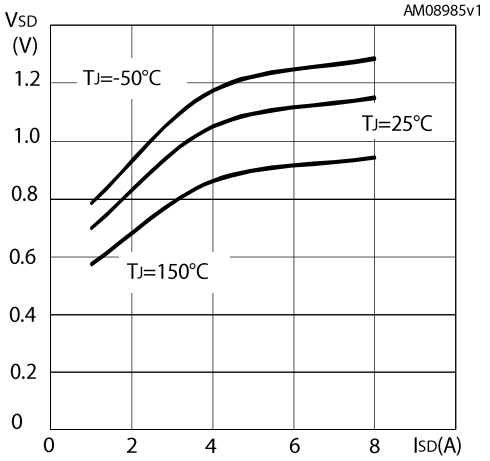


Figure 17: Source-drain diode forward characteristics



3 Test circuits

Figure 18: Test circuit for resistive load switching times

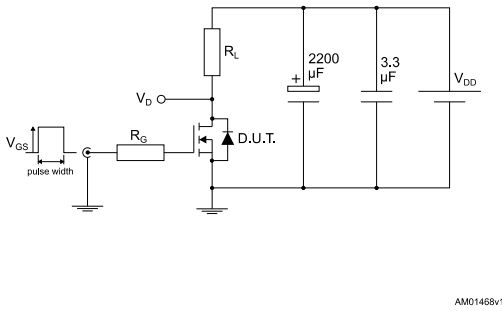


Figure 19: Test circuit for gate charge behavior

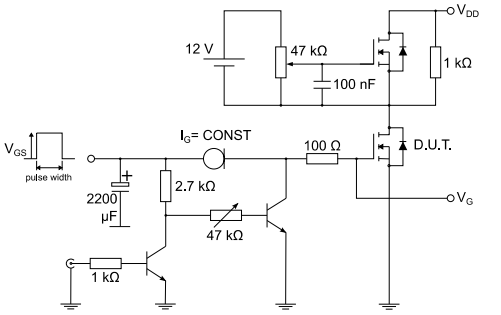


Figure 20: Test circuit for inductive load switching and diode recovery times

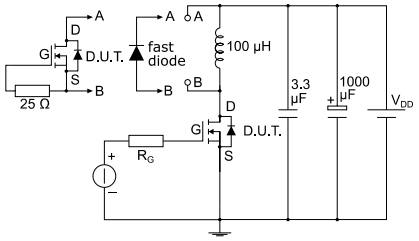


Figure 21: Unclamped inductive load test circuit

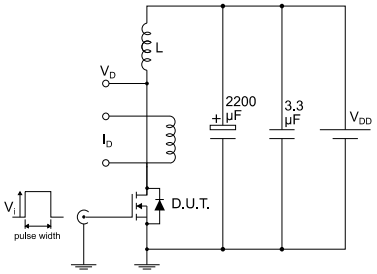


Figure 22: Unclamped inductive waveform

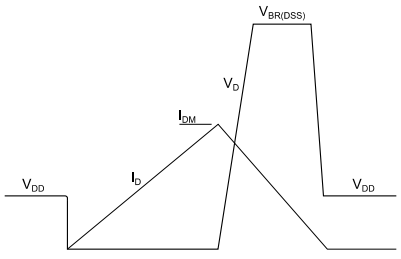
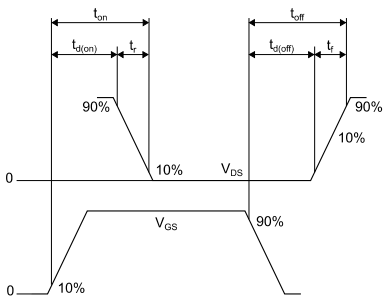


Figure 23: Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

4.1 DPAK (TO-252) type A package information

Figure 24: DPAK (TO-252) type A package outline

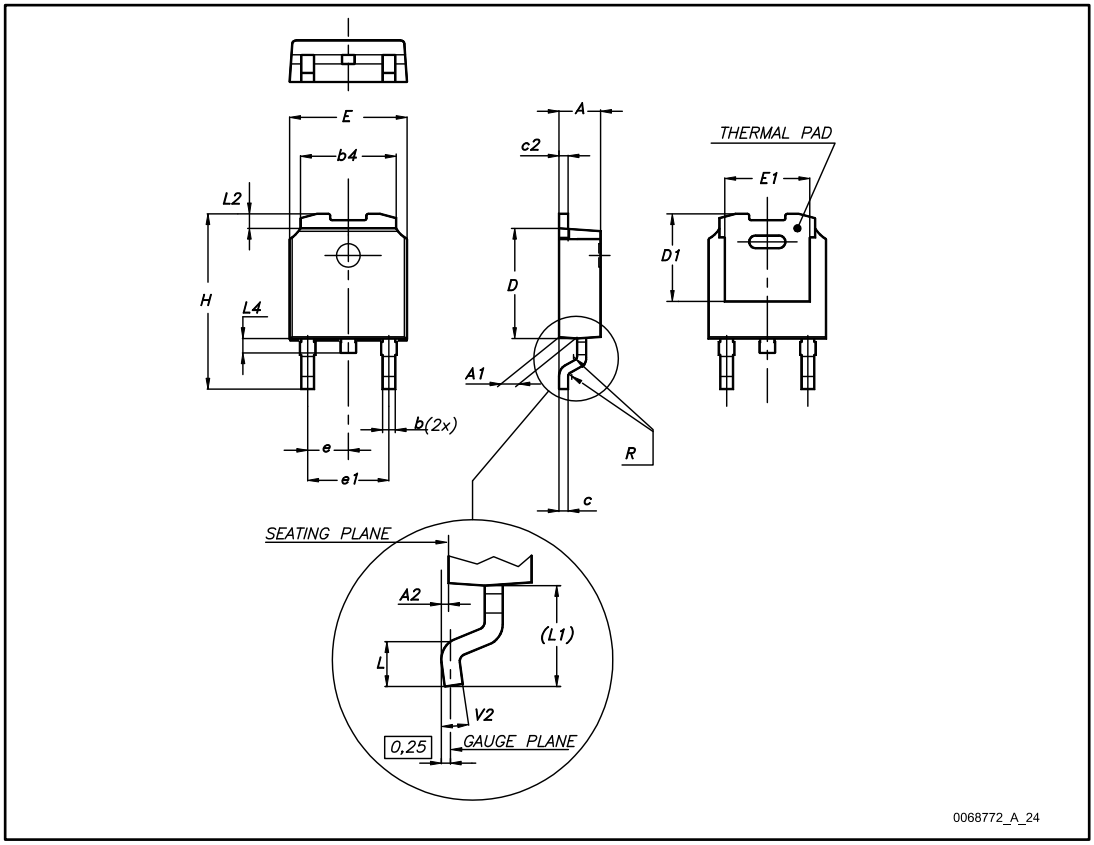


Table 9: DPAK (TO-252) type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1	4.95	5.10	5.25
E	6.40		6.60
E1	4.60	4.70	4.80
e	2.16	2.28	2.40
e1	4.40		4.60
H	9.35		10.10
L	1.00		1.50
(L1)	2.60	2.80	3.00
L2	0.65	0.80	0.95
L4	0.60		1.00
R		0.20	
V2	0°		8°

4.2 DPAK (TO-252) type E package information

Figure 25: DPAK (TO-252) type E package outline

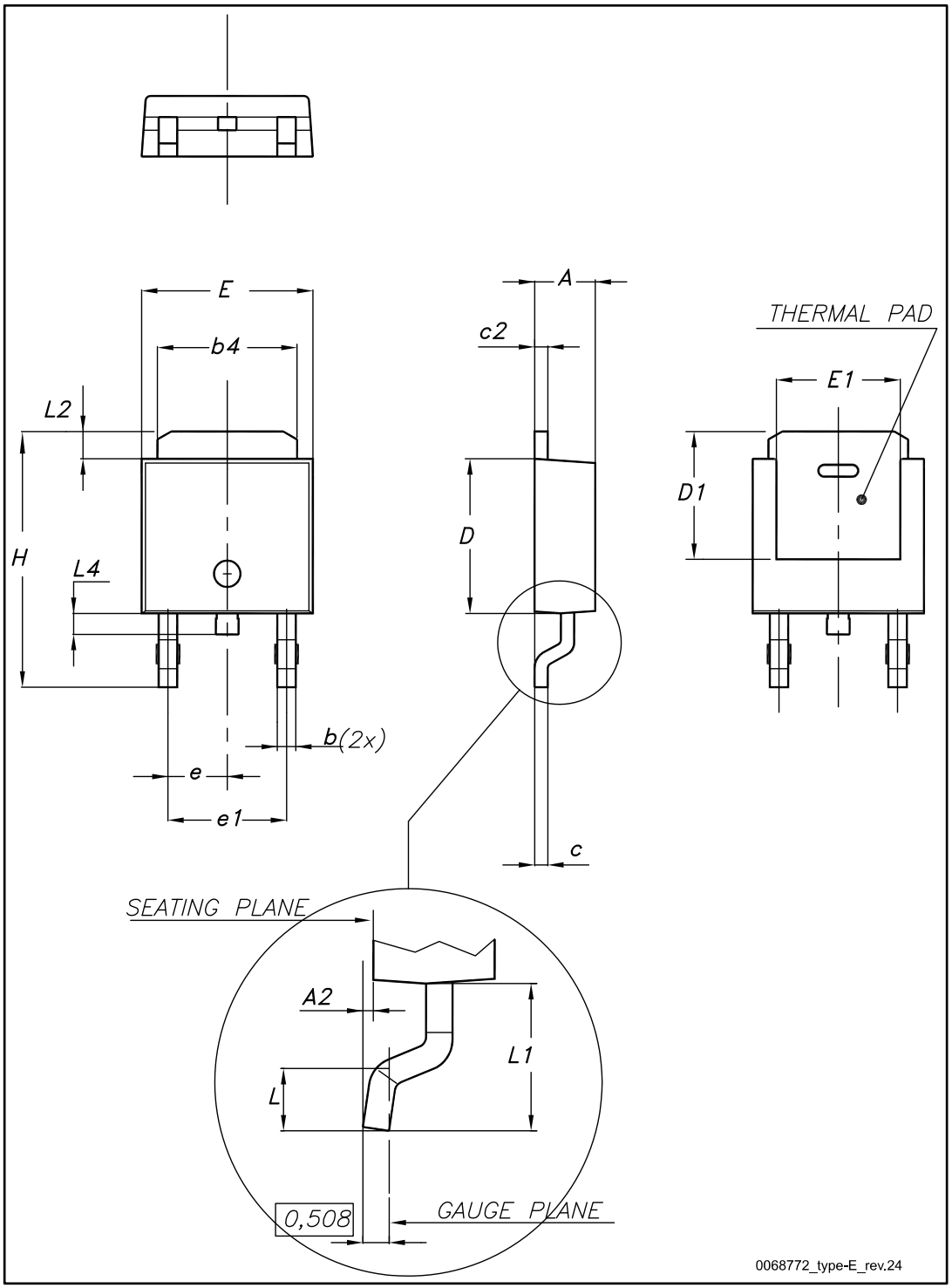
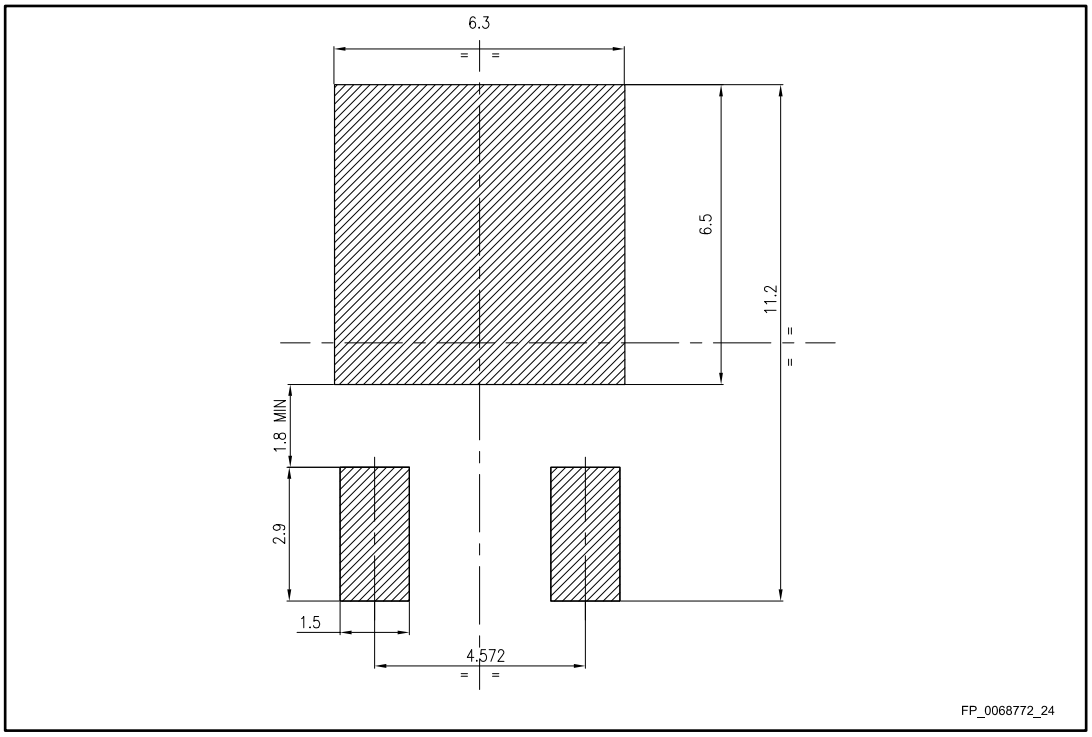


Table 10: DPAK (TO-252) type E mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.18		2.39
A2			0.13
b	0.65		0.884
b4	4.95		5.46
c	0.46		0.61
c2	0.46		0.60
D	5.97		6.22
D1	5.21		
E	6.35		6.73
E1	4.32		
e		2.286	
e1		4.572	
H	9.94		10.34
L	1.50		1.78
L1		2.74	
L2	0.89		1.27
L4			1.02

Figure 26: DPAK (TO-252) recommended footprint (dimensions are in mm)



4.3 TO-220FP package information

Figure 27: TO-220FP package outline

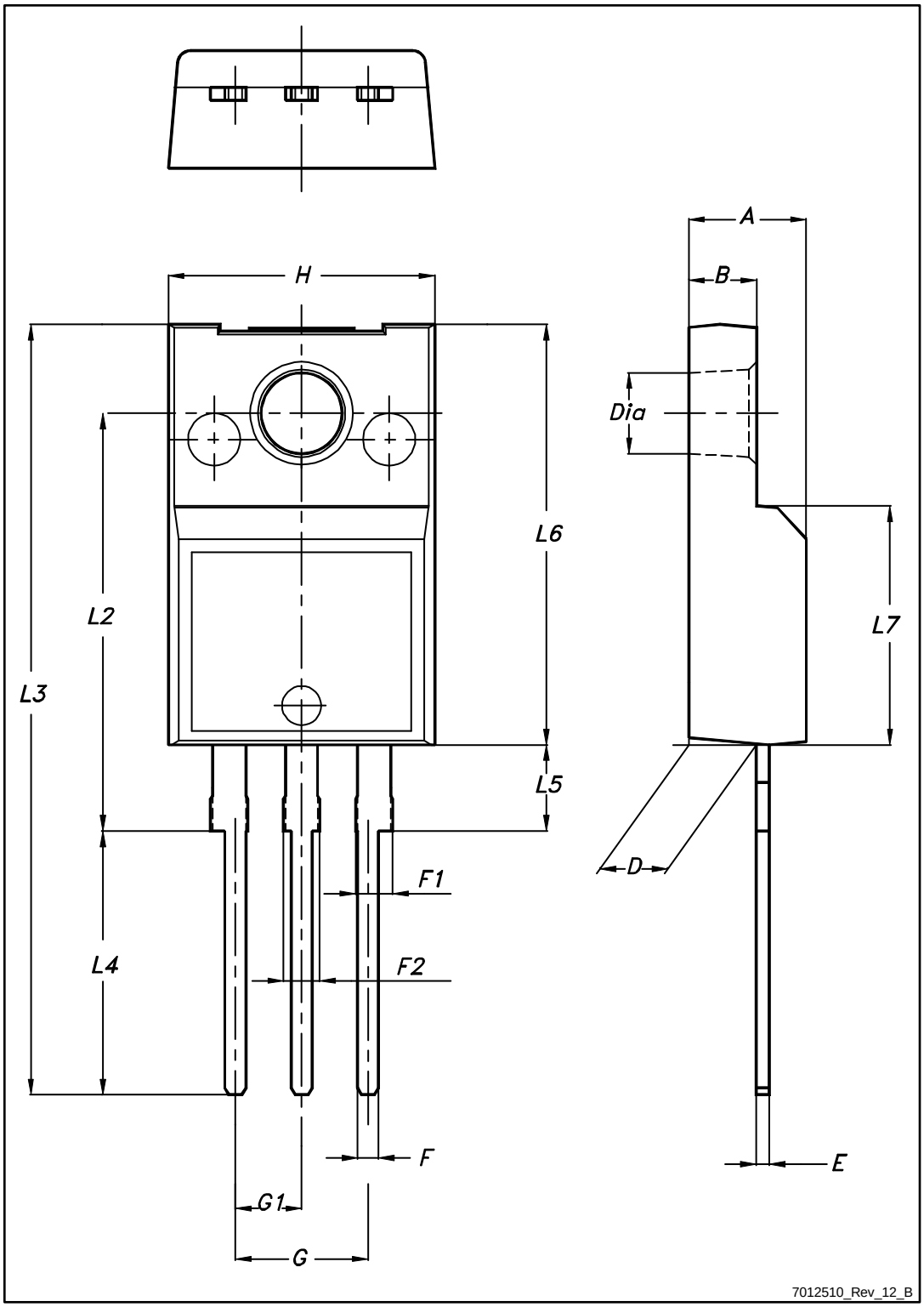


Table 11: TO-220FP package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

4.4 TO-220 package information

Figure 28: TO-220 type A package outline

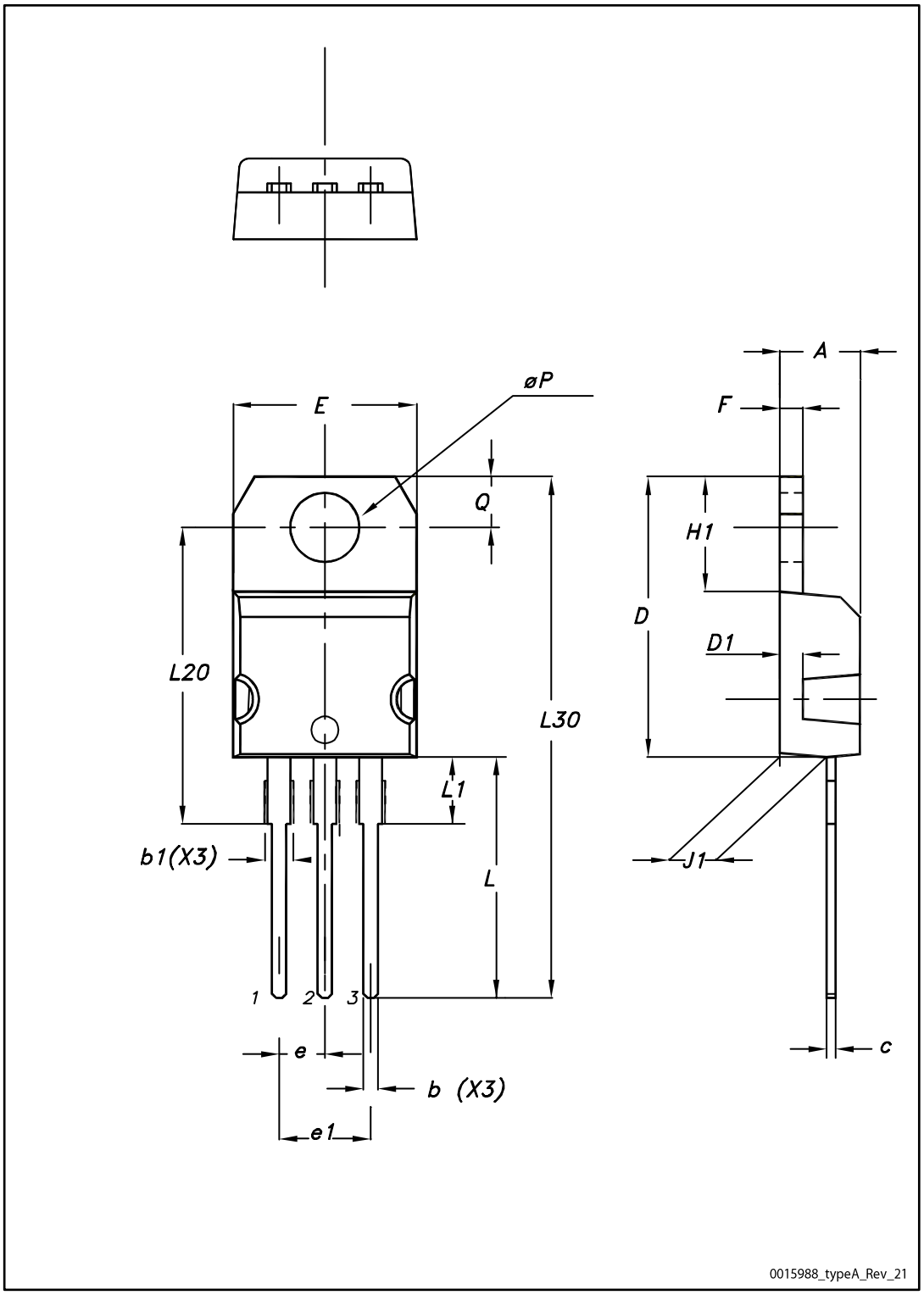


Table 12: TO-220 type A package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.55
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10.00		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13.00		14.00
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95

4.5 DPAK (TO-252) packing information

Figure 29: DPAK (TO-252) tape outline

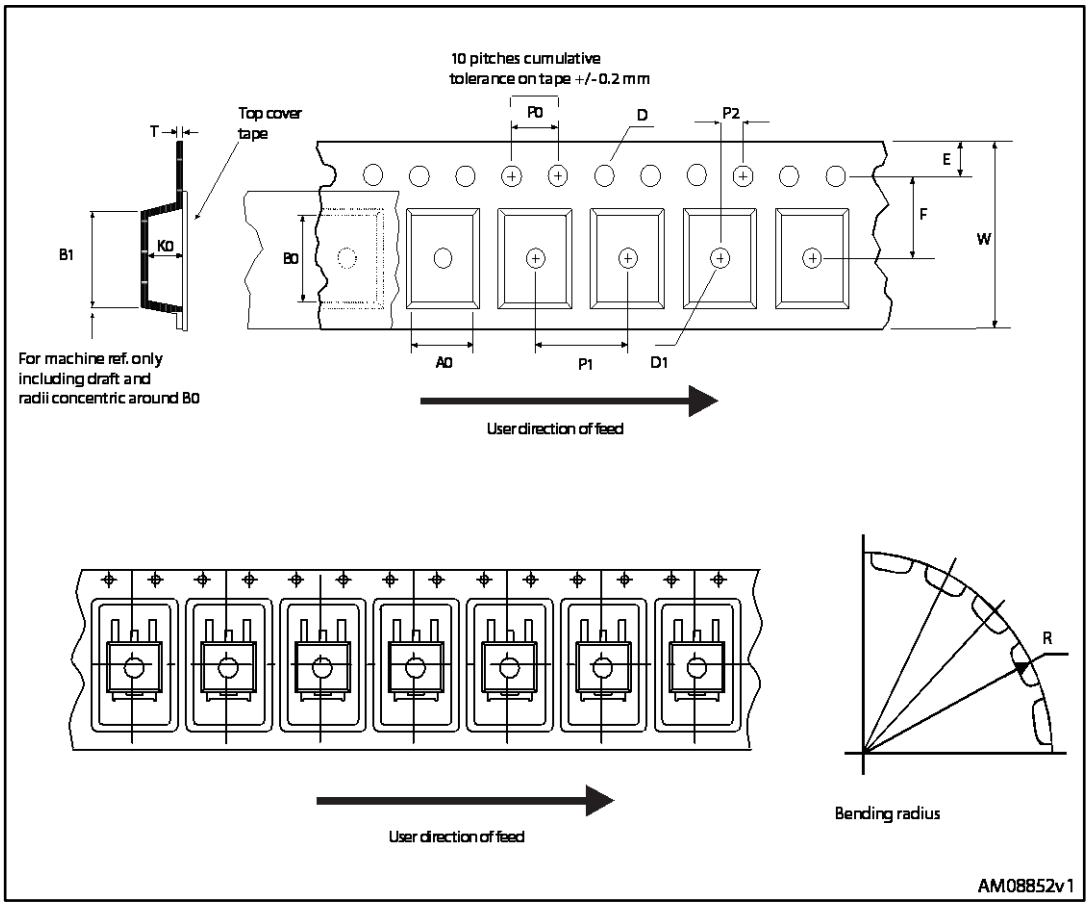


Figure 30: DPAK (TO-252) reel outline

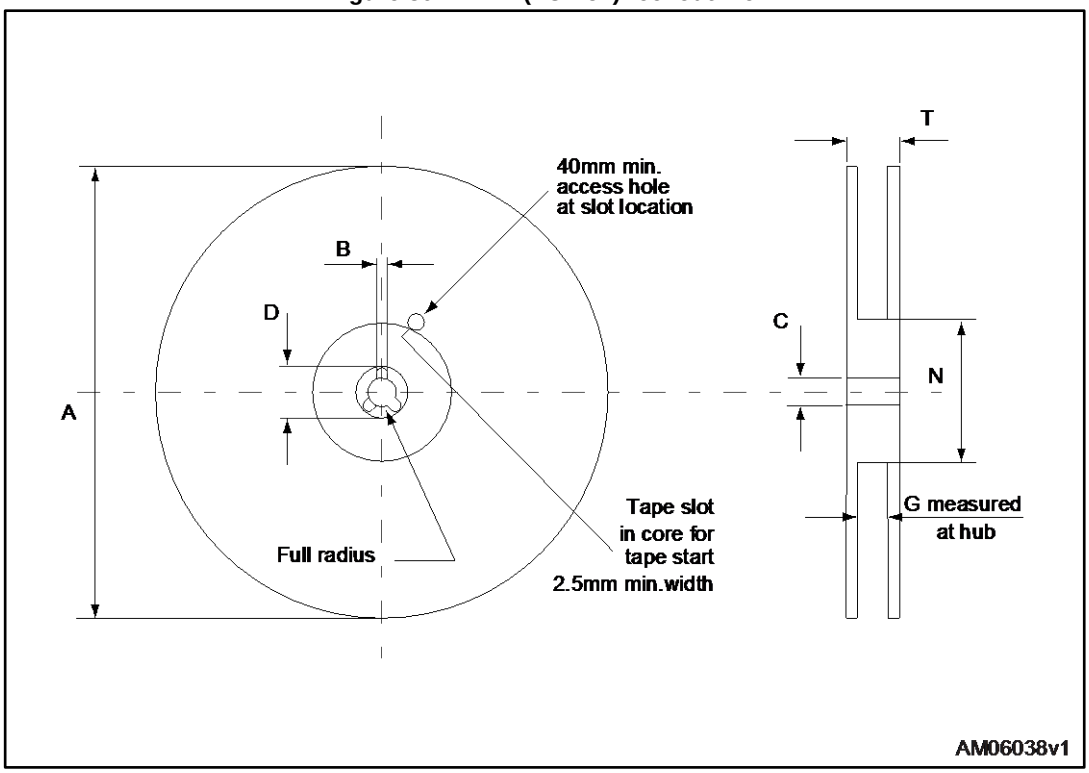


Table 13: DPAK (TO-252) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

5 Revision history

Table 14: Document revision history

Date	Revision	Changes
10-Feb-2011	1	First release.
17-Nov-2011	2	Updated features in table and description in cover page. Updated *Table 2: Absolute maximum ratings*, *Table 5: On /off states, Table 15: Normalized on resistance vs temperature*, *Figure 17: Normalized V_{DS} vs temperature* and *Section 4: Package mechanical data.*
03-Nov-2017	3	Modified *Table 3: "Thermal data"*. Modified *Section 4: "Package information"*. Minor text changes.

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