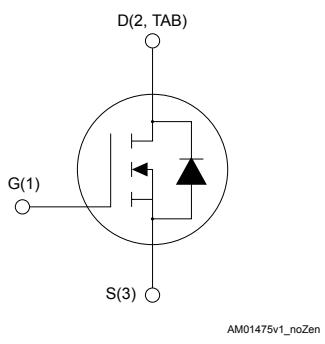
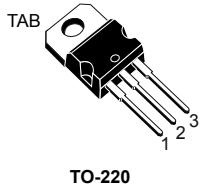


N-channel 600 V, 370 mΩ typ., 10 A FDmesh II Power MOSFET in a TO-220 package

Features



Order code	V_{DS} at T_J max.	$R_{DS(on)}$ max.	I_D
STP11NM60ND	650 V	450 mΩ	10 A

- Fast-recovery body diode
- Low gate charge and input capacitance
- Low on-resistance $R_{DS(on)}$
- 100% avalanche tested
- High dv/dt ruggedness

Applications

- Switching applications

Description

This FDmesh II Power MOSFET with fast-recovery body diode is produced using MDmesh II technology. Utilizing a new strip-layout vertical structure, this device features low on-resistance and superior switching performance. It is ideal for bridge topologies and ZVS phase-shift converters.



Product status link

[STP11NM60ND](#)

Product summary

Order code	STP11NM60ND
Marking	11NM60ND
Package	TO-220
Packing	Tube

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	600	V
V_{GS}	Gate-source voltage	± 25	V
I_D	Drain current (continuous) at $T_C = 25^\circ\text{C}$	10	A
	Drain current (continuous) at $T_C = 100^\circ\text{C}$	6.3	
$I_{DM}^{(1)}$	Drain current (pulsed)	40	A
P_{TOT}	Total power dissipation at $T_C = 25^\circ\text{C}$	90	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	40	V/ns
T_{stg}	Storage temperature range	-55 to 150	$^\circ\text{C}$
T_J	Maximum operating junction temperature	150	$^\circ\text{C}$

1. Pulse width is limited by safe operating area.
2. $I_{SD} \leq 10 \text{ A}$, $di/dt \leq 400 \text{ A}/\mu\text{s}$, $V_{DS} (\text{peak}) < V_{(BR)DSS}$, $V_{DD} = 80\% V_{(BR)DSS}$.

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	1.38	$^\circ\text{C}/\text{W}$
R_{thJA}	Thermal resistance, junction-to-ambient	62.5	$^\circ\text{C}/\text{W}$

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AS}	Avalanche current, repetitive or non-repetitive (pulse width limited by T_J max.)	3.5	A
E_{AS}	Single pulse avalanche energy (starting $T_J = 25^\circ\text{C}$, $I_D = I_{AS}$, $V_{DD} = 50 \text{ V}$)	200	mJ

2 Electrical characteristics

$T_C = 25^\circ\text{C}$ unless otherwise specified.

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(\text{BR})\text{DSS}}$	Drain-source breakdown voltage	$V_{GS} = 0 \text{ V}, I_D = 1 \text{ mA}$	600			V
$dv/dt^{(1)}$	Drain-source voltage slope	$V_{DD} = 480 \text{ V}, I_D = 10 \text{ A}, V_{GS} = 10 \text{ V}$		45		V/ns
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0 \text{ V}, V_{DS} = 600 \text{ V}$			1	μA
		$V_{GS} = 0 \text{ V}, V_{DS} = 600 \text{ V}, T_C = 125^\circ\text{C}^{(2)}$			100	
I_{GSS}	Gate-body leakage current	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA
$V_{GS(\text{th})}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$	3	4	5	V
$R_{D\text{S(on)}}$	Static drain-source on-resistance	$V_{GS} = 10 \text{ V}, I_D = 5 \text{ A}$		370	450	$\text{m}\Omega$

1. Value measured at turn off under inductive load.

2. Specified by design, not tested in production.

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 50 \text{ V}, f = 1 \text{ MHz}, V_{GS} = 0 \text{ V}$	-	850	-	pF
C_{oss}	Output capacitance		-	44	-	pF
C_{rss}	Reverse transfer capacitance		-	5	-	pF
$C_{oss \text{ eq.}}^{(1)}$	Equivalent output capacitance	$V_{GS} = 0 \text{ V}, V_{DS} = 0 \text{ to } 480 \text{ V}$	-	130	-	pF
R_G	Gate input resistance	$f = 1 \text{ MHz}, I_D = 0 \text{ A}$	-	3.7	-	Ω
Q_g	Total gate charge	$V_{DD} = 480 \text{ V}, I_D = 10 \text{ A}, V_{GS} = 0 \text{ to } 10 \text{ V}$ (see Figure 13. Test circuit for gate charge behavior)	-	30	-	nC
Q_{gs}	Gate-source charge		-	4	-	nC
Q_{gd}	Gate-drain charge		-	16	-	nC

1. $C_{oss \text{ eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS} .

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(\text{on})}$	Turn-on delay time	$V_{DD} = 300 \text{ V}, I_D = 10 \text{ A}, R_G = 4.7 \Omega, V_{GS} = 10 \text{ V}$ (see Figure 12. Test circuit for resistive load switching times and Figure 17. Switching time waveform)	-	16	-	ns
t_r	Rise time		-	7	-	ns
$t_{d(\text{off})}$	Turn-off delay time		-	50	-	ns
t_f	Fall time		-	9	-	ns

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		10	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		40	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 10 \text{ A}, V_{GS} = 0 \text{ V}$	-		1.3	V
t_{rr}	Reverse recovery time	$I_{SD} = 10 \text{ A}, dI/dt = 100 \text{ A}/\mu\text{s},$ $V_{DD} = 100 \text{ V}$	-	130		ns
Q_{rr}	Reverse recovery charge	(see Figure 14. Test circuit for inductive load switching and diode recovery times)	-	0.69		μC
I_{RRM}	Reverse recovery current		-	11		A
t_{rr}	Reverse recovery time	$I_{SD} = 10 \text{ A}, dI/dt = 100 \text{ A}/\mu\text{s},$ $V_{DD} = 100 \text{ V}, T_J = 150 \text{ }^\circ\text{C}$	-	200		ns
Q_{rr}	Reverse recovery charge	(see Figure 14. Test circuit for inductive load switching and diode recovery times)	-	1.2		μC
I_{RRM}	Reverse recovery current		-	12		A

1. Pulse width is limited by safe operating area.
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

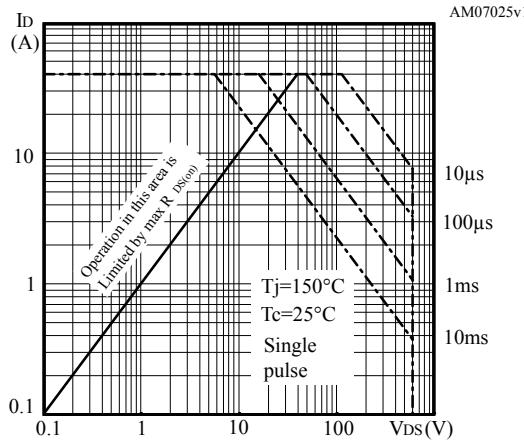


Figure 2. Normalized transient thermal impedance

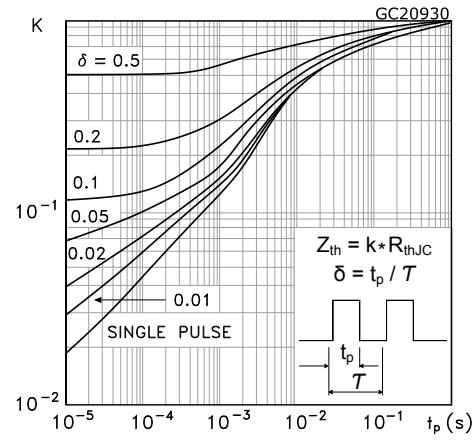


Figure 3. Typical drain-source on-resistance

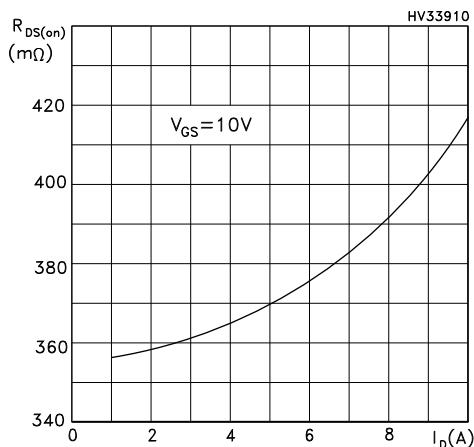


Figure 4. Typical output characteristics

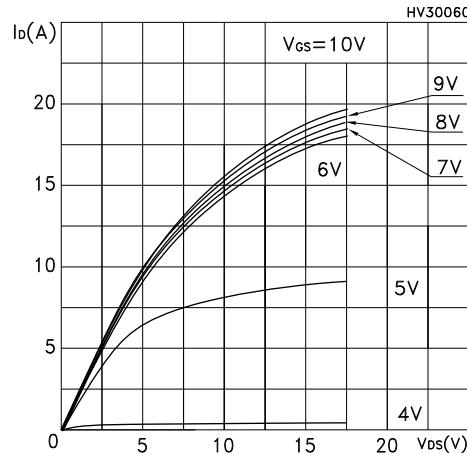


Figure 5. Typical transfer characteristics

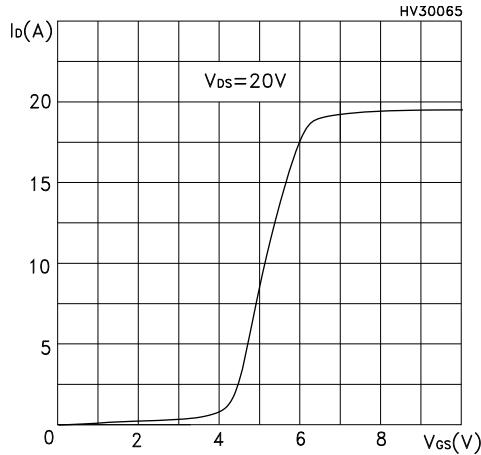


Figure 6. Normalized gate threshold vs temperature

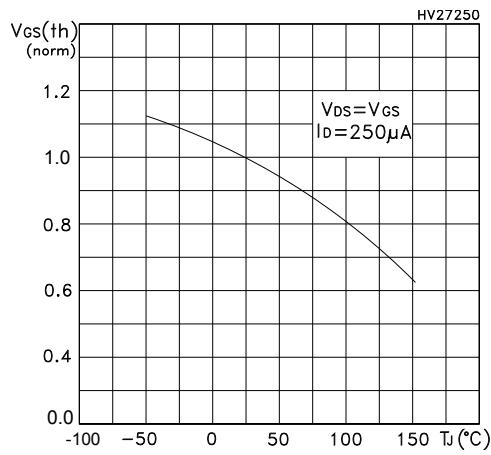
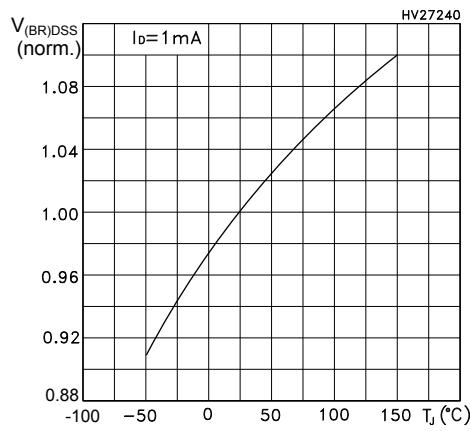
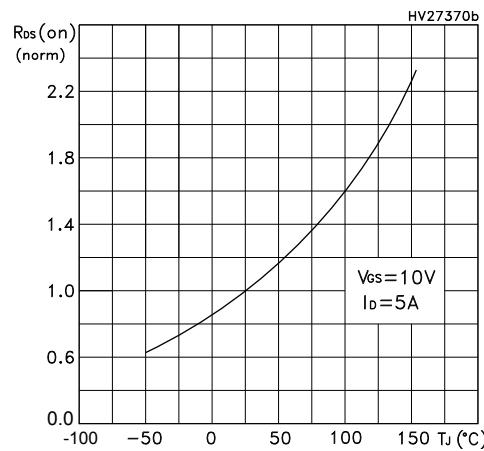
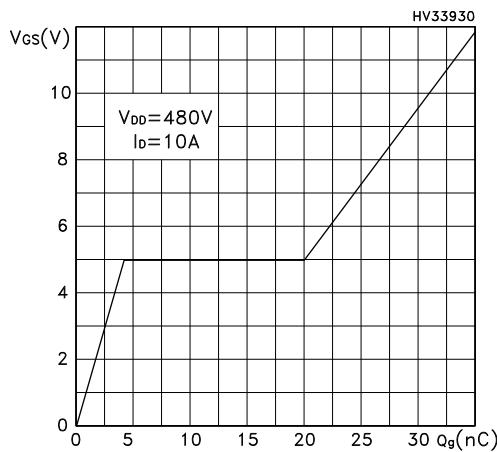
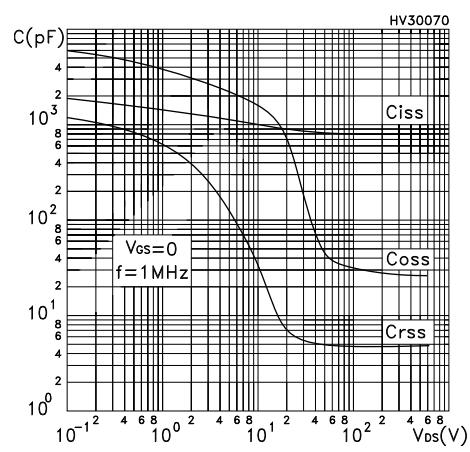
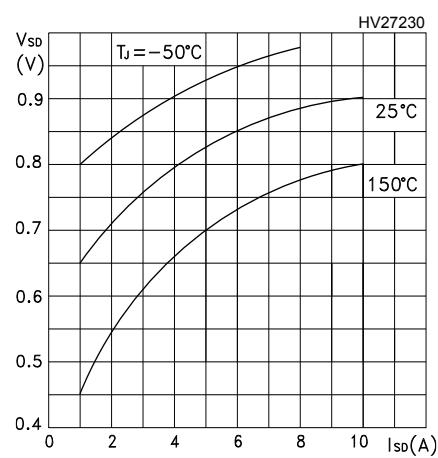
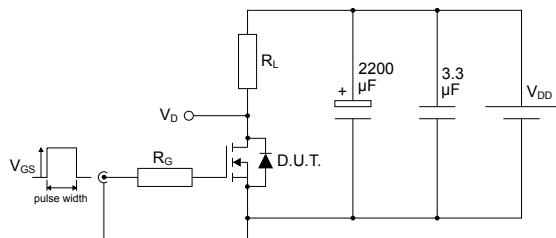


Figure 7. Normalized breakdown voltage vs temperature

Figure 8. Normalized on-resistance vs temperature

Figure 9. Typical gate charge characteristics

Figure 10. Typical capacitance characteristics

Figure 11. Typical reverse diode forward characteristics


3 Test circuits

Figure 12. Test circuit for resistive load switching times



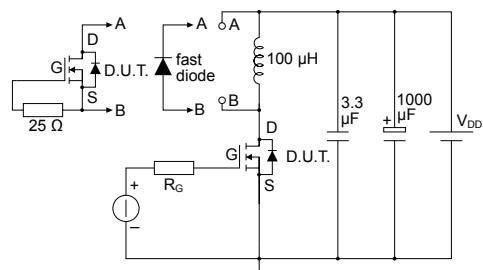
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Figure 13. Test circuit for gate charge behavior



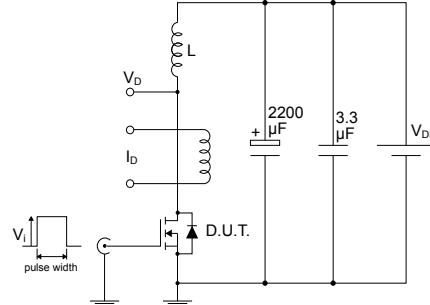
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Figure 14. Test circuit for inductive load switching and diode recovery times



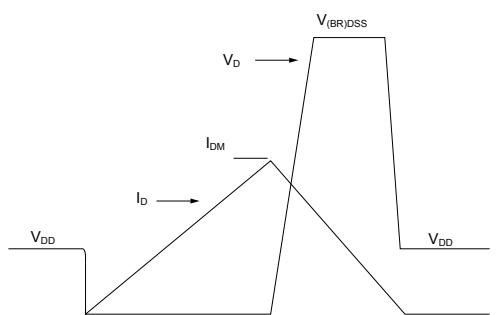
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Figure 15. Unclamped inductive load test circuit



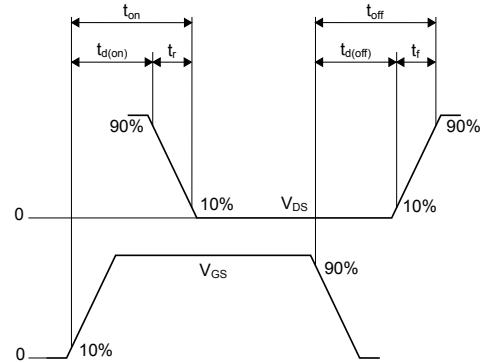
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Figure 16. Unclamped inductive waveform



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Figure 17. Switching time waveform



AM01473v1

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 TO-220 type A package information

Figure 18. TO-220 type A package outline

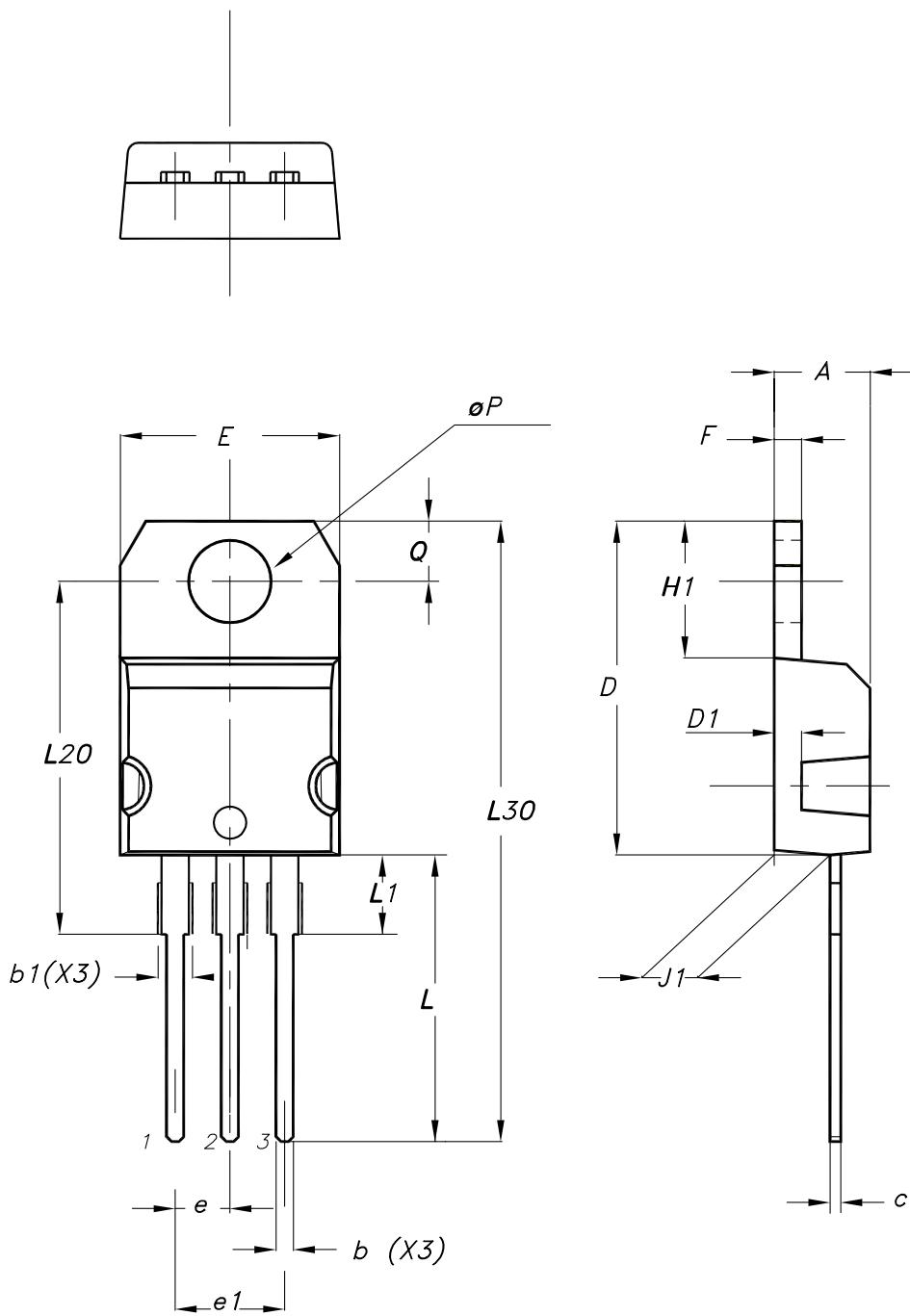


Table 8. TO-220 type A package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.55
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10.00		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13.00		14.00
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95
Slug flatness		0.03	0.10

Revision history

Table 9. Document revision history

Date	Revision	Changes
21-Jun-2023	1	First release. Part number previously included in datasheet DS5797.

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