



STB120NH03L - STI120NH03L STP120NH03L

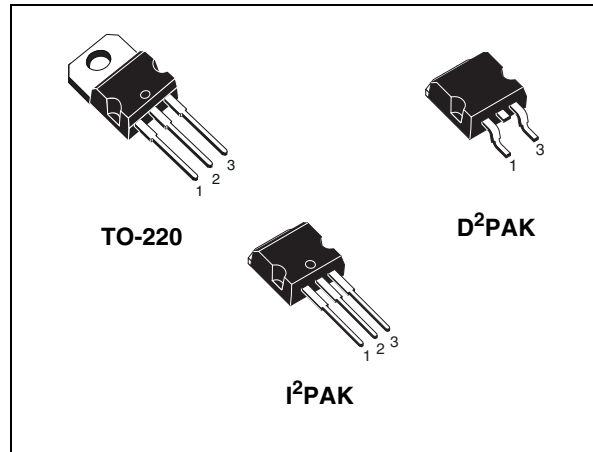
N-channel 30V - 0.005Ω - 60A - TO-220 / D²PAK / I²PAK
STripFET™ Power MOSFET for DC-DC conversion

General features

Type	V _{DSS}	R _{DS(on)}	I _D
STB120NH03L	30V	<0.0055Ω	60 ⁽¹⁾
STP120NH03L	30V	<0.0055Ω	60 ⁽¹⁾
STI120NH03L	30V	<0.0055Ω	60 ⁽¹⁾

1. Value limited by wire bonding

- R_{DS(on)} *Qg industry's benchmark Low
- Conduction losses reduced
- Switching losses reduced
- Low Threshold device



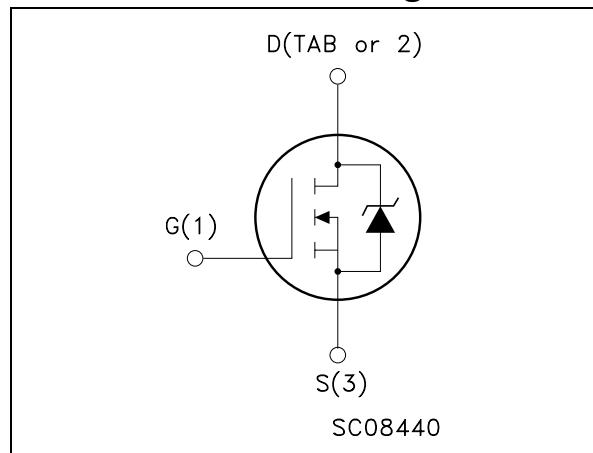
Description

These devices utilize the latest advanced design rules of ST's proprietary STripFET™ technology. It is ideal in high performance DC-DC converter applications where efficiency is to be achieved at very high output currents.

Applications

- Switching application

Internal schematic diagram



Order codes

Part number	Marking	Package	Packaging
STB120NH03L	B120NH03L	D ² PAK	Tape & reel
STI120NH03L	120NH03L	I ² PAK	Tube
STP120NH03L	P120NH03L	TO-220	Tube

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1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage ($V_{GS} = 0V$)	30	V
V_{GS}	Gate-source voltage	± 20	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25^\circ C$	60	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100^\circ C$	60	A
$I_{DM}^{(2)}$	Drain current (pulsed)	240	A
P_{TOT}	Total dissipation at $T_C = 25^\circ C$	110	W
	Derating factor	0.73	W/ $^\circ C$
EAS ⁽³⁾	Single pulse avalanche energy	700	mJ
T_J T_{stg}	Operating junction temperature Storage temperature	-55 to 175	$^\circ C$

1. Value limited by wire bonding
2. Pulse width limited by safe operating area
3. Starting $T_J = 25^\circ C$, $I_D = 30A$, $V_{DD} \leq 30V$

Table 2. Thermal data

R_{thJC}	Thermal resistance junction-case max	1.30	$^\circ C/W$
R_{thJA}	Thermal resistance junction-amb max	62.5	$^\circ C/W$
T_I	Maximum lead temperature for soldering purpose	300	$^\circ C$

2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Table 3. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	I _D = 250μA, V _{GS} = 0	30			V
I _{DSS}	Zero gate voltage drain current (V _{GS} = 0)	V _{DS} = Max rating, V _{DS} = Max rating, T _C =125°C			1 10	μA μA
I _{GSS}	Gate body leakage current (V _{DS} = 0)	V _{GS} = ±20V			±100	μA
V _{GS(th)}	Gate threshold voltage	V _{DS} = V _{GS} , I _D = 250μA	1	1.8	3	V
R _{DS(on)}	Static drain-source on resistance	V _{GS} = 10V, I _D = 30A V _{GS} = 5V, I _D = 30A		0.005 0.006	0.0055 0.0105	Ω Ω

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C _{iss} C _{oss} C _{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V _{DS} = 25V, f = 1MHz, V _{GS} = 0		4100 680 70		pF pF pF
t _{d(on)} t _r t _{d(off)} t _f	Turn-on delay time Rise time Off voltage rise time Fall time	V _{DD} = 15V, I _D = 30A, R _G = 4.7Ω, V _{GS} = 10V (see Figure 12)		16 95 48 23		ns ns ns ns
R _g	Gate input resistance	f = 1MHz gate DC bias=0 test signal level=20mV open drain		1.3		Ω
Q _g Q _{gs} Q _{gd}	Total gate charge Gate-source charge Gate-drain charge	V _{DD} =15V, I _D = 60A V _{GS} =10V (see Figure 13)		57 12 7	77	nC nC nC
Q _{oss} ⁽¹⁾	Output charge	V _{DS} = 24V, V _{GS} = 0		27		ns
Q _{gls} ⁽²⁾	Third-quadrant gate charge	V _{DS} < 0, V _{GS} = 0V		55		ns

1. Q_{oss} = C_{oss} * ΔV_{IN}, C_{oss} = C_{gd} + C_{ds}. See power losses calculation

2. Gate charge for synchronous operation.

Table 5. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM}	Source-drain current Source-drain current (pulsed)				60 240	A A
$V_{SD}^{(1)}$	Forward on voltage	$I_{SD} = 30A$, $V_{GS} = 0$			1.4	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD} = 60A$, $di/dt = 100A/\mu s$, $V_{DD} = 30V$, $T_J = 150^\circ C$		46 64 2.8		ns nC A

1. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

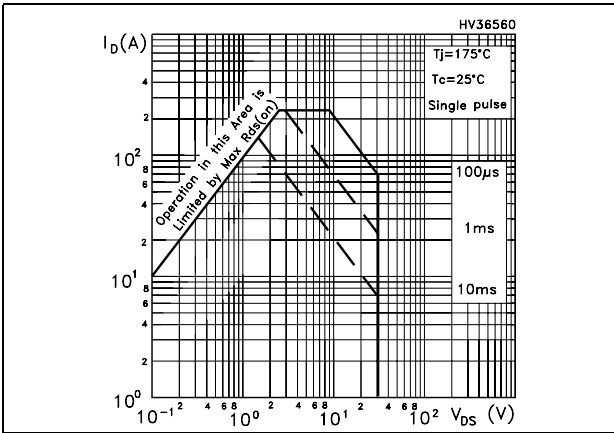


Figure 2. Thermal impedance

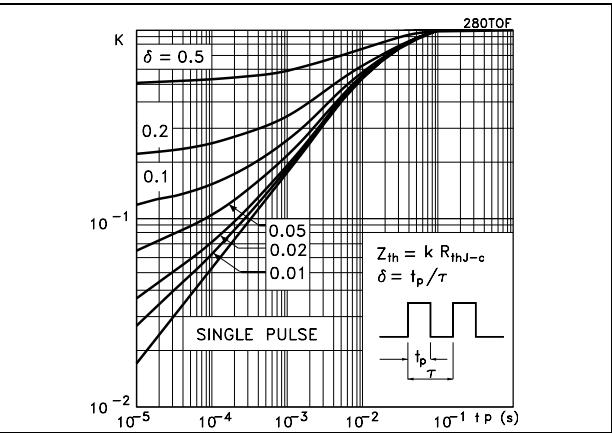


Figure 3. Output characteristics

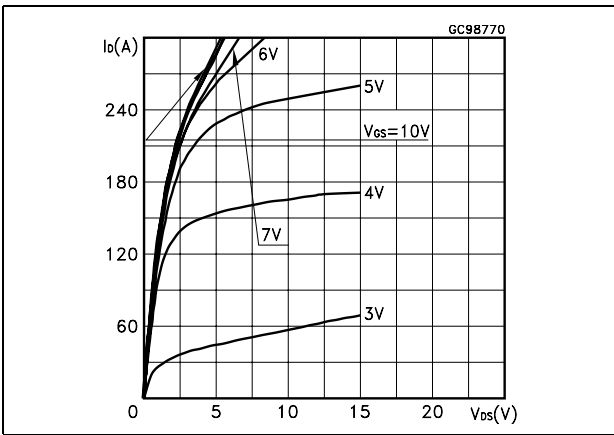


Figure 4. Transfer characteristics

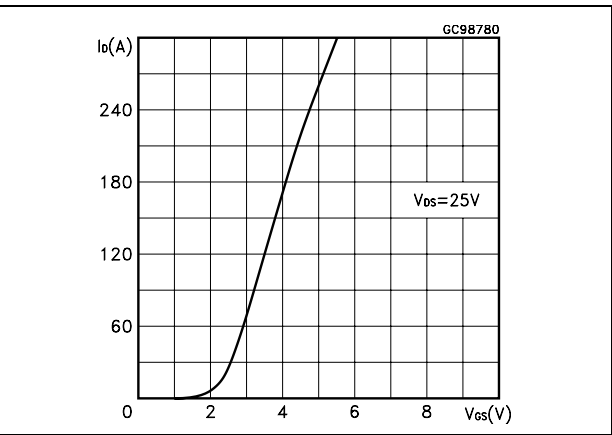


Figure 5. Normalized B_VDSS vs temperature

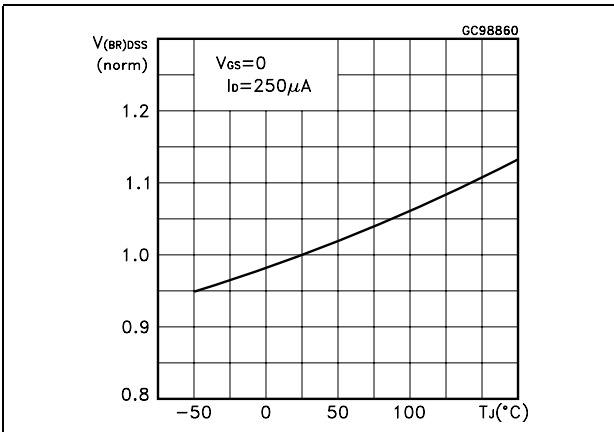


Figure 6. Static drain-source on resistance

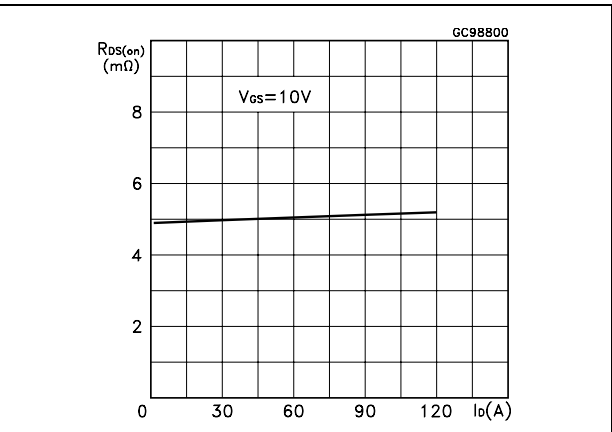


Figure 7. Gate charge vs gate-source voltage Figure 8. Capacitance variations

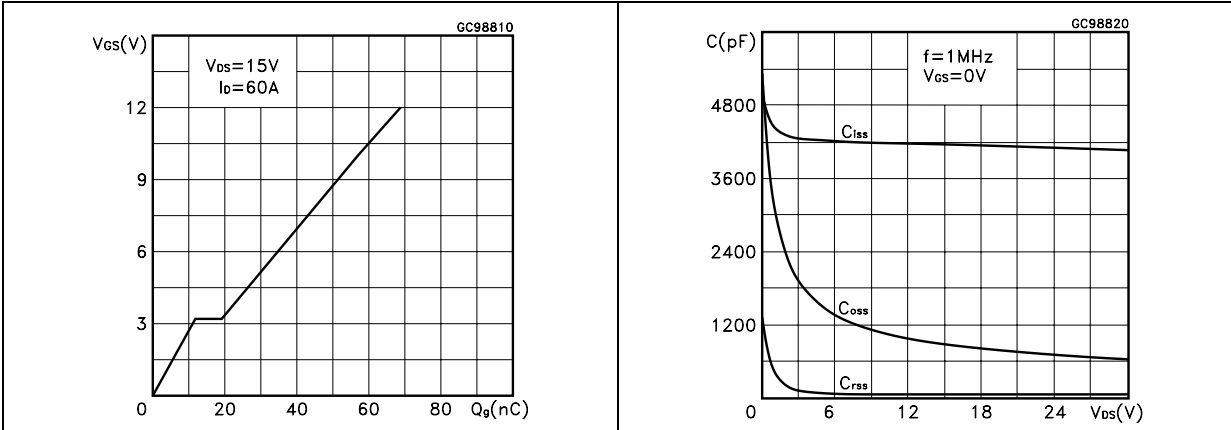


Figure 9. Normalized gate threshold voltage vs temperature Figure 10. Normalized on resistance vs temperature

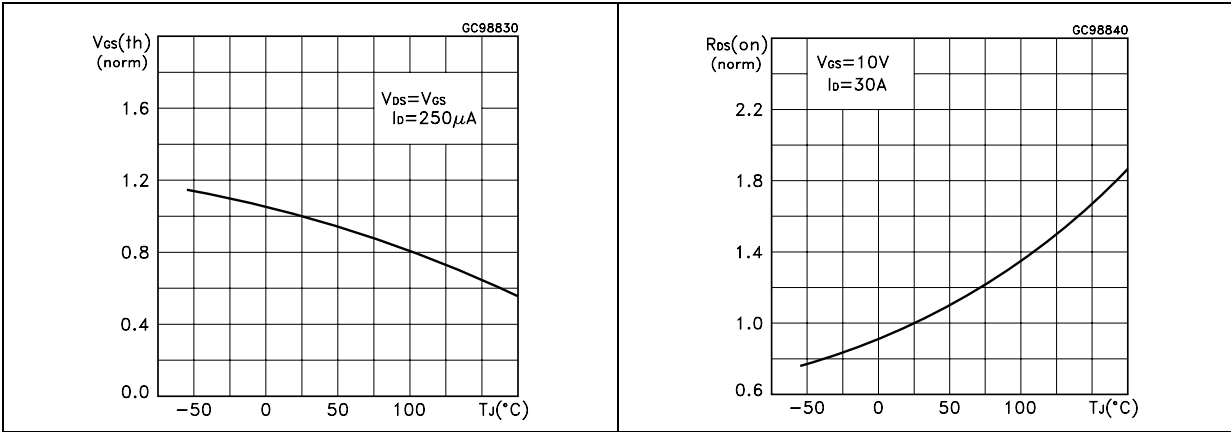
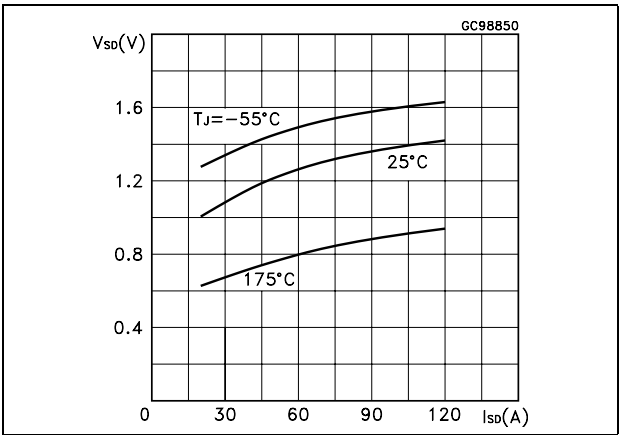


Figure 11. Source-drain diode forward characteristics



3 Test circuit

Figure 12. Switching times test circuit for resistive load

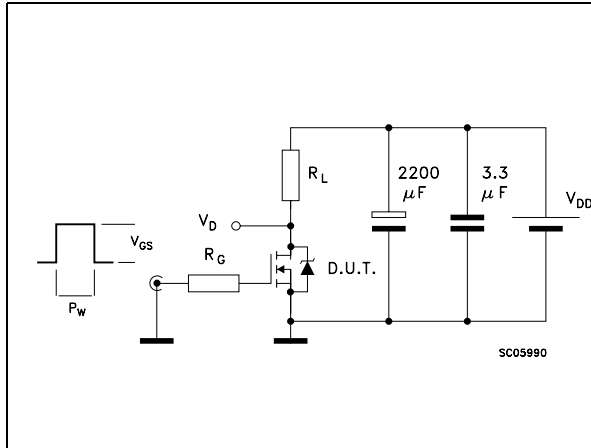


Figure 13. Gate charge test circuit

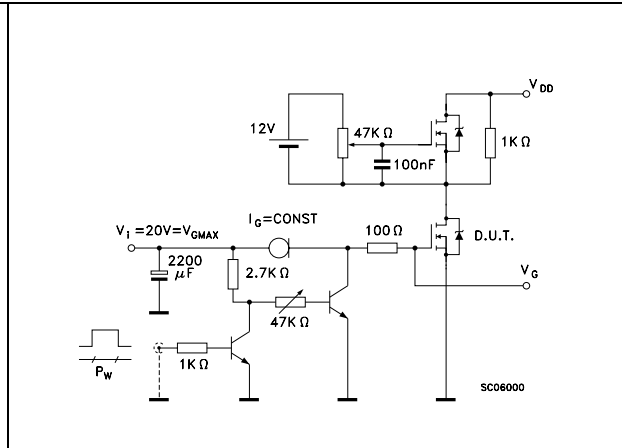


Figure 14. Test circuit for inductive load switching and diode recovery times



Figure 15. Unclamped Inductive load test circuit

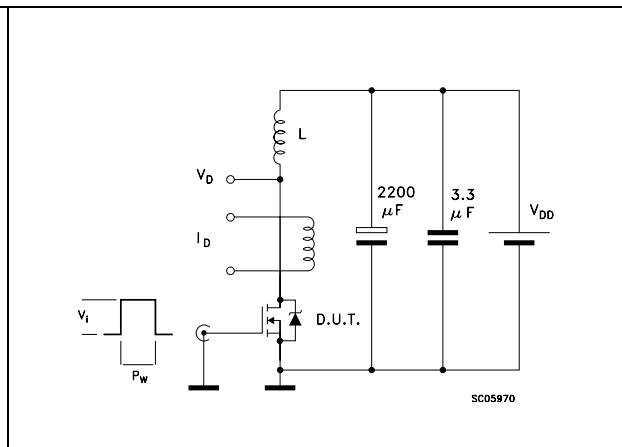


Figure 16. Unclamped inductive waveform

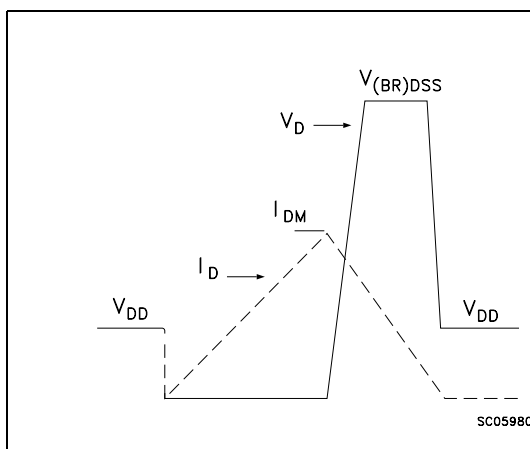
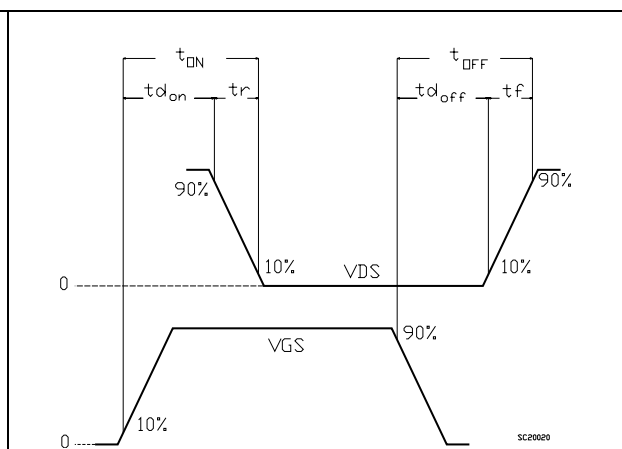


Figure 17. Switching time waveform

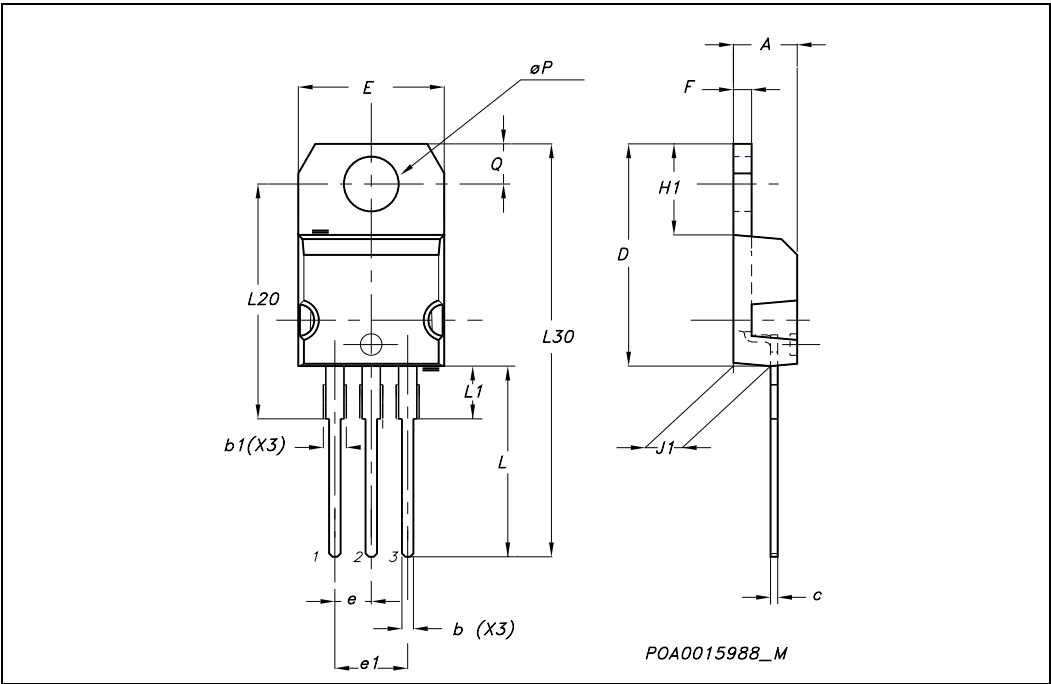


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

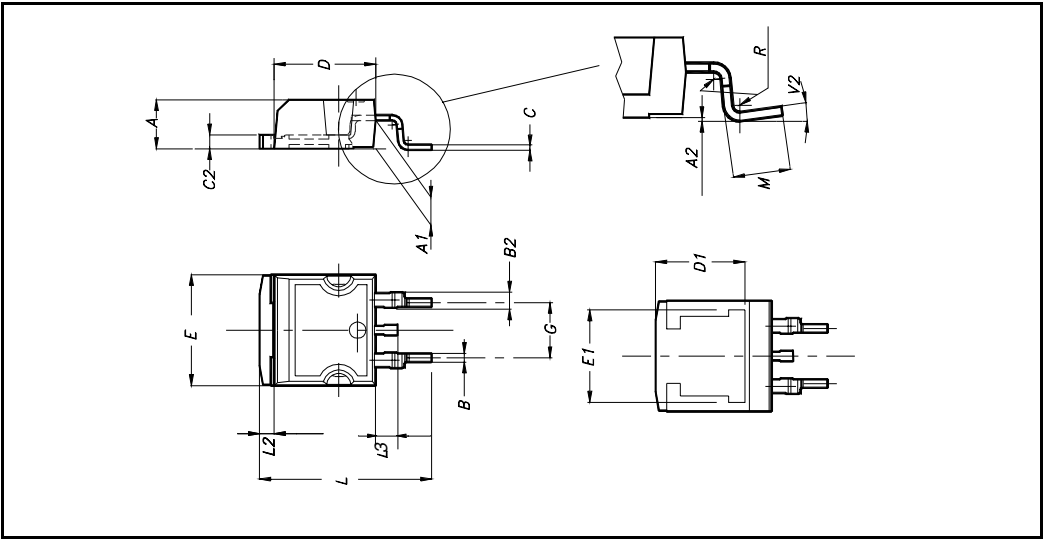
TO-220 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.15		1.70	0.045		0.066
c	0.49		0.70	0.019		0.027
D	15.25		15.75	0.60		0.620
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.052
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
øP	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116



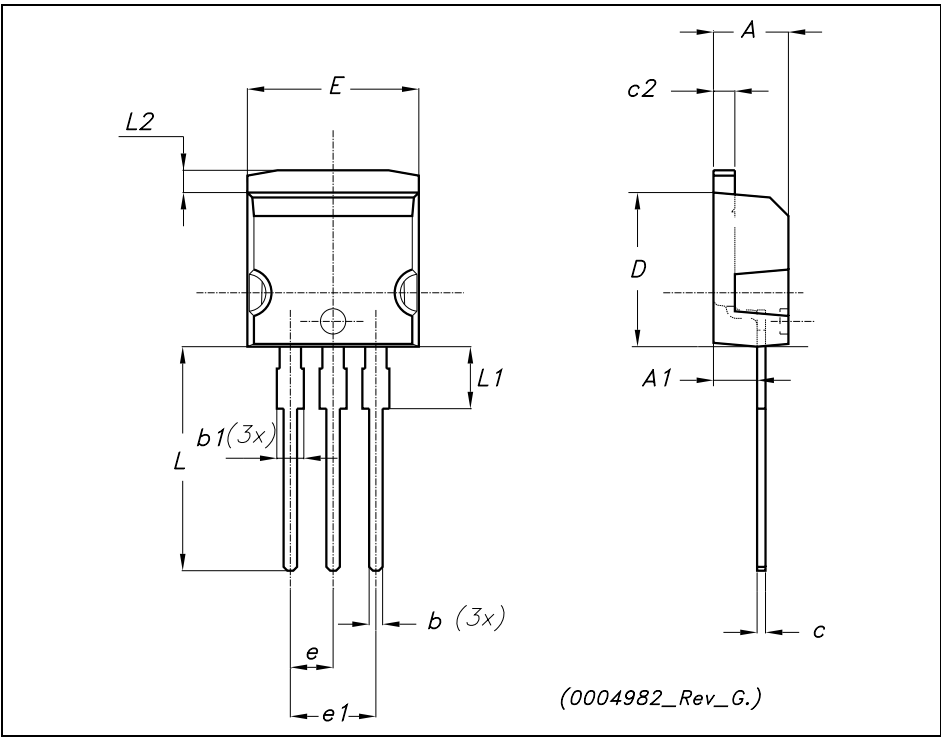
D²PAK MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
A1	2.49		2.69	0.098		0.106
A2	0.03		0.23	0.001		0.009
B	0.7		0.93	0.027		0.036
B2	1.14		1.7	0.044		0.067
C	0.45		0.6	0.017		0.023
C2	1.23		1.36	0.048		0.053
D	8.95		9.35	0.352		0.368
D1		8			0.315	
E	10		10.4	0.393		
E1		8.5			0.334	
G	4.88		5.28	0.192		0.208
L	15		15.85	0.590		0.625
L2	1.27		1.4	0.050		0.055
L3	1.4		1.75	0.055		0.068
M	2.4		3.2	0.094		0.126
R		0.4			0.015	
V2	0°		4°			



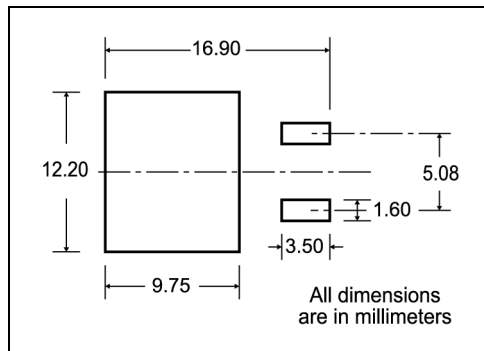
TO-262 (I²PAK) MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
A1	2.40		2.72	0.094		0.107
b	0.61		0.88	0.024		0.034
b1	1.14		1.70	0.044		0.066
c	0.49		0.70	0.019		0.027
c2	1.23		1.32	0.048		0.052
D	8.95		9.35	0.352		0.368
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
E	10		10.40	0.393		0.410
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L2	1.27		1.40	0.050		0.055

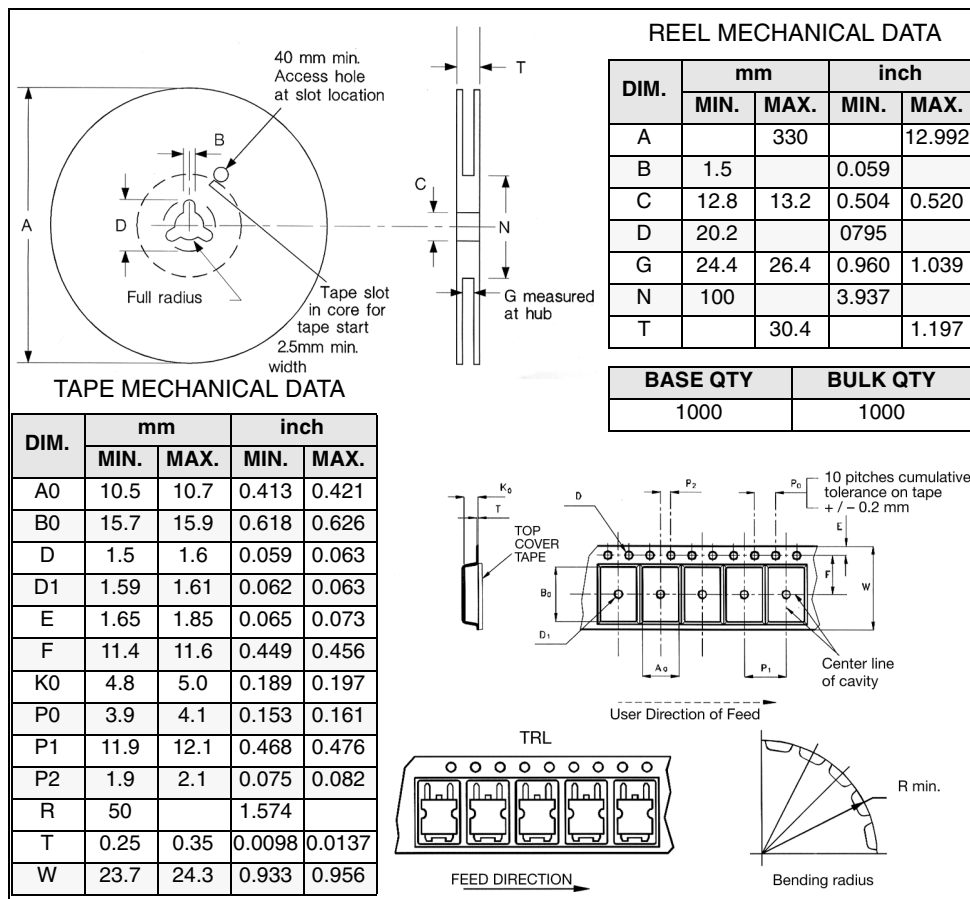


5 Packing mechanical data

D²PAK FOOTPRINT



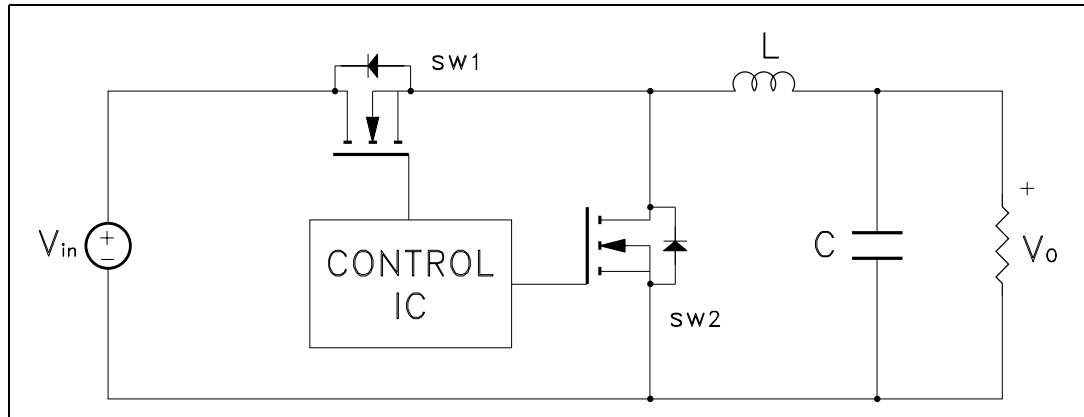
TAPE AND REEL SHIPMENT



* on sales type

6 Appendix A

Figure 18. Buck converter: power losses estimation



The power losses associated with the FETs in a synchronous buck converter can be estimated using the equations shown in the table below. The formulas give a good approximation, for the sake of performance comparison, of how different pairs of devices affect the converter efficiency. However a very important parameter, the working temperature, is not considered. The real device behavior is really dependent on how the heat generated inside the devices is removed to allow for a safer working junction temperature.

- The low side (SW2) device requires:
 - Very low $R_{DS(on)}$ to reduce conduction losses
 - Small Q_{gl} to reduce the gate charge losses
 - Small C_{oss} to reduce losses due to output capacitance
 - Small Q_{rr} to reduce losses on SW1 during its turn-on
 - The C_{gd}/C_{gs} ratio lower than V_{th}/V_{gg} ratio especially with low drain to source voltage to avoid the cross conduction phenomenon;
- The high side (SW1) device requires:
 - Small R_g and L_s to allow higher gate current peak and to limit the voltage feedback on the gate
 - Small Q_g to have a faster commutation and to reduce gate charge losses
 - Low $R_{DS(on)}$ to reduce the conduction losses.

Table 6. Power losses calculation

		High side switching (SW1)	Low side switch (SW2)
Pconduction		$R_{DS(on)SW1} * I_L^2 * \delta$	$R_{DS(on)SW2} * I_L^2 * (1 - \delta)$
Pswitching		$V_{in} * (Q_{gsth(SW1)} + Q_{gd(SW1)}) * f * \frac{I_L}{I_g}$	Zero Voltage Switching
Pdiode	Recovery ⁽¹⁾	Not applicable	$V_{in} * Q_{rr(SW2)} * f$
	Conduction	Not applicable	$V_{f(SW2)} * I_L * t_{deadtime} * f$
Pgate(Q _G)		$Q_{g(SW1)} * V_{gg} * f$	$Q_{gls(SW2)} * V_{gg} * f$
P _{Qoss}		$\frac{V_{in} * Q_{oss(SW1)} * f}{2}$	$\frac{V_{in} * Q_{oss(SW2)} * f}{2}$

1. Dissipated by SW1 during turn-on

Table 7. Parameters meaning

Parameter	Meaning
d	Duty-cycle
Q _{gsth}	Post threshold gate charge
Q _{gls}	Third quadrant gate charge
Pconduction	On state losses
Pswitching	On-off transition losses
Pdiode	Conduction and reverse recovery diode losses
Pgate	Gate drive losses
P _{Qoss}	Output capacitance losses

7 Revision history

Table 8. Revision history

Date	Revision	Changes
20-Dec-2004	4	First release
20-Dec-2005	5	New device inserted
19-Jun-2006	6	The document has been reformatted
16-Feb-2007	7	Added I ² PAK package

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