

N-channel 1200 V, 0.62 Ω typ., 12 A MDmesh K5 Power MOSFETs
in H²PAK-2, TO-220, TO-247 and TO-247 long leads

Datasheet - production data

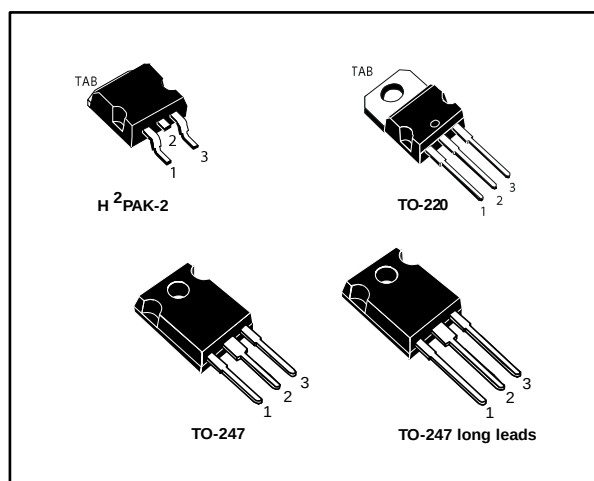
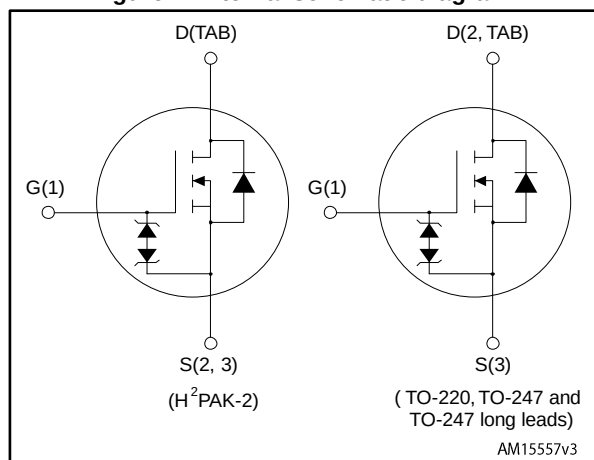


Figure 1: Internal schematic diagram



Features

Order codes	V _{DS}	R _{DS(on)} max.	I _D	P _{TOT}
STH12N120K5-2	1200 V	0.69 Ω	12 A	250 W
STP12N120K5				
STW12N120K5				
STWA12N120K5				

- Worldwide best FOM (figure of merit)
- Ultra-low gate charge
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

These very high voltage N-channel Power MOSFETs are designed using MDmesh™ K5 technology based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance and ultra-low gate charge for applications requiring superior power density and high efficiency.

Table 1: Device summary

Order code	Marking	Package	Packing
STH12N120K5-2	12N120K5	H ² PAK-2	Tape and reel
STP12N120K5		TO-220	Tube
STW12N120K5		TO-247	
STWA12N120K5		TO-247 long leads	

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1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 30	V
I_D	Drain current at $T_C = 25\text{ }^{\circ}\text{C}$	12	A
I_D	Drain current at $T_C = 100\text{ }^{\circ}\text{C}$	7.6	A
$I_{DM}^{(1)}$	Drain current (pulsed)	48	A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^{\circ}\text{C}$	250	W
$I_{AR}^{(2)}$	Max current during repetitive or single pulse avalanche	4	A
$E_{AS}^{(3)}$	Single pulse avalanche energy	215	mJ
$dv/dt^{(4)}$	Peak diode recovery voltage slope	4.5	V/ns
$dv/dt^{(5)}$	MOSFET dv/dt ruggedness	50	V/ns
T_j T_{stg}	Operating junction temperature Storage temperature	- 55 to 150	$^{\circ}\text{C}$

Notes:

⁽¹⁾Pulse width limited by safe operating area.

⁽²⁾Pulse width limited by T_{Jmax} .

⁽³⁾Starting $T_J = 25\text{ }^{\circ}\text{C}$, $I_D = I_{AS}$, $V_{DD} = 50\text{ V}$

⁽⁴⁾ $I_{SD} \leq 12\text{ A}$, $di/dt \leq 100\text{ A}/\mu\text{s}$, $V_{Peak} \leq V_{(BR)DSS}$

⁽⁵⁾ $V_{DS} \leq 960\text{ V}$

Table 3: Thermal data

Symbol	Parameter	Value			Unit
		H ² PAK-2	TO-220	TO-247 TO-247 long leads	
$R_{thj-case}$	Thermal resistance junction-case max	0.5			$^{\circ}\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-amb max		62.5	50	$^{\circ}\text{C}/\text{W}$
$R_{thj-pcb}$	Thermal resistance junction-pcb max	30			$^{\circ}\text{C}/\text{W}$

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 4: On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	V _{GS} = 0 V, I _D = 1 mA	1200			V
I _{DSS}	Zero gate voltage drain current	V _{GS} = 0 V, V _{DS} = 1200 V			1	μA
		V _{GS} = 0, V _{DS} = 1200 V, T _C = 125 °C			50	μA
I _{GSS}	Gate body leakage current	V _{DS} = 0 V, V _{GS} = ± 20 V			±10	μA
V _{GS(th)}	Gate threshold voltage	V _{DS} = V _{GS} , I _D = 100 μA	3	4	5	V
R _{DS(on)}	Static drain-source on-resistance	V _{GS} = 10 V, I _D = 6 A		0.62	0.69	Ω

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C _{iss}	Input capacitance	V _{GS} = 0 V, V _{DS} = 100 V, f = 1 MHz	-	1370	-	pF
C _{oss}	Output capacitance		-	110	-	pF
C _{rss}	Reverse transfer capacitance		-	0.6	-	pF
C _{o(tr)} ⁽¹⁾	Equivalent capacitance, time-related	V _{GS} = 0, V _{DS} = 0 to 960 V	-	128	-	pF
C _{o(er)} ⁽²⁾	Equivalent capacitance, energy-related		-	42	-	pF
R _G	Intrinsic gate resistance	f = 1 MHz, I _D = 0 A	-	3	-	Ω
Q _g	Total gate charge	V _{DD} = 960 V, I _D = 12 A	-	44.2	-	nC
Q _{gs}	Gate-source charge	V _{GS} = 10 V	-	7.3	-	nC
Q _{gd}	Gate-drain charge	(see Figure 18: "Gate charge test circuit")	-	30	-	nC

Notes:

⁽¹⁾Time-related is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

⁽²⁾Energy-related is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 600\text{ V}$, $I_D = 6\text{ A}$, $R_G = 4.7\ \Omega$, $V_{GS} = 10\text{ V}$ (see Figure 20: "Unclamped inductive load test circuit")	-	23	-	ns
t_r	Rise time		-	11	-	ns
$t_{d(off)}$	Turn-off delay time		-	68.5	-	ns
t_f	Fall time		-	18.5	-	ns

Table 7: Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		12	A
I_{SDM}	Source-drain current (pulsed)		-		48	A
$V_{SD}^{(1)}$	Forward on voltage	$I_{SD} = 12\text{ A}$, $V_{GS} = 0\text{ V}$	-		1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 12\text{ A}$, $V_{DD} = 60\text{ V}$ $di/dt = 100\text{ A}/\mu\text{s}$, (see Figure 19: "Test circuit for inductive load switching and diode recovery times")	-	630		ns
Q_{rr}	Reverse recovery charge		-	12.6		μC
I_{RRM}	Reverse recovery current		-	40		A
t_{rr}	Reverse recovery time	$I_{SD} = 12\text{ A}$, $V_{DD} = 60\text{ V}$ $di/dt = 100\text{ A}/\mu\text{s}$, $T_j = 150\text{ }^\circ\text{C}$ (see Figure 19: "Test circuit for inductive load switching and diode recovery times")	-	892		ns
Q_{rr}	Reverse recovery charge		-	15.6		μC
I_{RRM}	Reverse recovery current		-	35		A

Notes:

⁽¹⁾Pulsed: pulse duration = 300 μs , duty cycle 1.5%

Table 8: Gate-source Zener diode

Symbol	Parameter	Test conditions	Min	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	$I_{GS} = \pm 1\text{ mA}$, $I_D = 0\text{ A}$	30	-		V

The built-in back-to-back Zener diodes have been specifically designed to enhance the ESD capability of the device. The Zener voltage is appropriate for efficient and cost-effective intervention to protect the device integrity. These integrated Zener diodes thus eliminate the need for external components.

2.1 Electrical characteristics (curves)

Figure 2: Safe operating area for H²PAK-2 and TO-220

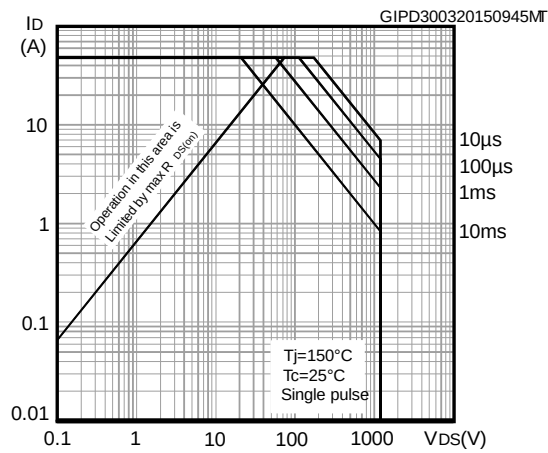


Figure 3: Thermal impedance for H²PAK-2 and TO-220

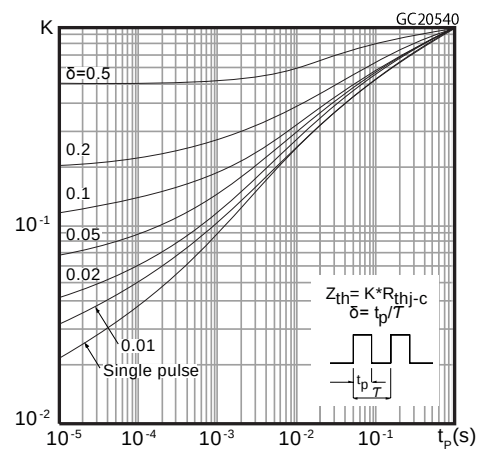


Figure 4: Safe operating area for TO-247 and TO-247 long leads

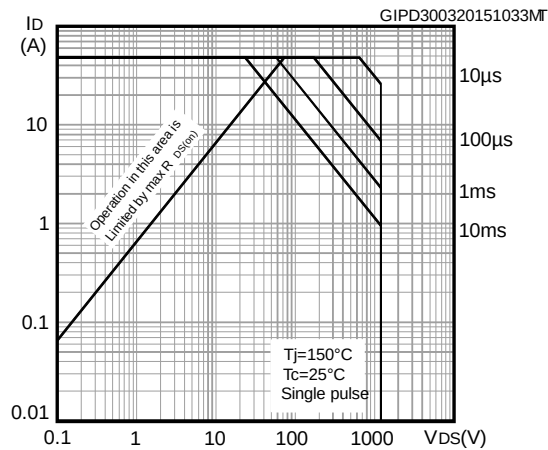


Figure 5: Thermal impedance for TO-247 and TO-247 long leads

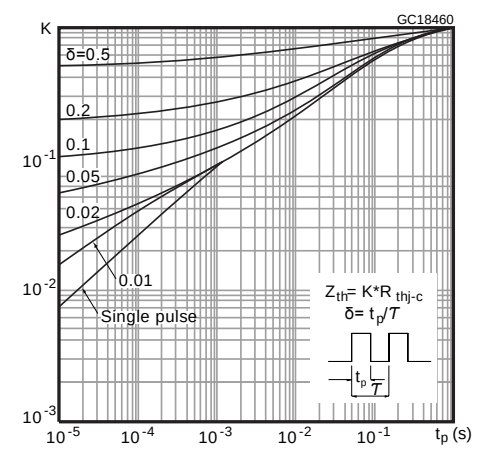


Figure 6: Output characteristics

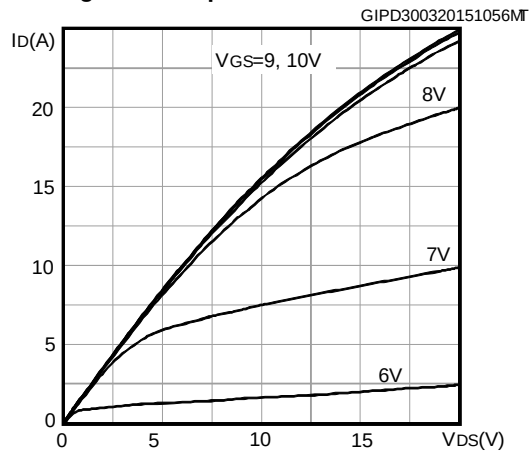


Figure 7: Transfer characteristics

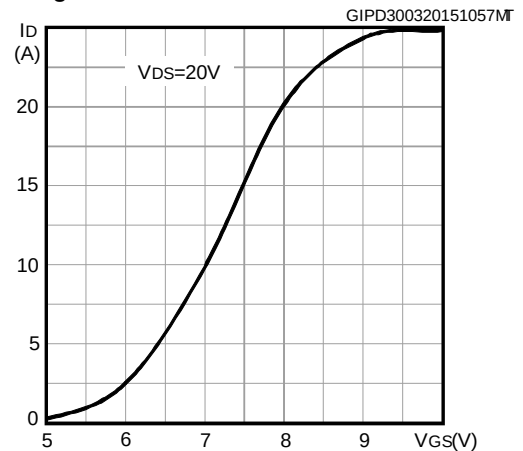


Figure 8: Gate charge vs gate-source voltage

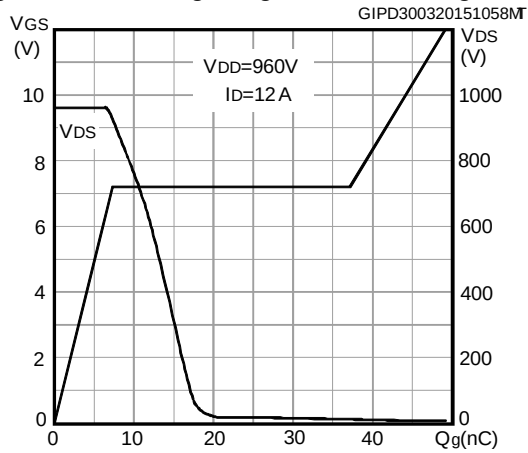


Figure 9: Static drain-source on-resistance

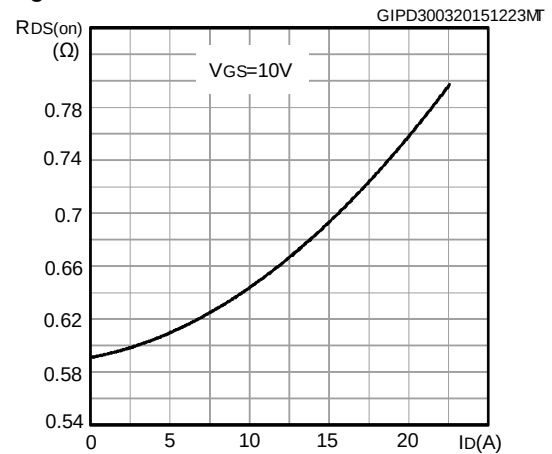


Figure 10: Capacitance variations

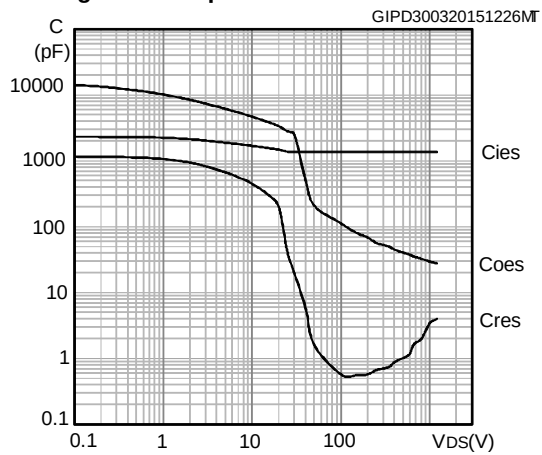


Figure 11: Output capacitance stored energy

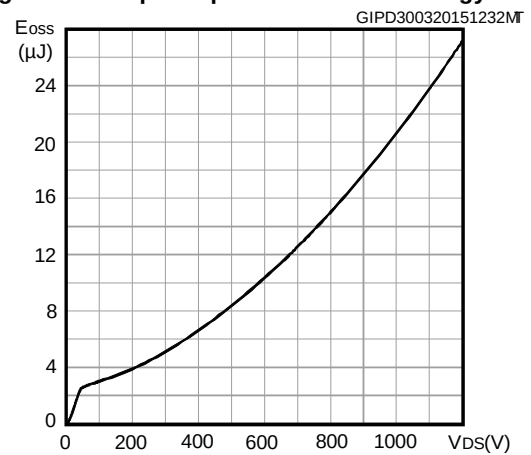


Figure 12: Normalized gate threshold voltage vs temperature

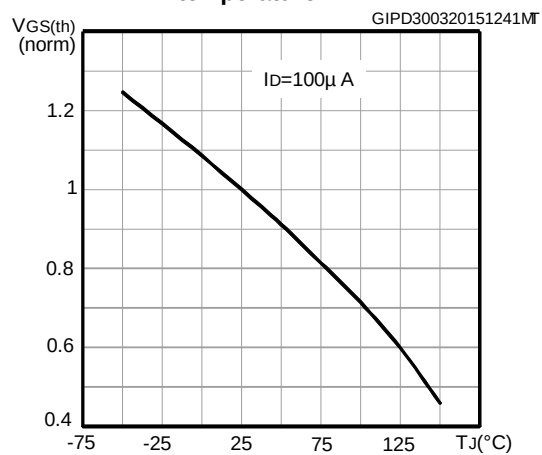


Figure 13: Normalized on-resistance vs temperature

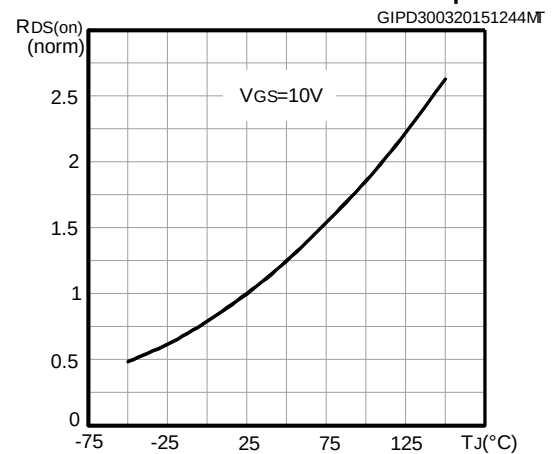


Figure 14: Normalized $V_{(BR)DSS}$ vs temperature

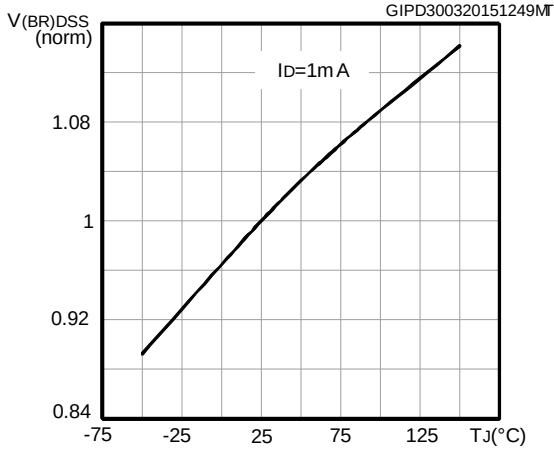


Figure 15: Source-drain diode forward characteristics

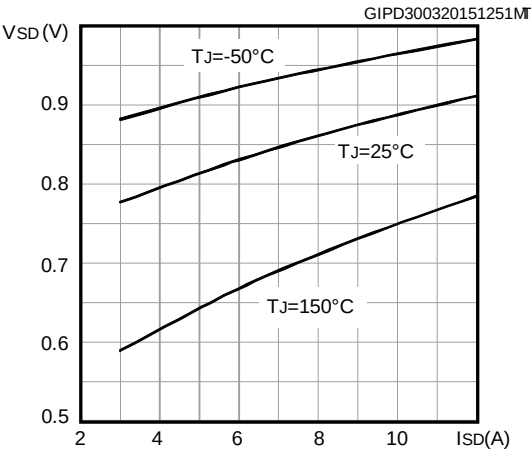
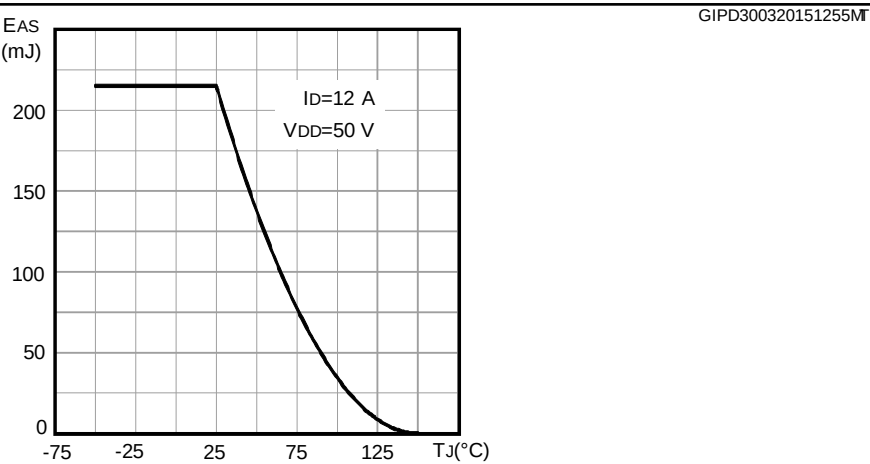


Figure 16: Maximum avalanche energy vs starting T_J



AM01468v1

AM01469v1

AM01470v1

AM01471v1

AM01472v1

AM01473v1

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: **www.st.com**. ECOPACK[®] is an ST trademark.

4.1 H²PAK-2 package information

Figure 23: H²PAK-2 package outline

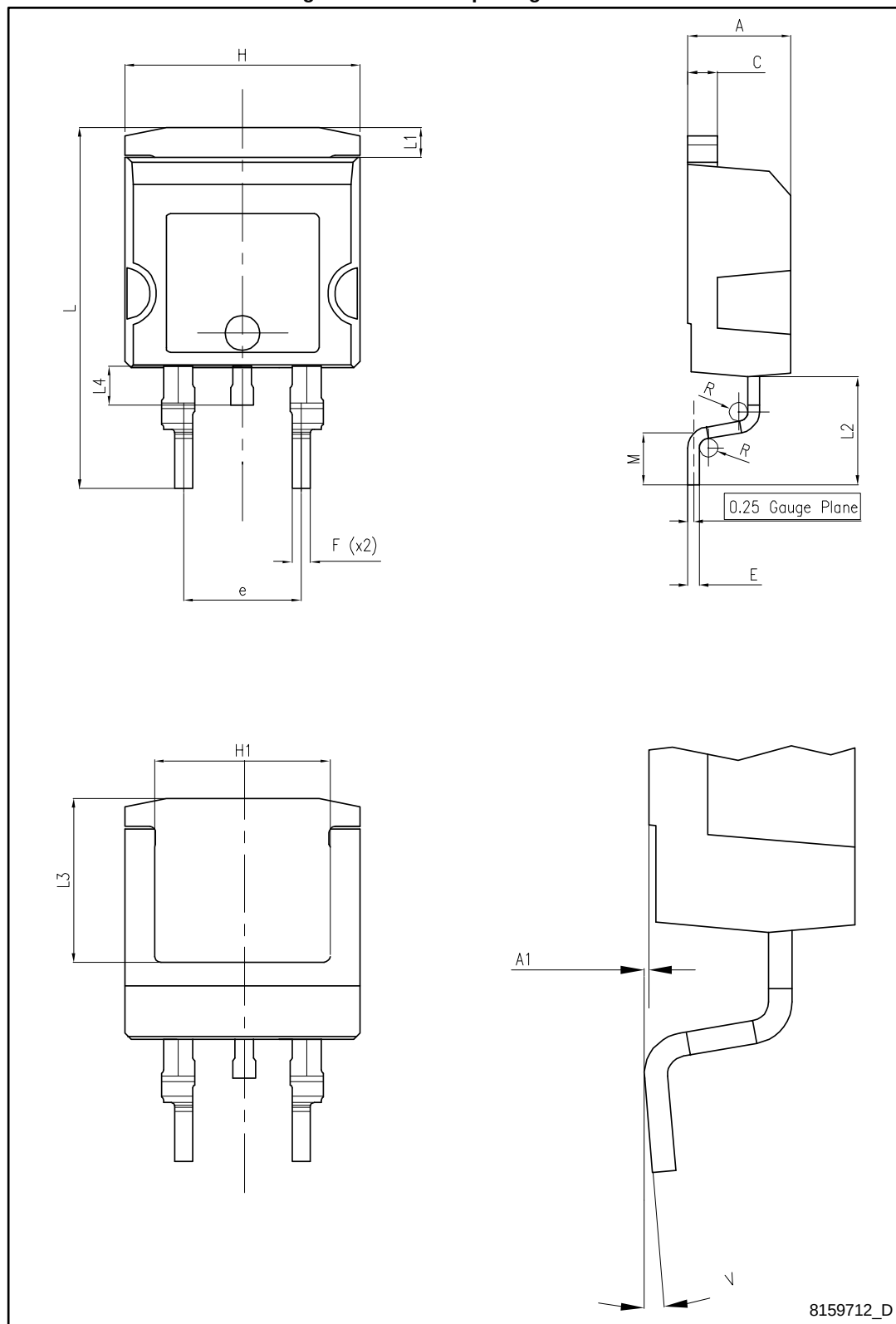
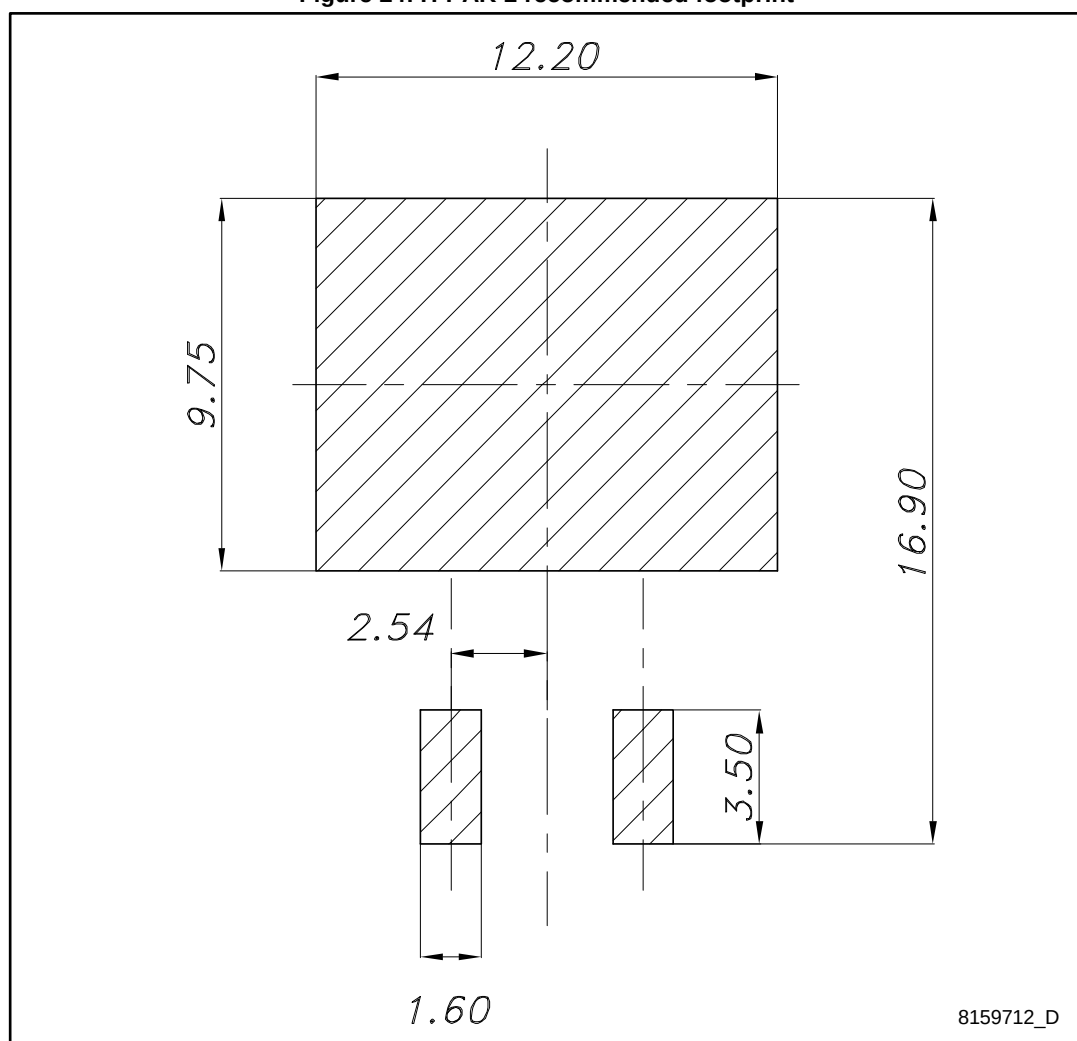


Table 9: H²PAK-2 mechanical data

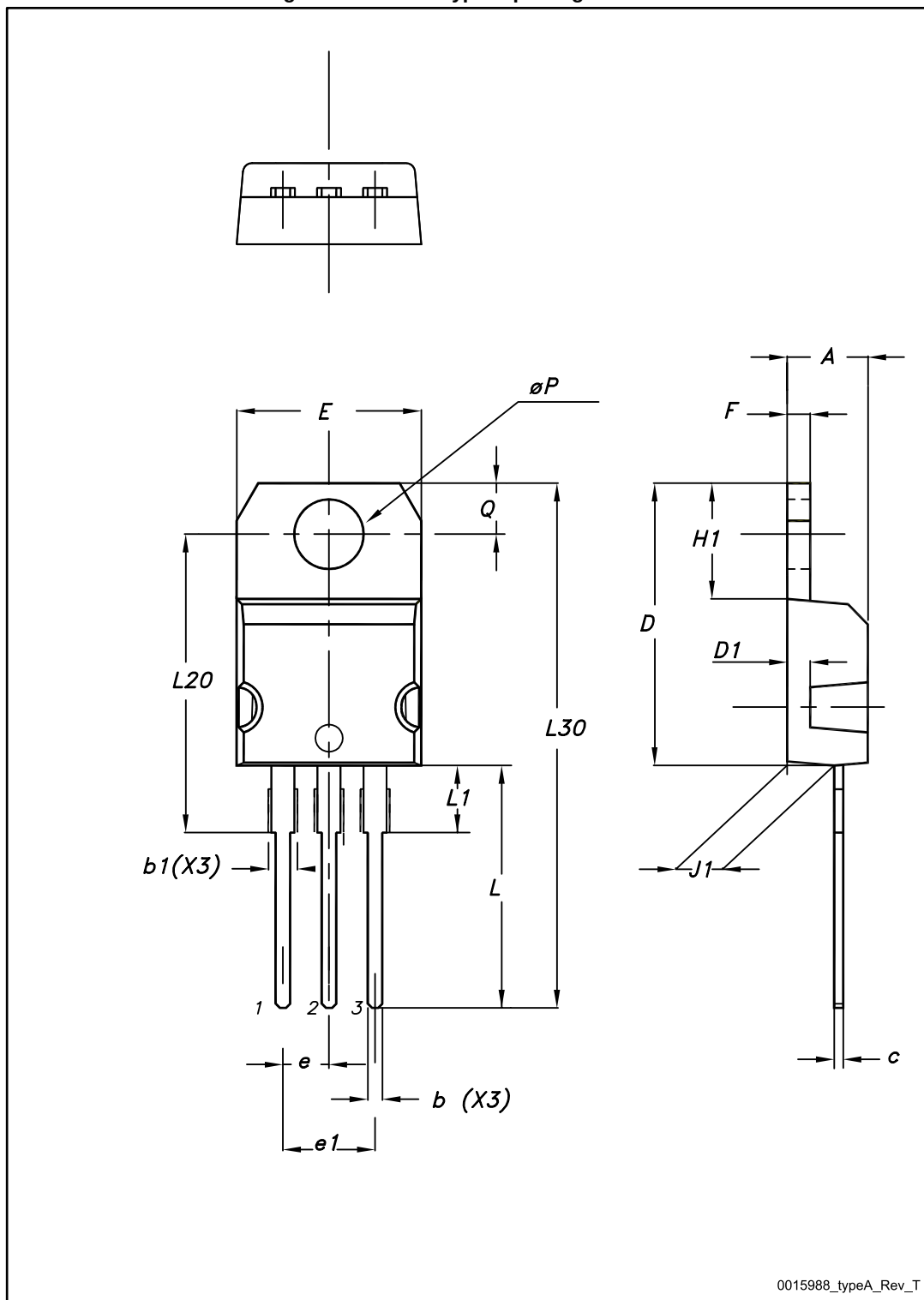
Dim.	mm		
	Min.	Typ.	Max.
A	4.30	-	4.80
A1	0.03		0.20
C	1.17		1.37
e	4.98		5.18
E	0.50		0.90
F	0.78		0.85
H	10.00		10.40
H1	7.40		7.80
L	15.30		15.80
L1	1.27		1.40
L2	4.93		5.23
L3	6.85		7.25
L4	1.5		1.7
M	2.6		2.9
R	0.20		0.60
V	0°		8°

Figure 24: H²PAK-2 recommended footprint



4.2 TO-220 type A package information

Figure 25: TO-220 type A package outline



0015988_typeA_Rev_T

Table 10: TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95

4.3 TO-247 package information

Figure 26: TO-247 package outline

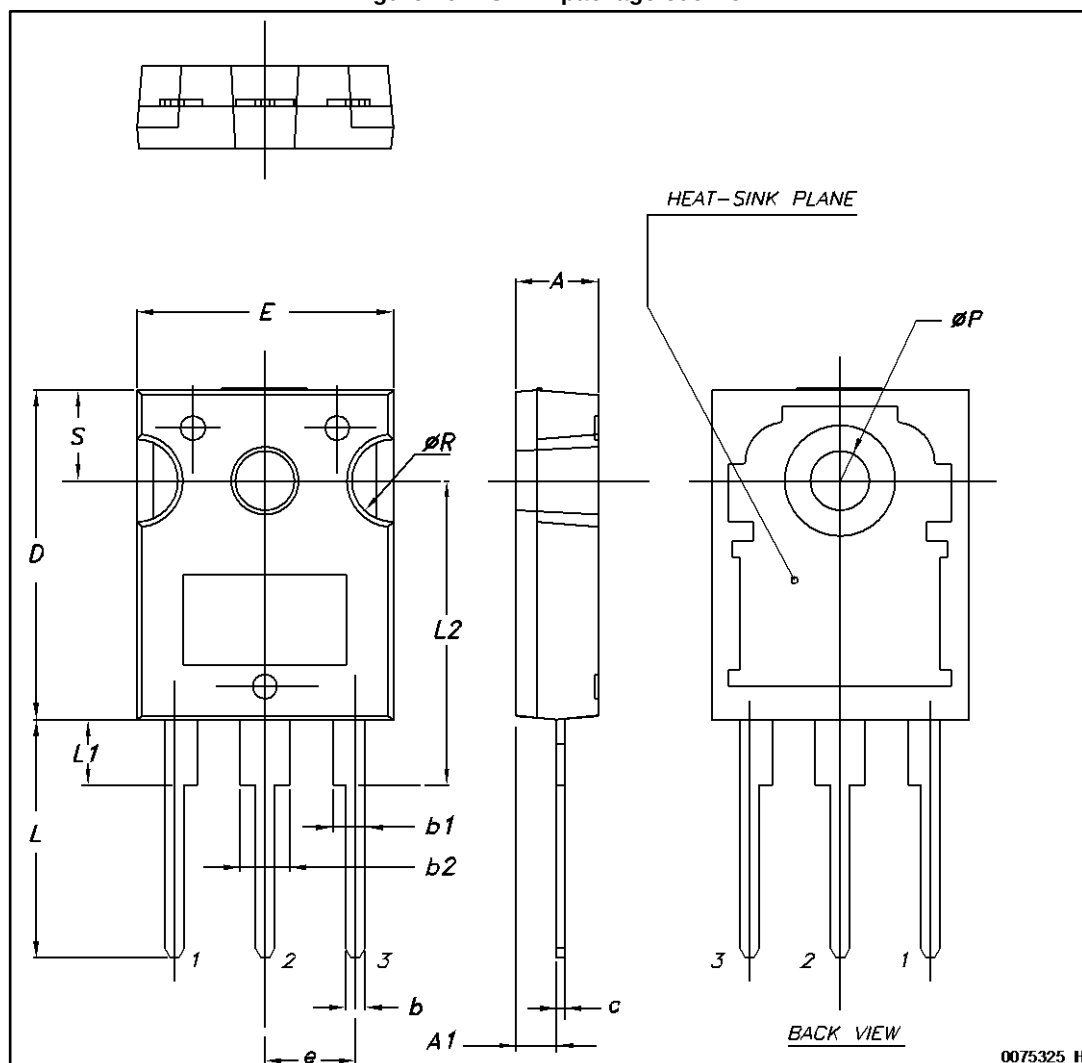
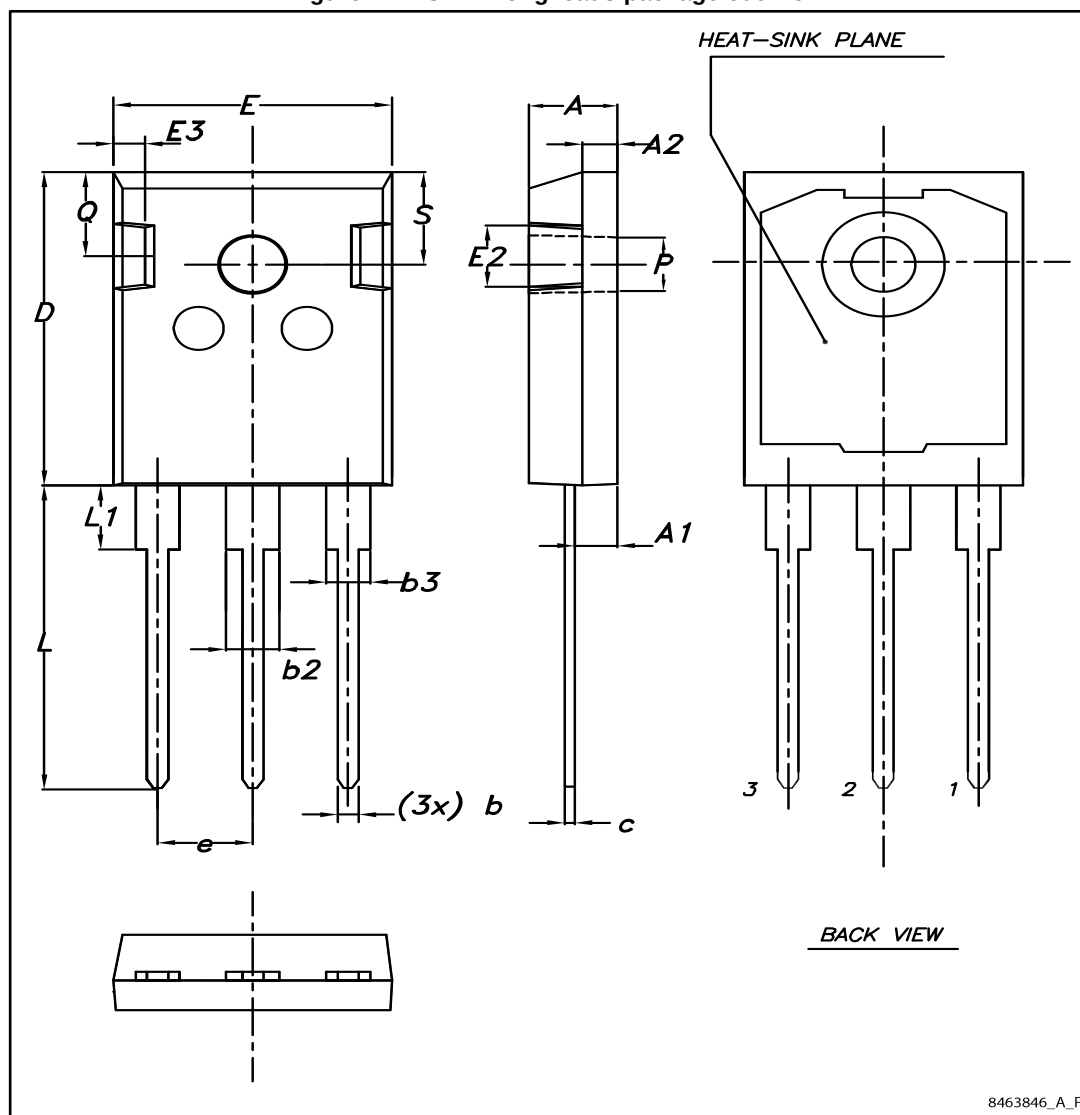


Table 11: TO-247 mechanical data

Dim.	mm.		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e	5.30	5.45	5.60
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
ØP	3.55		3.65
ØR	4.50		5.50
S	5.30	5.50	5.70

4.4 TO-247 long leads package information

Figure 27: TO-247 long leads package outline



8463846_A_F

Table 12: TO-247 long leads mechanical data

Dim.	mm.		
	Min.	Typ.	Max.
A	4.90	5.00	5.10
A1	2.31	2.41	2.51
A2	1.90	2.00	2.10
b	1.16		1.26
b2			3.25
b3			2.25
c	0.59		0.66
D	20.90	21.00	21.10
E	15.70	15.80	15.90
E2	4.90	5.00	5.10
E3	2.40	2.50	2.60
e	5.34	5.44	5.54
L	19.80	19.92	20.10
L1			4.30
P	3.50	3.60	3.70
Q	5.60		6.00
S	6.05	6.15	6.25

5 Revision history

Table 13: Document revision history

Date	Revision	Changes
23-Aug-2011	1	First release.
17-Jan-2013	2	- Minor text changes - Added: H²PAK package - The part number STB12N120K5 has been moved to a separate datasheet - Updated: - Updated: mechanical data for TO-247 package
16-May-2014	3	- The part numbers STFW12N120K5 has been moved to a separate datasheet - Added: TO-247 long leads package - Modified: I_{AR}, E_{AS}, dv/dt values in Table 2: "Absolute maximum ratings" - Modified: the entire typical values in Table 5: "Dynamic", Table 6: "Switching times" and Table 7: "Source drain diode" - Added: Section 2.1: "Electrical characteristics (curves)" - Minor text changes
08-Apr-2015	4	Updated title, silhouette and description in cover page. Updated Table 4: "On/off states", Table 5: "Dynamic", Figure 9: "Static drain-source on-resistance" and Figure 10: "Capacitance variations". Minor text change.

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