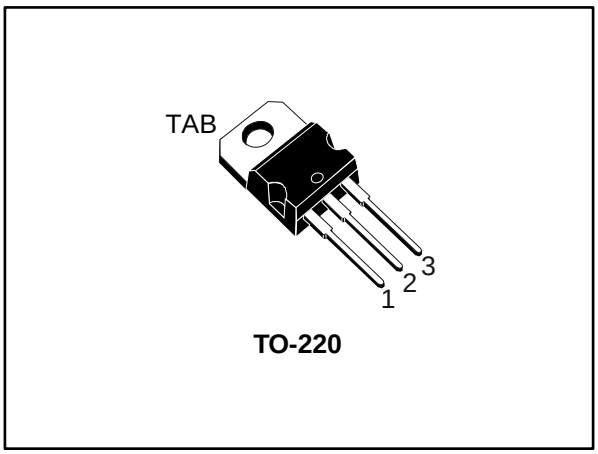
STP130N8F7

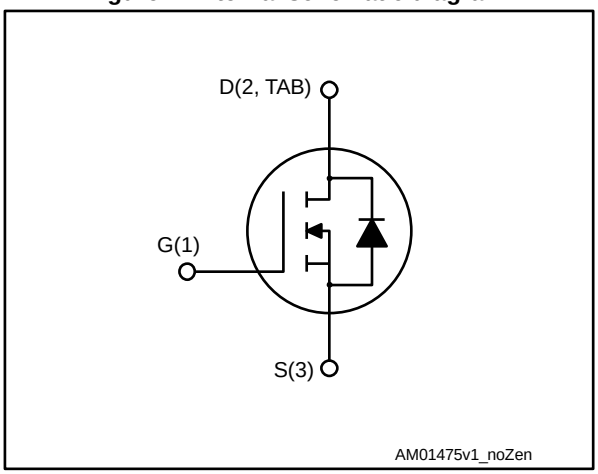
N-channel 80 V, 5.0 mΩ typ., 80 A STripFET™ F7 Power MOSFET in a TO-220 package

Datasheet - production data



TO-220

Figure 1: Internal schematic diagram



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D	P_{TOT}
STP130N8F7	80 V	5.8 mΩ	80 A	205 W

- Among the lowest $R_{DS(on)}$ on the market
- Excellent FoM (figure of merit)
- Low C_{rss}/C_{iss} ratio for EMI immunity
- High avalanche ruggedness

Applications

- Switching applications

Description

This N-channel Power MOSFET utilizes STripFET™ F7 technology with an enhanced trench gate structure that results in very low on-state resistance, while also reducing internal capacitance and gate charge for faster and more efficient switching.

Table 1: Device summary

Order code	Marking	Package	Packing
STP130N8F7	130N8F7	TO-220	Tube

This is information on a product in full production.

www.st.com

Contents

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	80	V
V_{GS}	Gate-source voltage	±20	V
I_D	Drain current (continuous) at T_C= 25 °C	80	A
I_D	Drain current (continuous) at T_C= 100 °C	80	A
I_{DM}(1)	Drain current (pulsed)	320	A
P_{TOT}	Total dissipation at T_C= 25 °C	205	W
E_{AS}(2)	Single pulse avalanche energy	320	mJ
T_j	Operating junction temperature range	-55 to 175	°C
T_{stg}	Storage temperature range		

Notes:

(1)Pulse width is limited by safe operating area

(2)Starting T_j =25 °C, I_D = 40 A, V_{DD} = 40 V

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case	0.73	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient	62.5	°C/W

2 Electrical characteristics

(T_{CASE}= 25 °C unless otherwise specified)

Table 4: On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS}= 0 V, I_D= 250 µA	80			V
I_{DSS}	Zero gate voltage drain current	V_{GS}= 0 V, V_{DS}= 80 V			1	µA
		V_{GS}= 0 V, V_{DS}= 80 V, T_J=125 °C(1)			100	µA
I_{GSS}	Gate-source leakage current	V_{DS}= 0 V, V_{GS}= 20 V			100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS}= V_{GS}, I_D= 250 µA	2.5		4.5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS}= 10 V, I_D= 40 A		5.0	5.8	mΩ

Notes:

(1)Defined by design, not subject to production test.

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS}= 25 V, f = 1 MHz, V_{GS}= 0 V	-	4500	-	pF
C_{oss}	Output capacitance		-	1100	-	pF
C_{rss}	Reverse transfer capacitance		-	110	-	pF
Q_g	Total gate charge	V_{DD}= 40 V, I_D= 80 A, V_{GS}= 0 to 10 V (see *Figure 14: "Test circuit for gate charge behavior"*)	-	60	-	nC
Q_{gs}	Gate-source charge		-	25	-	nC
Q_{gd}	Gate-drain charge		-	15	-	nC

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD}= 40 V, I_D= 40 A, R_G = 4.7 Ω, V_{GS}= 10 V (see *Figure 13: "Test circuit for resistive load switching times"* and *Figure 18: "Switching time waveform"*)	-	140	-	ns
t_r	Rise time		-	210	-	ns
$t_{d(off)}$	Turn-off-delay time		-	190	-	ns
t_f	Fall time		-	120	-	ns

Table 7: Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{SD}(1)	Forward on voltage	I_{SD}= 80 A, V_{GS}= 0 V	-		1.2	V
t_{rr}	Reverse recovery time	I_{SD}= 80 A, di/dt = 100 A/µs, V_{DD}= 80 V, T_j= 150 °C (see *Figure 15: "Test circuit for inductive load switching and diode recovery times"*)	-	45		ns
Q_{rr}	Reverse recovery charge		-	54		nC
I_{RRM}	Reverse recovery current		-	2.5		A

Notes:

(1)Pulse test: pulse duration = 300 µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2: Safe operating area

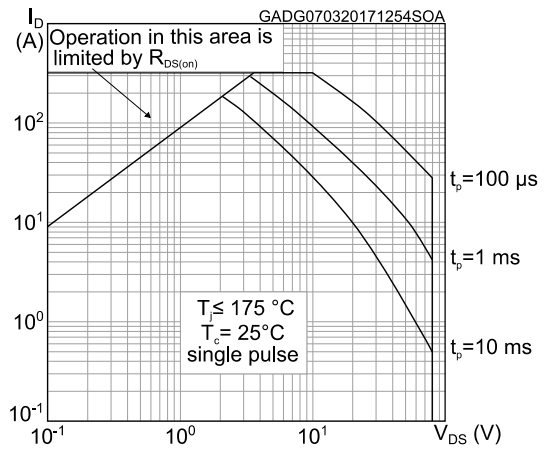


Figure 3: Normalized thermal impedance

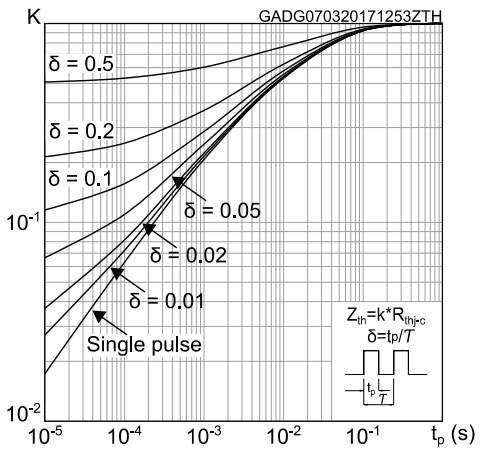


Figure 4: Output characteristics

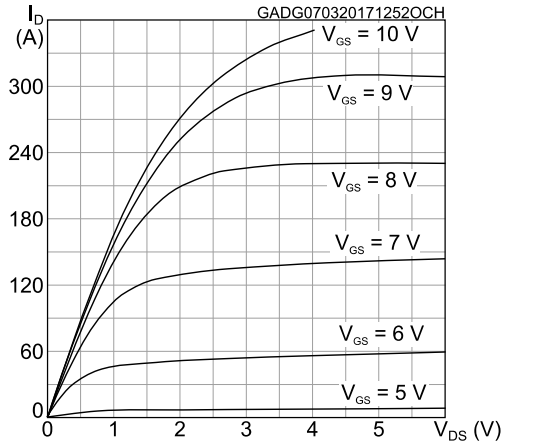


Figure 5: Transfer characteristics

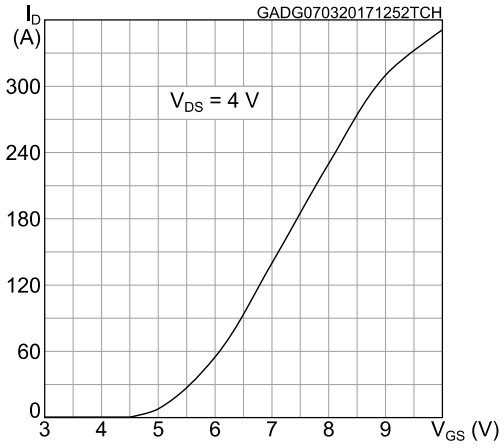


Figure 6: Capacitance variations

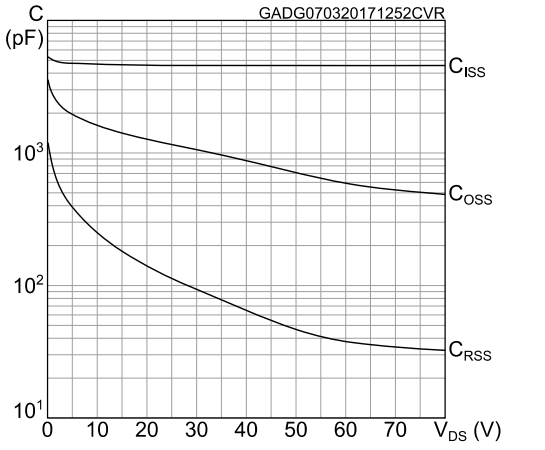


Figure 7: Gate charge vs. gate-source voltage

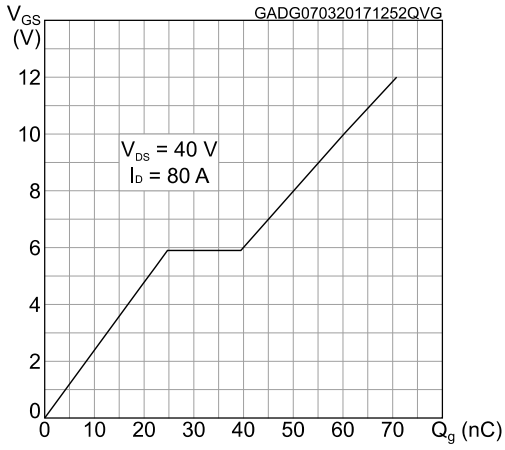


Figure 8: Static drain-source on-resistance

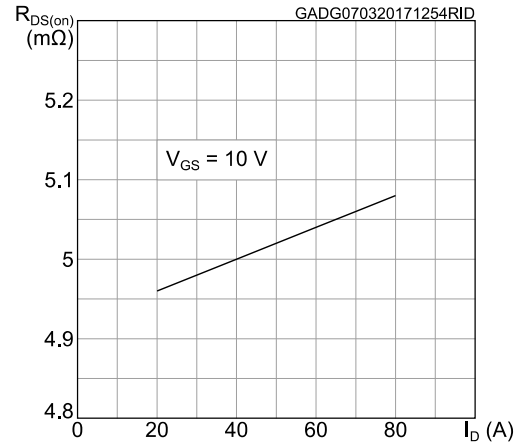


Figure 9: Source-drain diode forward characteristics

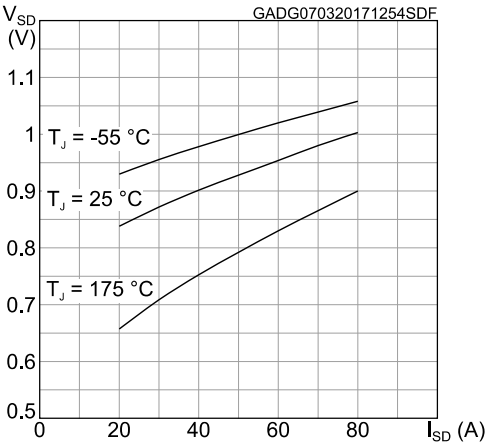


Figure 10: Normalized gate threshold voltage vs. temperature

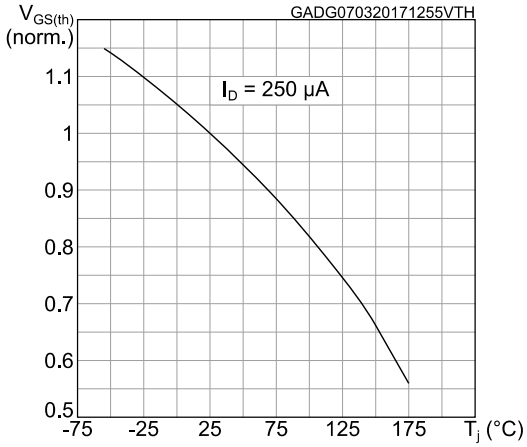


Figure 11: Normalized on-resistance vs temperature

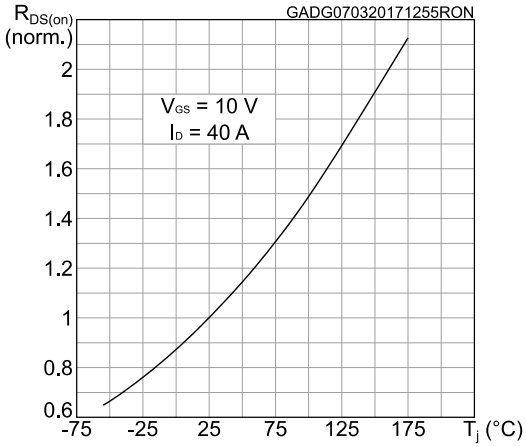
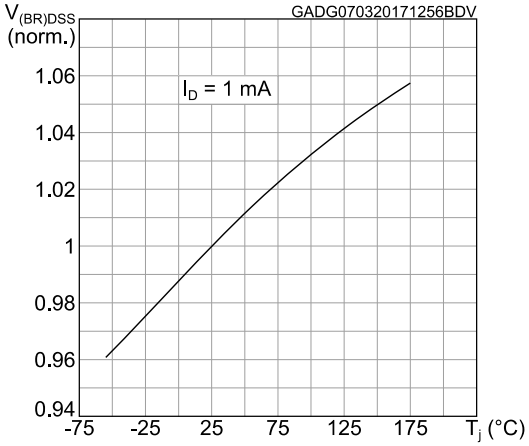


Figure 12: Normalized $V_{(BR)DSS}$ vs. temperature



3 Test circuits

Figure 13: Test circuit for resistive load switching times

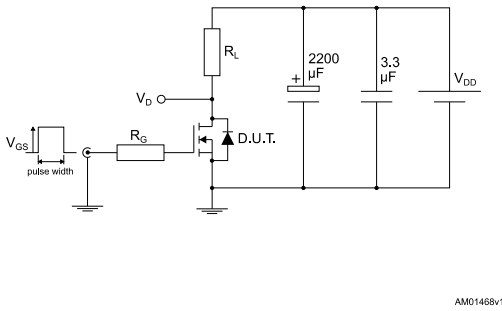


Figure 14: Test circuit for gate charge behavior

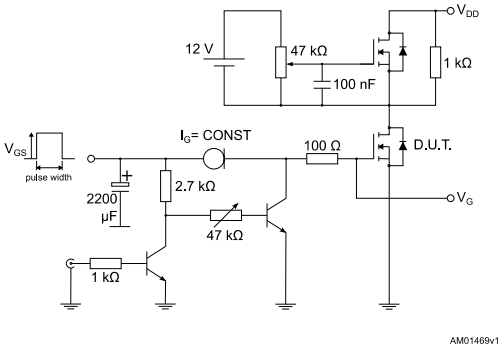


Figure 15: Test circuit for inductive load switching and diode recovery times

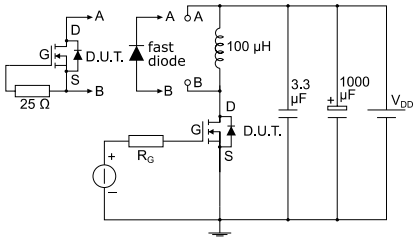


Figure 16: Unclamped inductive load test circuit

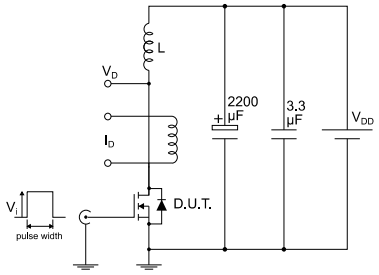


Figure 17: Unclamped inductive waveform

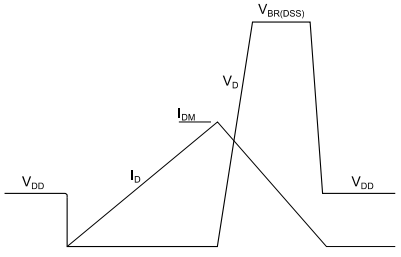
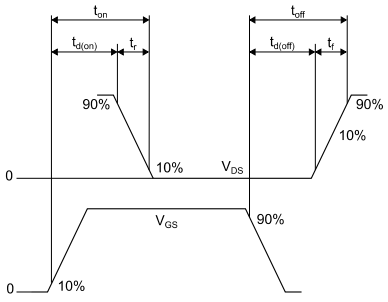


Figure 18: Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

4.1 TO-220 package information

Figure 19: TO-220 type A package outline

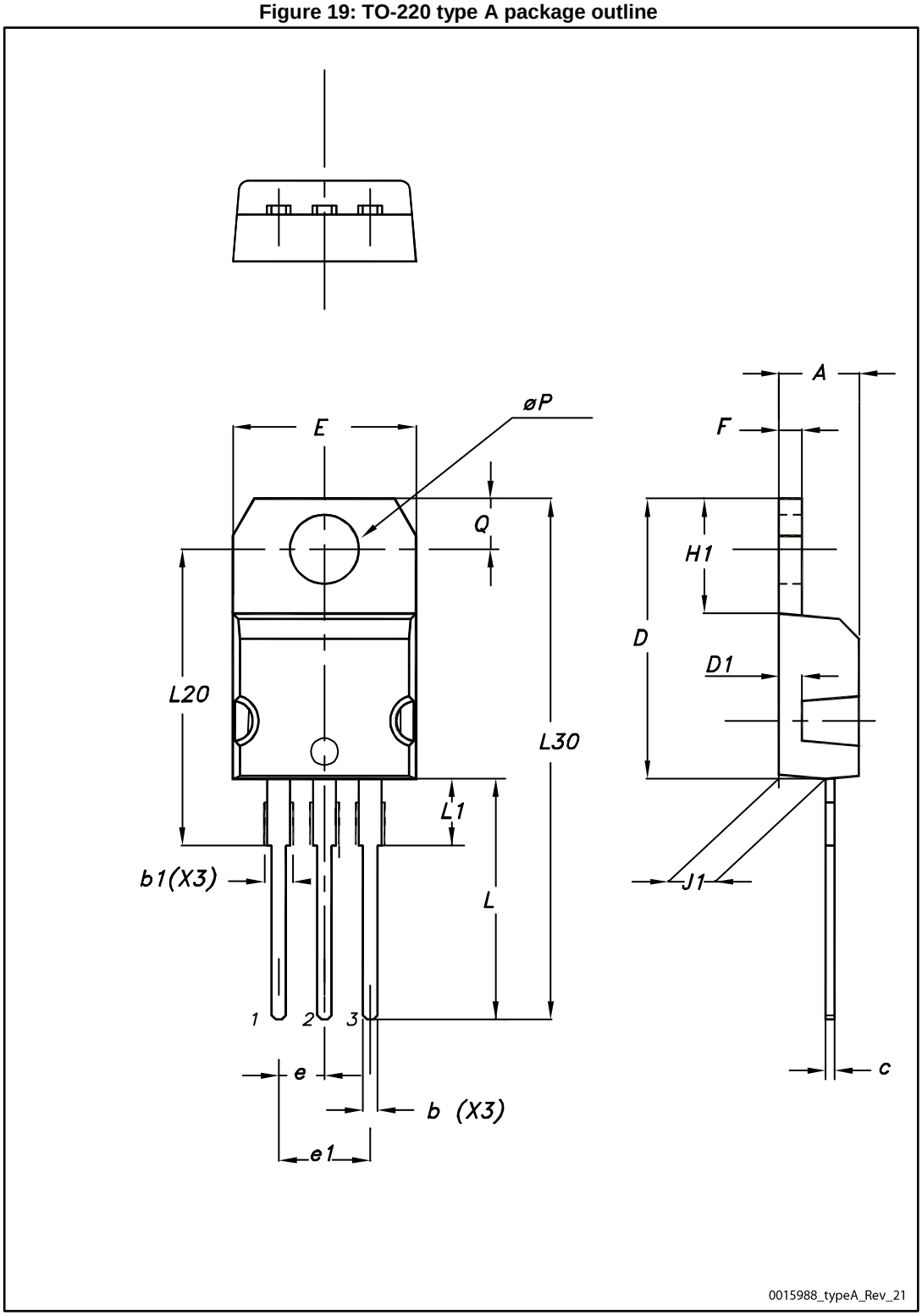


Table 8: TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.55
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10.00		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13.00		14.00
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95

5 Revision history

Table 9: Document revision history

Date	Revision	Changes
04-Dec-2014	1	First release
09-Mar-2017	2	Datasheet status promoted from preliminary to production data. Updated *Section 1: "Electrical ratings"* and *Section 2: "Electrical characteristics"*. Minor text changes

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