STP130NH02L

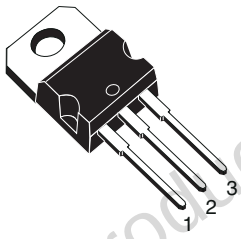
N-channel 24V - 0.0034Ω - 120A - TO-220
STripFET™ Power MOSFET for DC-DC conversion

Features

Type	V_{DSS}	$R_{DS(on)}$	I_D
STP130NH02L	24V	<0.0044Ω	90(1)

1. Value limited by wire bonding

- $R_{DS(on)}$ *Qg industry's benchmark Low
- Conduction losses reduced
- Switching losses reduced
- Low Threshold device

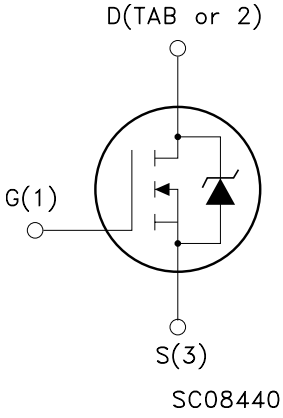


TO-220

Description

These devices utilizes the latest advanced design rules of ST's proprietary STripFET™ technology. It is ideal in high performance DC-DC converter applications where efficiency is to be achieved at very high output currents.

Internal schematic diagram



Application

- Switching application

Order code

Part number	Marking	Package	Packaging
STP130NH02L	P130NH02L	TO-220	Tube

Contents

1 Electrical ratings

Table 1.

Symbol	Parameter	Value	Unit
V_{spike} (1)	Drain-source voltage rating	30	V
V_{DS}	Drain-source voltage (V_{GS} = 0)	24	V
V_{DGR}	Drain-gate voltage (R_{GS} = 20 kΩ)	24	V
V_{GS}	Gate- source voltage	± 20	V
I_D (2)	Drain current (continuous) at T_C = 25°C	90	A
I_D (2)	Drain current (continuous) at T_C = 100°C	90	A
I_{DM} (3)	Drain current (pulsed)	360	A
P_{tot}	Total dissipation at T_C = 25°C	150	W
	Derating factor	1	W/°C
E_{AS} (4)	Single pulse avalanche energy	900	mJ
T_{stg}	Storage temperature	-55 to 175	°C
T_j	Max. operating junction temperature		

1. Guaranteed when external Rg=4.7 Ω and $t_f < t_{fmax}$
2. Value limited by wire bonding
3. Pulse width limited by safe operating area
4. Starting T_J = 25°C, I_D = 45A, V_{DD} = 10V

Table 2. Thermal data

Rthj-case	Thermal resistance junction-case max	1.0	°C/W
Rthj-amb	Thermal resistance junction-ambient max	62.5	°C/W
T_l	Maximum lead temperature for soldering purpose	300	°C

2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Table 3. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 25mA V_{GS}= 0	24			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max rating, V_{DS} = Max rating, T_C=125°C			1 10	µA µA
I_{GSS}	Gate body leakage current (V_{DS} = 0)	V_{GS} = ±20V			±100	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250µA	1			V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10V , I_D = 45A V_{GS} = 5V, I_D = 22.5A		0.0034 0.005	0.0044 0.008	Ω Ω

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward transconductance	V_{DS} = 10V, I_D = 45A		55		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 15V, f = 1MHz, V_{GS} = 0		4450 1126 141		pF pF pF
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on delay time Rise time Off voltage rise time Fall time	V_{DD} = 10V, I_D = 45A, R_G = 4.7Ω, V_{GS} = 10V (see *Figure 13*)		14 224 69 40		ns ns ns ns
Rg	Gate input resistance	f = 1MHz gate DC bias=0 test signal level=20mV open drain		1.6		Ω
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD}=10V, I_D = 90A V_{GS} =10V (see *Figure 14*)		69 13 9	93	nC nC nC
Q_{oss} (2)	Output charge	V_{DS} = 16V, V_{GS} = 0		27		ns
Q_{gls} (3)	Third-quadrant gate charge	V_{DS} < 0, V_{GS}= 10V		64		ns

1. Pulsed: pulse duration = 300µs, duty cycle 1.5%
2. Qoss = Coss* ΔV_{IN}, Coss = Cgd + Cds. See power losses calculation
3. Gate charge for synchronous operation.

Table 5. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM}	Source-drain current Source-drain current (pulsed)				90 360	A A
V_{SD} (1)	Forward on voltage	I_{SD} = 45A, V_{GS} = 0			1.3	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 90A, di/dt = 100A/µs, V_{DD} = 15V, T_J =150°C		47 58 2.5		ns nC A

1. Pulsed: pulse duration = 300µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

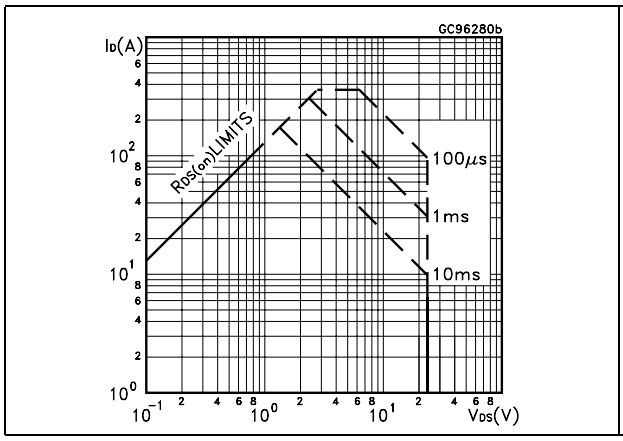


Figure 2. Thermal impedance

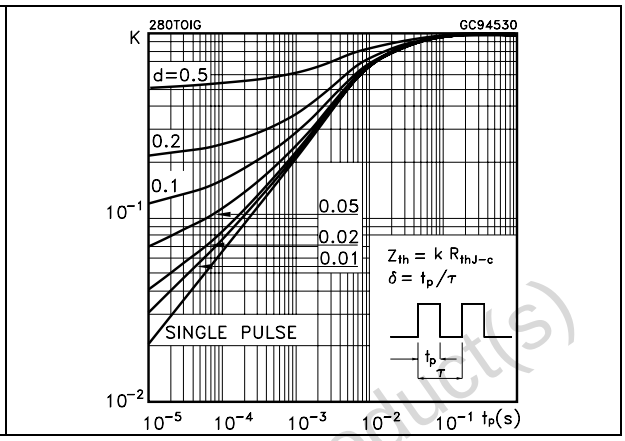


Figure 3. Output characteristics

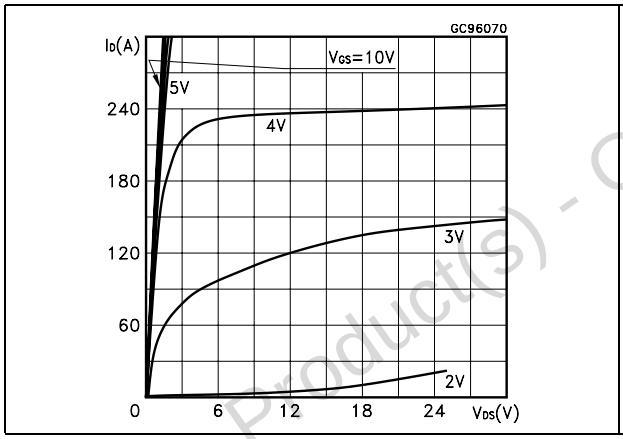


Figure 4. Transfer characteristics

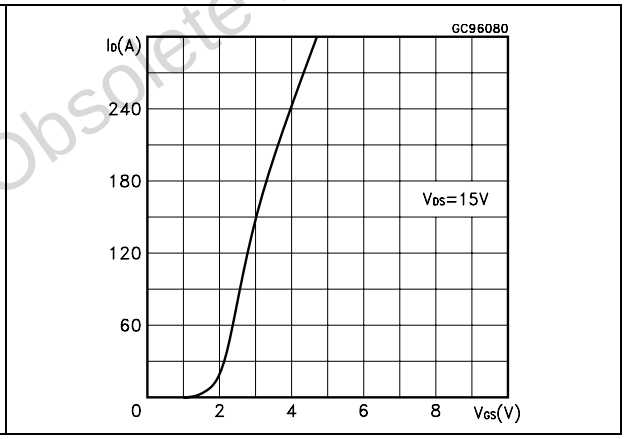


Figure 5. Transconductance

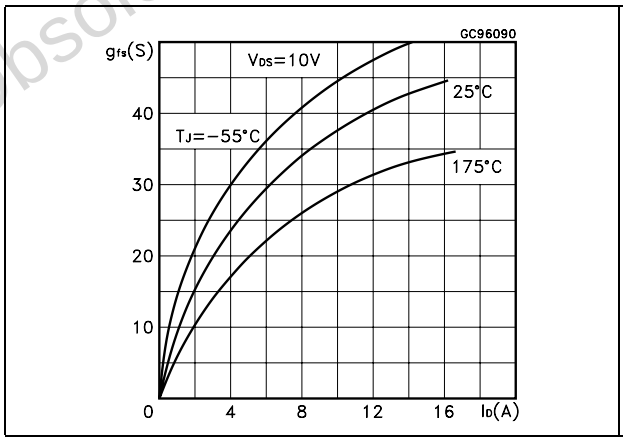


Figure 6. Static drain-source on resistance

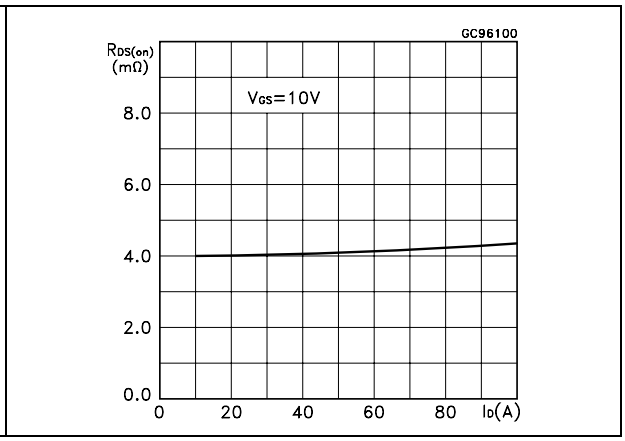


Figure 7. Gate charge vs gate-source voltage

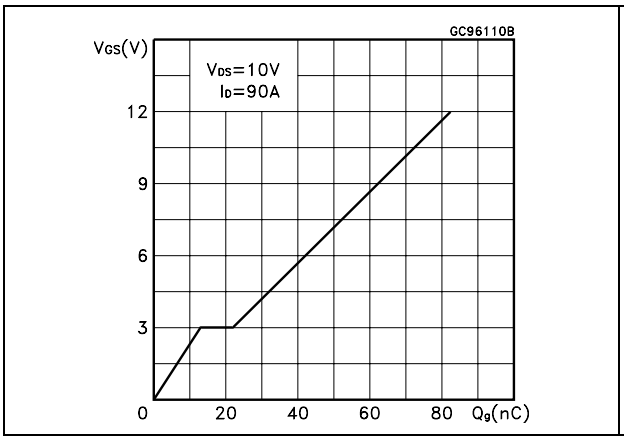


Figure 8. Capacitance variations

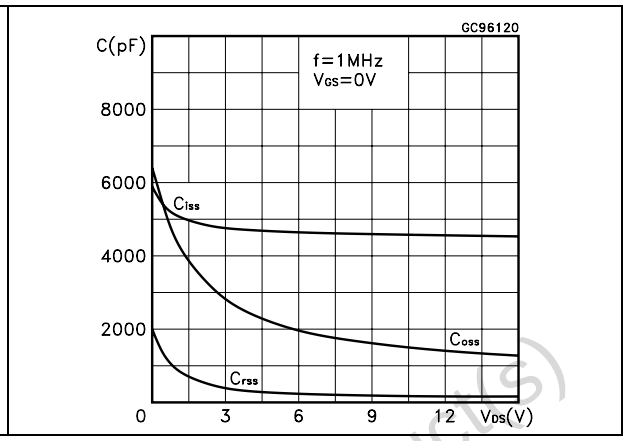


Figure 9. Normalized gate threshold voltage vs temperature

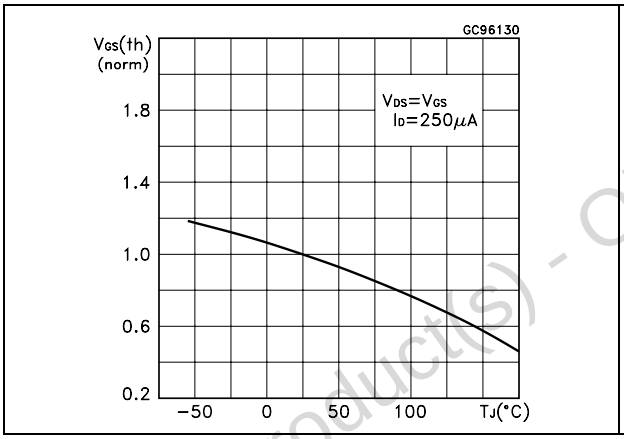


Figure 10. Normalized on resistance vs temperature

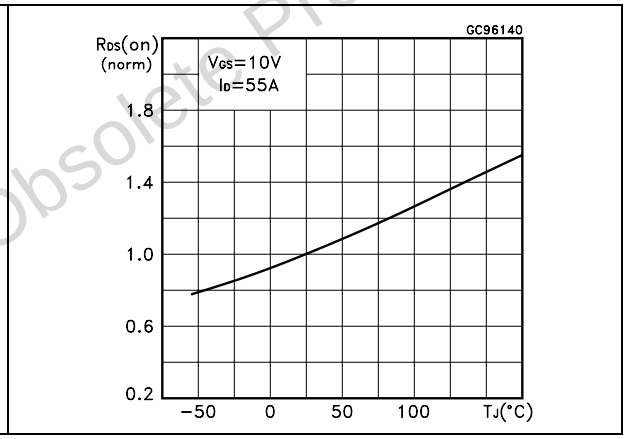


Figure 11. Source-drain diode forward characteristics

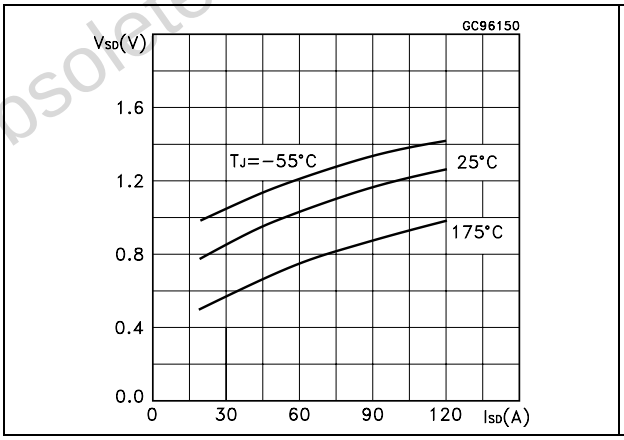
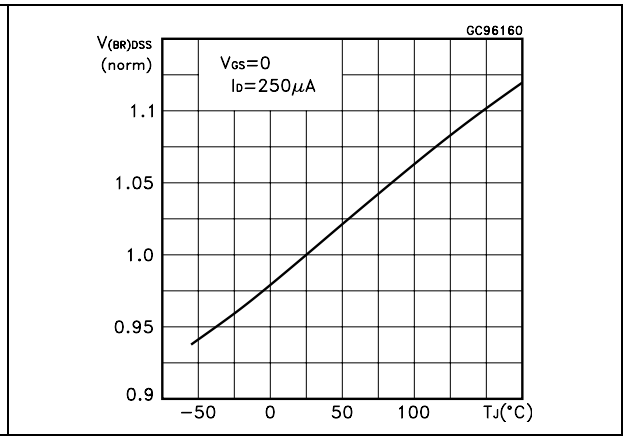


Figure 12. Normalized B_{VDSS} vs temperature



3 Test circuit

Figure 13. Switching times test circuit for resistive load

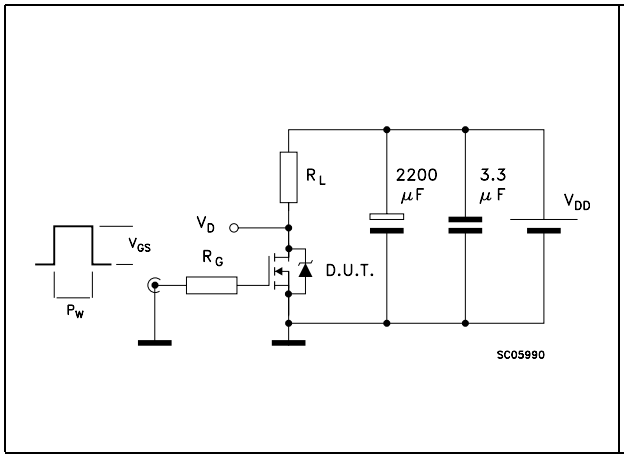


Figure 14. Gate charge test circuit

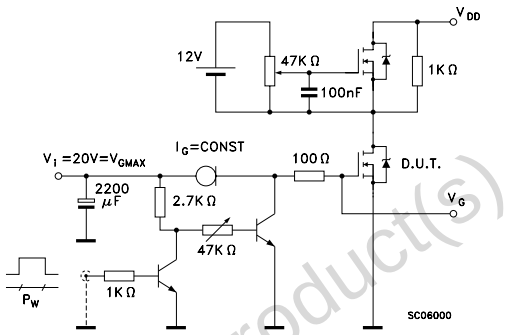


Figure 15. Test circuit for inductive load switching and diode recovery times

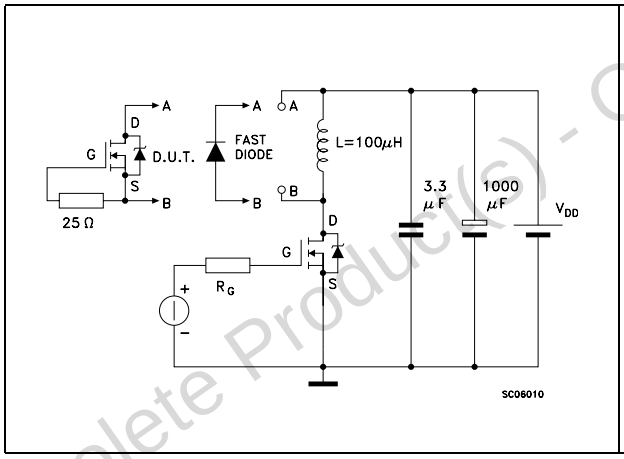


Figure 16. Unclamped Inductive load test circuit

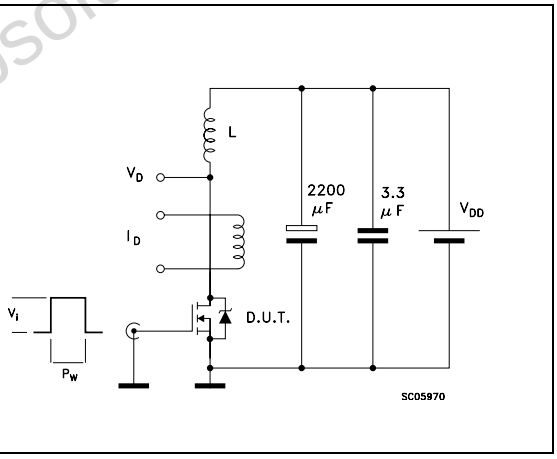


Figure 17. Unclamped inductive waveform

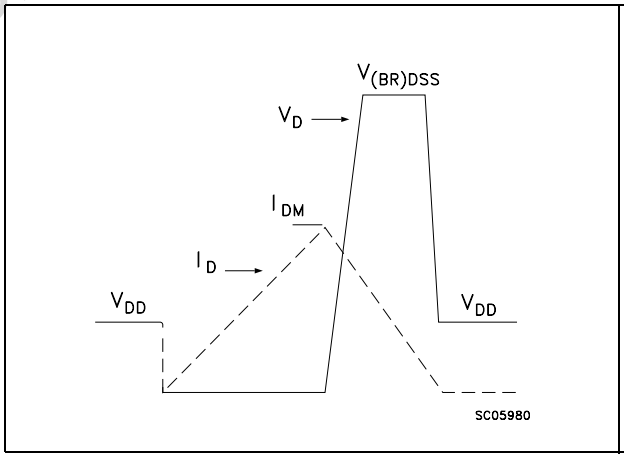
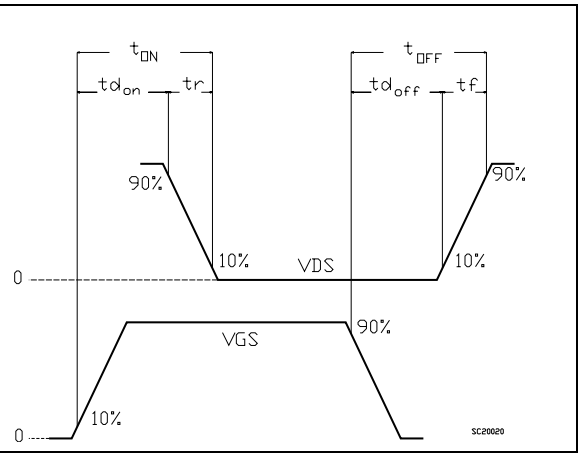


Figure 18. Switching time waveform

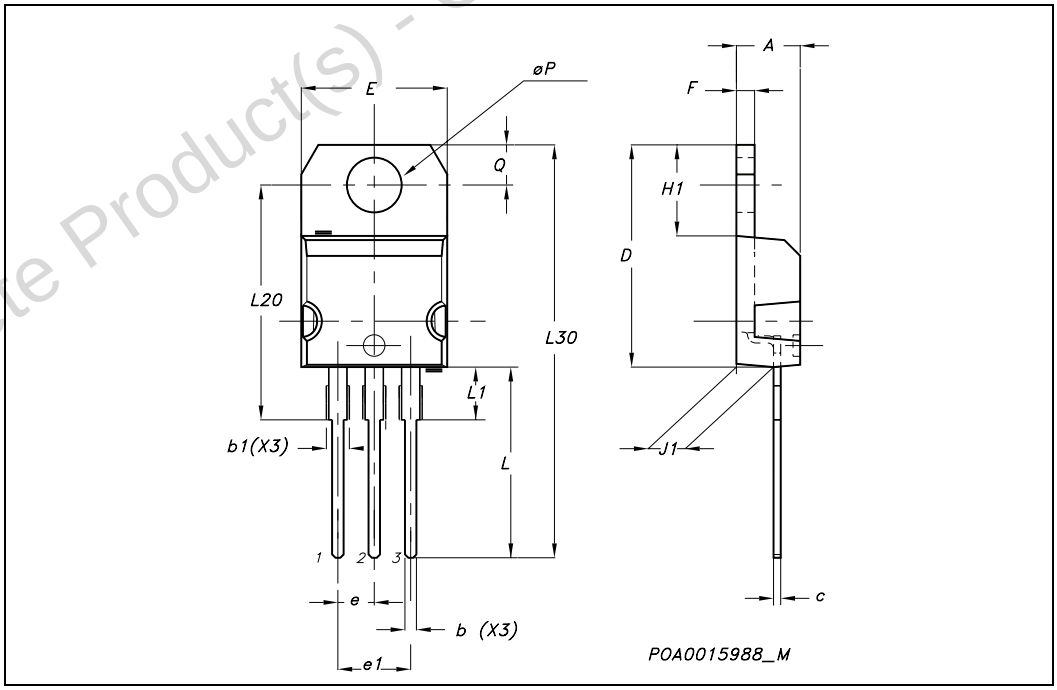


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

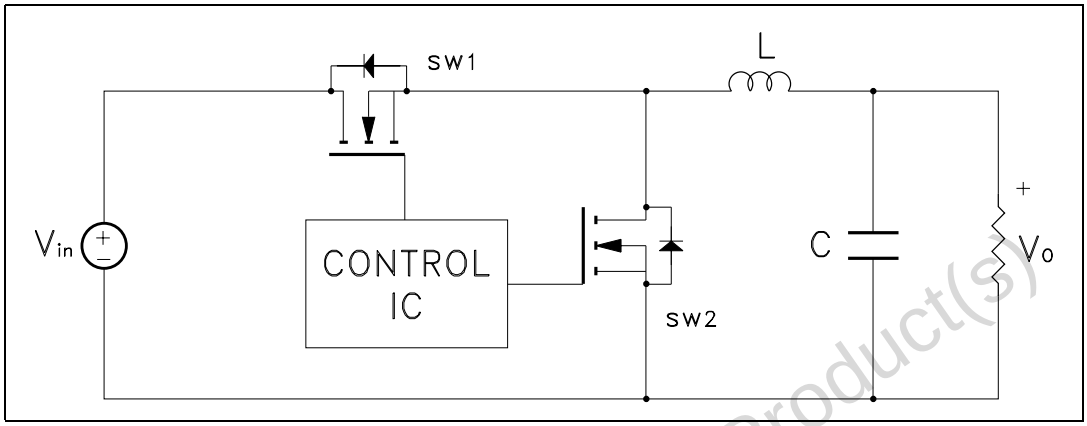
TO-220 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.15		1.70	0.045		0.066
c	0.49		0.70	0.019		0.027
D	15.25		15.75	0.60		0.620
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.052
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
øP	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116



5 Appendix A

Figure 19. Buck converter: power losses estimation



The power losses associated with the FETs in a synchronous buck converter can be estimated using the equations shown in the table below. The formulas give a good approximation, for the sake of performance comparison, of how different pairs of devices affect the converter efficiency. However a very important parameter, the working temperature, is not considered. The real device behavior is really dependent on how the heat generated inside the devices is removed to allow for a safer working junction temperature.

- The low side (SW2) device requires:
- Very low $R_{DS(on)}$ to reduce conduction losses
- Small Qgls to reduce the gate charge losses
- Small Coss to reduce losses due to output capacitance
- Small Qrr to reduce losses on SW1 during its turn-on
- The Cgd/Cgs ratio lower than Vth/Vgg ratio especially with low drain to source
- voltage to avoid the cross conduction phenomenon;
- The high side (SW1) device requires:
- Small Rg and Ls to allow higher gate current peak and to limit the voltage feedback on the gate
- Small Qg to have a faster commutation and to reduce gate charge losses
- Low $R_{DS(on)}$ to reduce the conduction losses.

Table 6. Power losses calculation

		High side switching (SW1)	Low side switch (SW2)
Pconduction		$R_{DS(on)SW1} * I_L^2 * \delta$	$R_{DS(on)SW2} * I_L^2 * (1-\delta)$
Pswitching		$V_{in} * (Q_{gsth(SW1)} + Q_{gd(SW1)}) * f * \frac{I_L}{I_g}$	Zero Voltage Switching
Pdiode	Recovery (1)	Not applicable	$V_{in} * Q_{rr(SW2)} * f$
	Conduction	Not applicable	$V_{f(SW2)} * I_L * t_{deadtime} * f$
Pgate(Q_G)		$Q_{g(SW1)} * V_{gg} * f$	$Q_{gls(SW2)} * V_{gg} * f$
P_{Qoss}		$\frac{V_{in} * Q_{oss(SW1)} * f}{2}$	$\frac{V_{in} * Q_{oss(SW2)} * f}{2}$

1. Dissipated by SW1 during turn-on

Table 7. Parameters meaning

Parameter	Meaning
d	Duty-cycle
Q_{gsth}	Post threshold gate charge
Q_{gls}	Third quadrant gate charge
Pconduction	On state losses
Pswitching	On-off transition losses
Pdiode	Conduction and reverse recovery diode losses
Pgate	Gate drive losses
P_{Qoss}	Output capacitance losses

6 Revision history

Table 8. Revision history

Date	Revision	Changes
14-Mar-2005	4	Preliminary document
24-Mar-2005	5	New package inserted (TO-220)
19-Jun-2006	6	New template, no content change
13-Apr-2007	7	Package removed (D^2PAK)

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