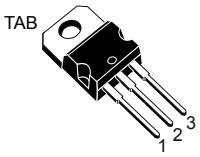
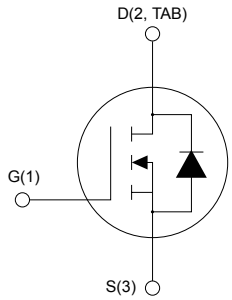
STP18N55M5

Datasheet

N-channel 550 V, 150 mΩ typ., 16 A MDmesh M5 Power MOSFET in a TO-220 package



TO-220



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Features

Order code	V_{DS} at T_J max.	$R_{DS(on)}$ max.	I_D
STP18N55M5	600 V	192 mΩ	16 A

- Extremely low $R_{DS(on)}$
- Low gate charge and input capacitance
- Excellent switching performance
- 100% avalanche tested

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET based on the MDmesh M5 innovative vertical process technology combined with the well-known PowerMESH horizontal layout. The resulting product offers extremely low on-resistance, making it particularly suitable for applications requiring high power and superior efficiency.

Product status link
STP18N55M5

Product summary	
Order code	STP18N55M5
Marking	18N55M5
Package	TO-220
Packing	Tube

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	±25	V
I_D	Drain current (continuous) at T_C = 25 °C	16	A
	Drain current (continuous) at T_C = 100 °C	10	
I_{DM}(1)	Drain current (pulsed)	64	A
P_{TOT}	Total power dissipation at T_C = 25 °C	110	W
dv/dt(2)	Peak diode recovery voltage slope	15	V/ns
T_{stg}	Storage temperature range	-55 to 150	°C
T_J	Operating junction temperature range		°C

1. *Pulse width is limited by safe operating area.*
2. *I_{SD} ≤ 16 A, di/dt ≤ 400 A/µs, V_{DS} (peak) < $V_{(BR)DSS}$, V_{DD} = 340 V.*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	1.14	°C/W
R_{thJA}	Thermal resistance, junction-to-ambient	62.5	°C/W

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or non-repetitive (pulse width limited by T_J max.)	4	A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	210	mJ

2 Electrical characteristics

T_C = 25 °C unless otherwise specified.

Table 4. On/off states

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0 V	550			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 550 V			1	µA
		V_{GS} = 0 V, V_{DS} = 550 V, T_C = 125 °C(1)			100	
I_{GSS}	Gate body leakage current	V_{DS} = 0 V, V_{GS} = ±25 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10 V, I_D = 8 A		150	192	mΩ

1. *Specified by design, not tested in production.*

Table 5. Dynamic

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0 V	-	1260	-	pF
C_{oss}	Output capacitance		-	42	-	pF
C_{rss}	Reverse transfer capacitance		-	3.6	-	pF
$C_{o(tr)}$ (1)	Equivalent capacitance time related	V_{DS} = 0 to 440 V, V_{GS} = 0 V	-	103	-	pF
$C_{o(er)}$(2)	Equivalent capacitance energy related		-	35	-	pF
Rg	Gate input resistance	f = 1 MHz open drain	-	2.8	-	Ω
Q_g	Total gate charge	V_{DD} = 440 V, I_D = 8 A, V_{GS} = 0 to 10 V (see Figure 15. Test circuit for gate charge behavior)	-	31	-	nC
Q_{gs}	Gate-source charge		-	8.3	-	nC
Q_{gd}	Gate-drain charge		-	14.2	-	nC

1. *Time related is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.*
2. *Energy related is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.*

Table 6. Switching times

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$t_{d(v)}$	Voltage delay time	V_{DD} = 400 V, I_D = 10.5 A, R_G = 4.7 Ω, V_{GS} = 10 V (see Figure 16. Test circuit for inductive load switching and diode recovery times and Figure 19. Switching time waveform)	-	37	-	ns
$t_{r(v)}$	Voltage rise time		-	7	-	ns
$t_{c(off)}$	Crossing time		-	10.3	-	ns
$t_{f(i)}$	Current fall time		-	8.3	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		16	A
I_{SDM}(1)	Source-drain current (pulsed)		-		64	A
V_{SD}(2)	Forward on voltage	I_{SD} = 16 A, V_{GS} = 0 V	-		1.5	V
t_{rr}	Reverse recovery time	I_{SD} = 16 A, di/dt = 100 A/µs, V_{DD} = 100 V (see Figure 16. Test circuit for inductive load switching and diode recovery times)	-	244		ns
Q_{rr}	Reverse recovery charge		-	2.8		µC
I_{RRM}	Reverse recovery current		-	23		A
t_{rr}	Reverse recovery time	I_{SD} = 16 A, di/dt = 100 A/µs, V_{DD} = 100 V, T_J = 150 °C (see Figure 16. Test circuit for inductive load switching and diode recovery times)	-	295		ns
Q_{rr}	Reverse recovery charge		-	3.7		µC
I_{RRM}	Reverse recovery current		-	25		A

1. *Pulse width limited by safe operating area.*
2. *Pulsed: pulse duration = 300 µs, duty cycle 1.5%.*

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

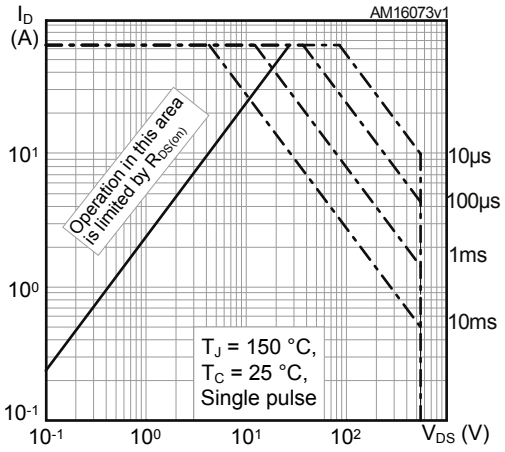


Figure 2. Thermal impedance

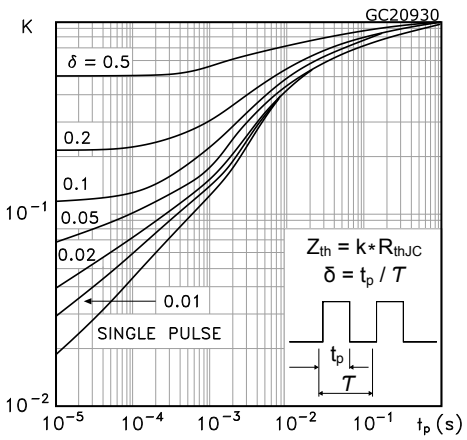


Figure 3. Output characterisics

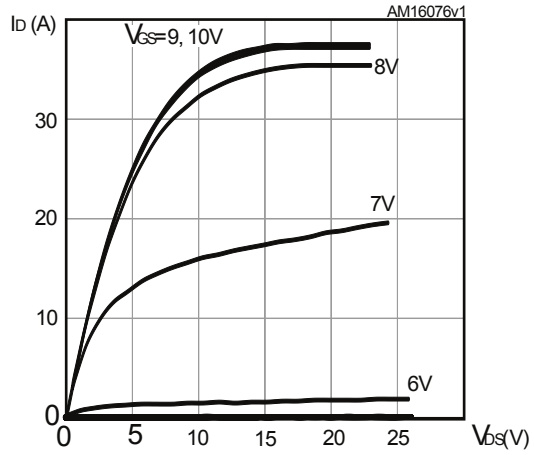


Figure 4. Transfer characteristics

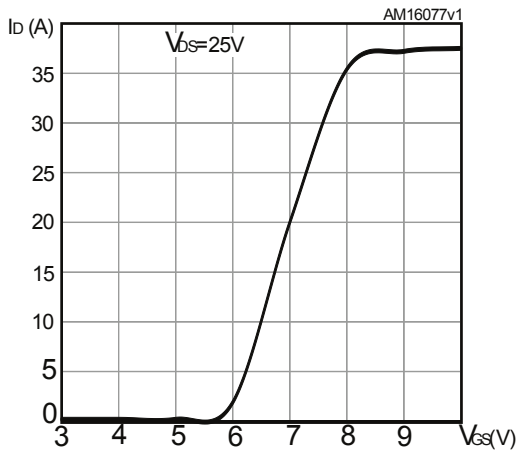


Figure 5. Gate charge vs gate-source voltage

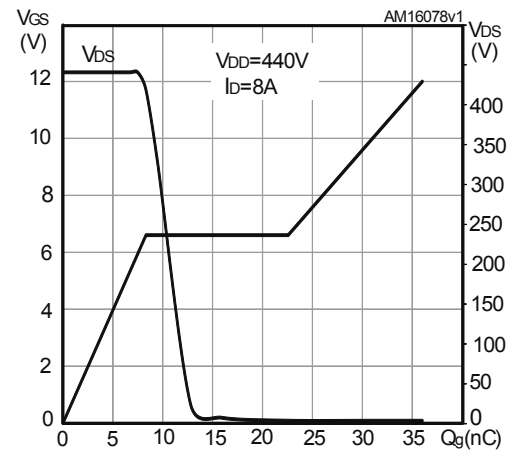


Figure 6. Static drain-source on resistance

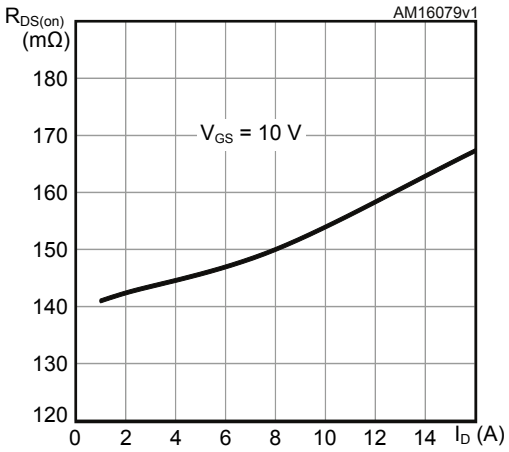


Figure 7. Capacitance variations

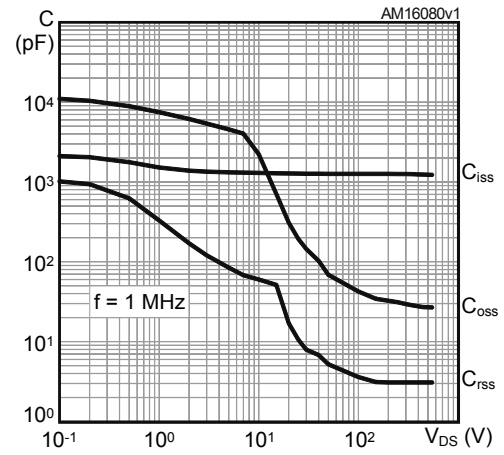


Figure 8. Output capacitance stored energy

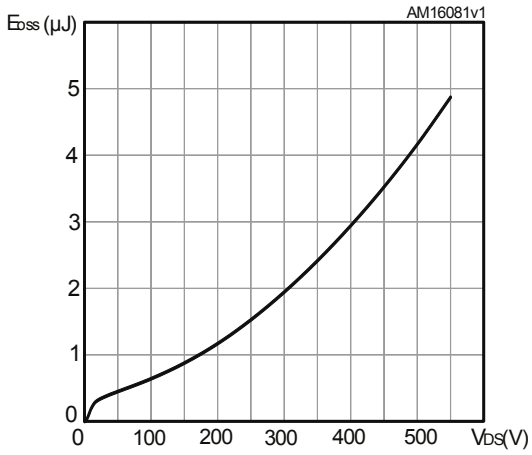


Figure 9. Normalized gate threshold voltage vs temperature

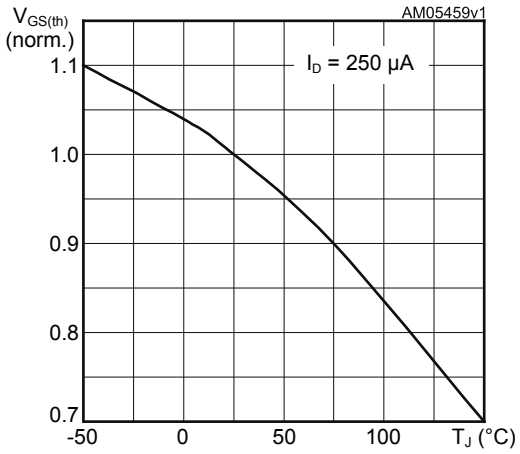


Figure 10. Normalized on-resistance vs temperature

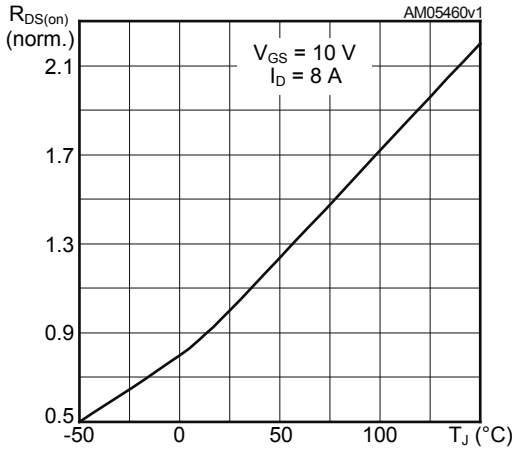


Figure 11. Drain-source diode forward characteristics

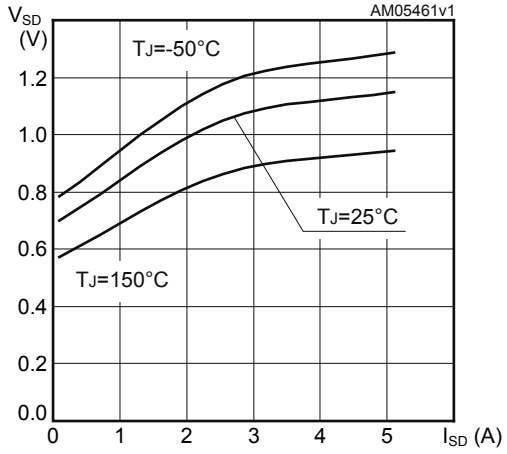


Figure 12. Normalized $V_{(BR)DSS}$ vs temperature

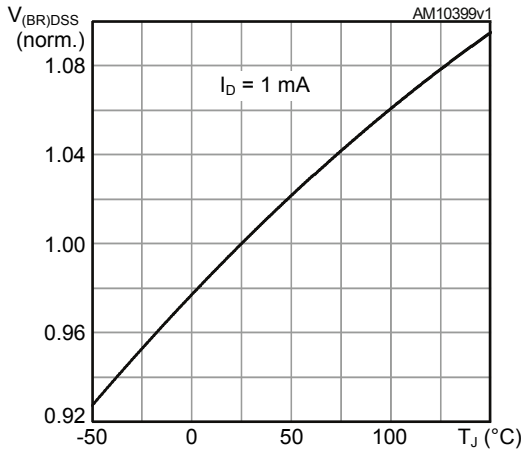
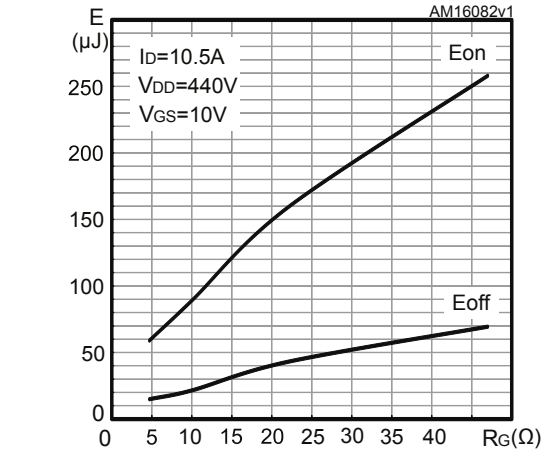


Figure 13. Switching energy vs gate resistance



* Eon including reverse recovery of a SiC diode

3 Test circuits

Figure 14. Test circuit for resistive load switching times

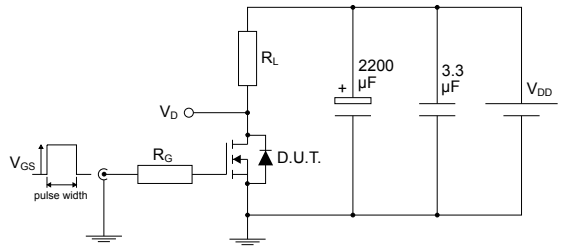


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Figure 15. Test circuit for gate charge behavior

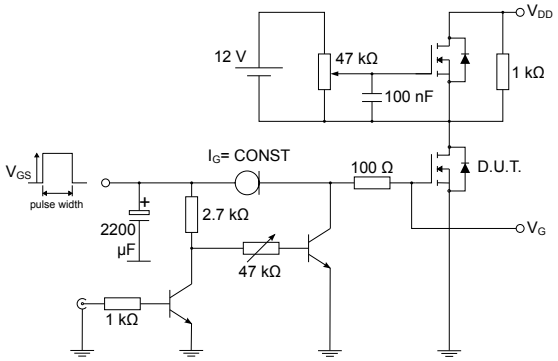

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Figure 16. Test circuit for inductive load switching and diode recovery times

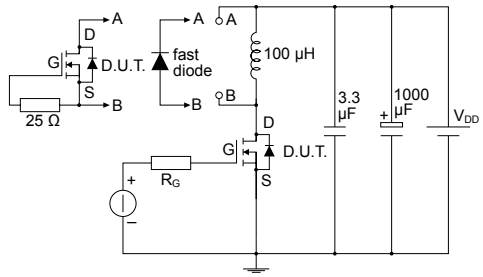

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Figure 17. Unclamped inductive load test circuit

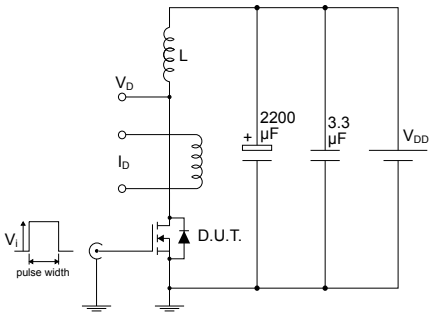

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Figure 18. Unclamped inductive waveform

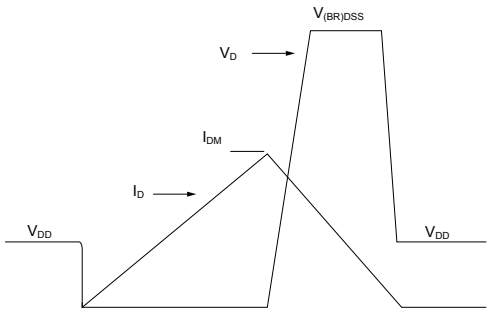

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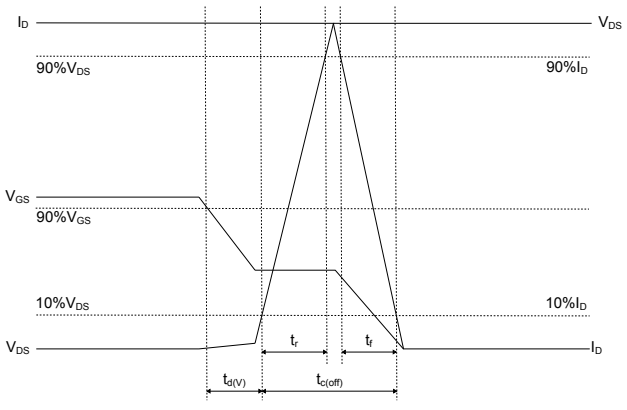
Figure 19. Switching time waveform



AM05540v2

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 TO-220 type A package information

Figure 20. TO-220 type A package outline

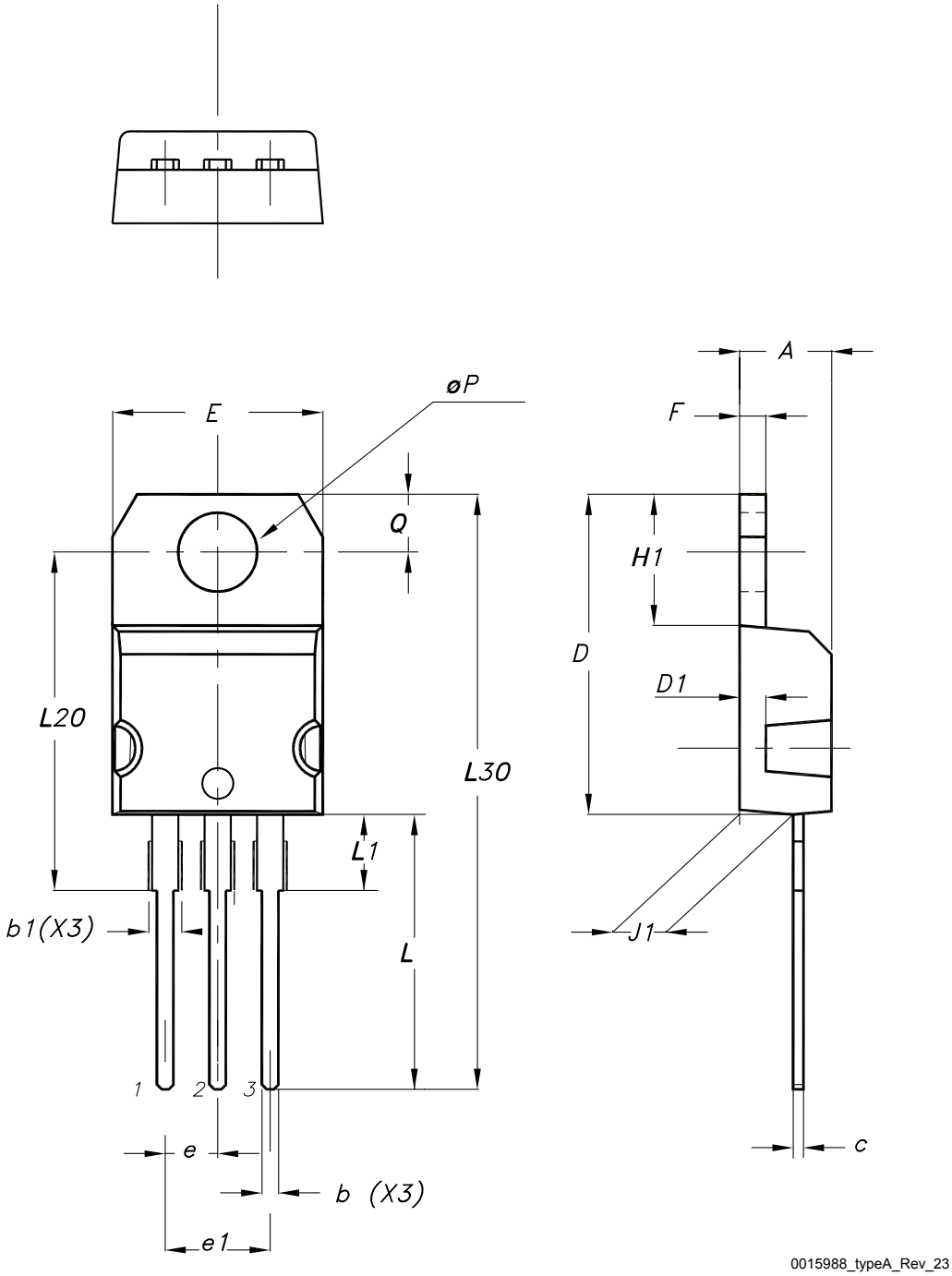


Table 8. **TO-220 type A package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.55
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10.00		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13.00		14.00
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95
Slug flatness		0.03	0.10

Revision history

Table 9. **Document revision history**

Date	Revision	Changes
31-Aug-2023	1	First release. The part number STP18N55M5 was previously inserted in the DS6705.

Contents