



STP190NF04

STB190NF04 STB190NF04-1

N-CHANNEL 40V - 3.9 mΩ - 120A D²PAK/I²PAK/TO-220

STripFET™ II POWER MOSFET

PRELIMINARY DATA

TYPE	V _{DSS}	R _{DS(on)}	I _D
STB190NF04/-1	40 V	<0.0043 Ω	120 A
STP190NF04	40 V	<0.0043 Ω	120 A

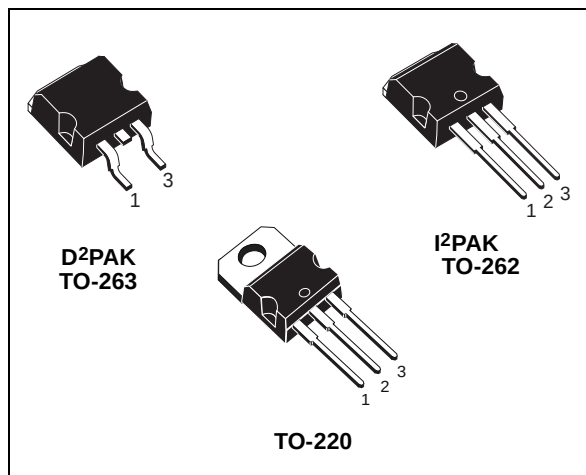
- TYPICAL R_{DS(on)} = 3.9 mΩ
- STANDARD THRESHOLD DRIVE
- 100% AVALANCHE TESTED

DESCRIPTION

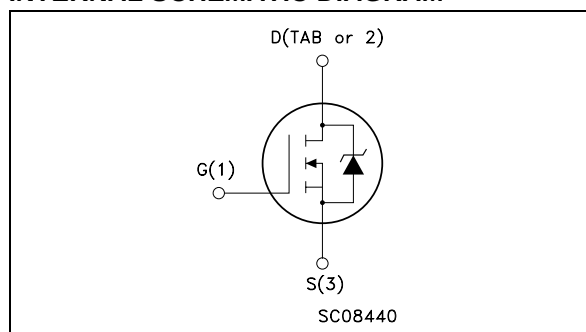
This Power MOSFET is the latest development of STMicroelectronics unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

APPLICATIONS

- HIGH CURRENT, HIGH SWITCHING SPEED
- AUTOMOTIVE



INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source Voltage (V _{GS} = 0)	40	V
V _{DGR}	Drain-gate Voltage (R _{GS} = 20 kΩ)	40	V
V _{GS}	Gate- source Voltage	± 20	V
I _D (●)	Drain Current (continuous) at T _C = 25°C	120	A
I _D	Drain Current (continuous) at T _C = 100°C	120	A
I _{DM} (●●)	Drain Current (pulsed)	480	A
P _{tot}	Total Dissipation at T _C = 25°C	310	W
	Derating Factor	2.07	W/°C
dv/dt (1)	Peak Diode Recovery voltage slope	7	V/ns
E _{AS} (1)	Single Pulse Avalanche Energy	860	mJ
T _{stg}	Storage Temperature	-55 to 175	°C
T _j	Max. Operating Junction Temperature		

(●) Current limited by package

(●●) Pulse width limited by safe operating area.

1) I_{SD} ≤ 190A, di/dt ≤ 600A/μs, V_{DD} ≤ V(BR)DSS, T_j ≤ T_{JMAX}

STB190NF04/-1 STP190NF04**THERMAL DATA**

R _{thj-case}	Thermal Resistance Junction-case	Max	0.48	°C/W
R _{thj-amb}	Thermal Resistance Junction-ambient	Max	50	°C/W
T _I	Maximum Lead Temperature For Soldering Purpose	Typ	300	°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25 °C unless otherwise specified)**OFF**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source Breakdown Voltage	I _D = 250 µA V _{GS} = 0	40			V
I _{DSS}	Zero Gate Voltage Drain Current (V _{GS} = 0)	V _{DS} = Max Rating V _{DS} = Max Rating T _C = 125°C			1 10	µA µA
I _{GSS}	Gate-body Leakage Current (V _{DS} = 0)	V _{GS} = ± 20V			±100	nA

ON (*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} I _D = 250 µA	2		4	V
R _{DS(on)}	Static Drain-source On Resistance	V _{GS} = 10 V I _D = 95A		0.0039	0.0043	Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g _{fs} (*)	Forward Transconductance	V _{DS} = 15 V I _D = 95 A		200		S
C _{iss} C _{oss} C _{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V _{DS} = 25V, f = 1 MHz, V _{GS} = 0		5800 1500 200		pF pF pF

ELECTRICAL CHARACTERISTICS (continued)**SWITCHING ON**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on Delay Time Rise Time	$V_{DD} = 20\text{ V}$ $I_D = 95\text{ A}$ $R_G = 4.7\ \Omega$ $V_{GS} = 10\text{ V}$ (Resistive Load, Figure 3)		45 380		ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	$V_{DD}=20\text{V}$ $I_D=190\text{ A}$ $V_{GS}=10\text{V}$		130 40 45		nC nC nC

SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$ t_f	Turn-off Delay Time Fall Time	$V_{DD} = 20\text{ V}$ $I_D = 95\text{ A}$ $R_G = 4.7\ \Omega$, $V_{GS} = 10\text{ V}$ (Resistive Load, Figure 3)		100 75		ns ns

SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} $I_{SDM}^{(*)}$	Source-drain Current Source-drain Current (pulsed)				120 480	A A
$V_{SD}^{(*)}$	Forward On Voltage	$I_{SD} = 120\text{ A}$ $V_{GS} = 0$			1.3	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 190\text{ A}$ $di/dt = 100\text{A}/\mu\text{s}$ $V_{DD} = 34\text{ V}$ $T_j = 150^\circ\text{C}$ (see test circuit, Figure 5)		90 295 6.5		ns nC A

(*) Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %.

(*) Pulse width limited by safe operating area.

Fig. 1: Unclamped Inductive Load Test Circuit

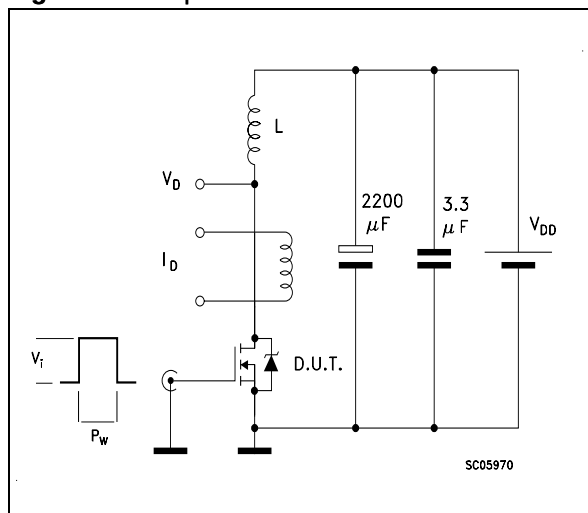


Fig. 2: Unclamped Inductive Waveform

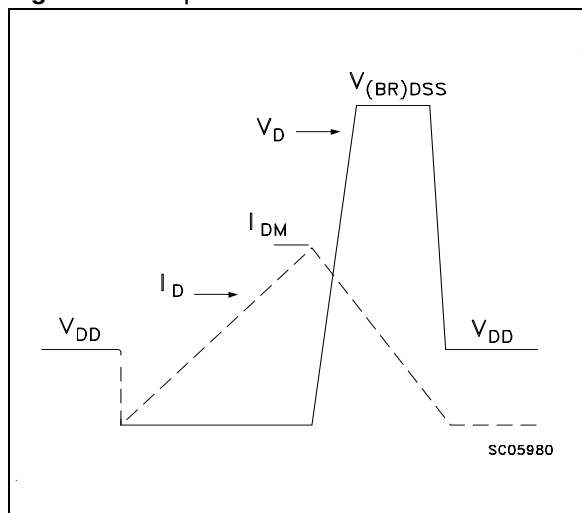


Fig. 3: Switching Times Test Circuits For Resistive Load

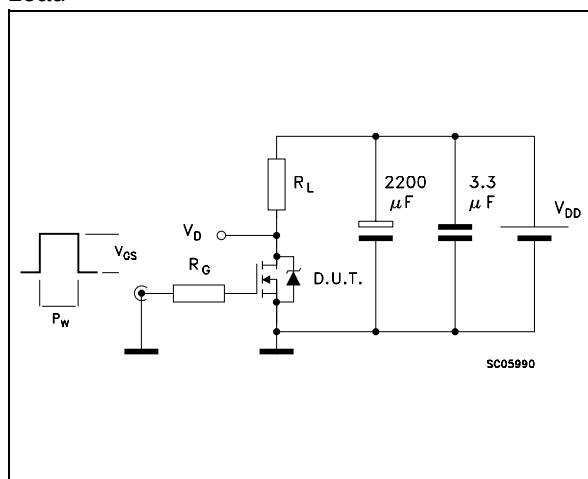


Fig. 4: Gate Charge test Circuit

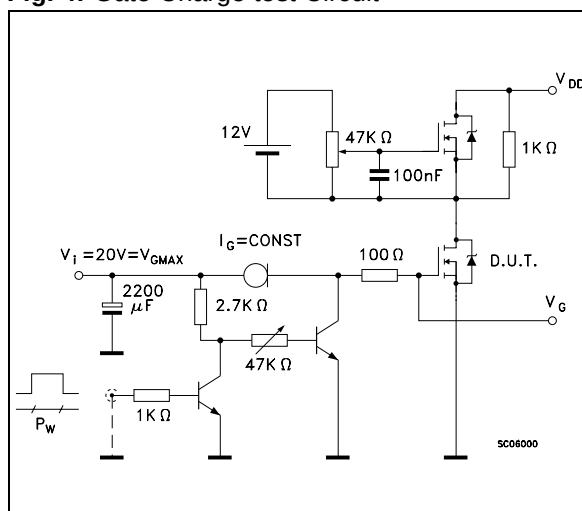
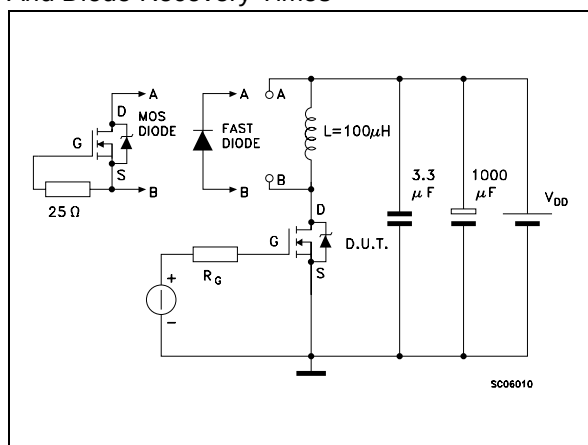
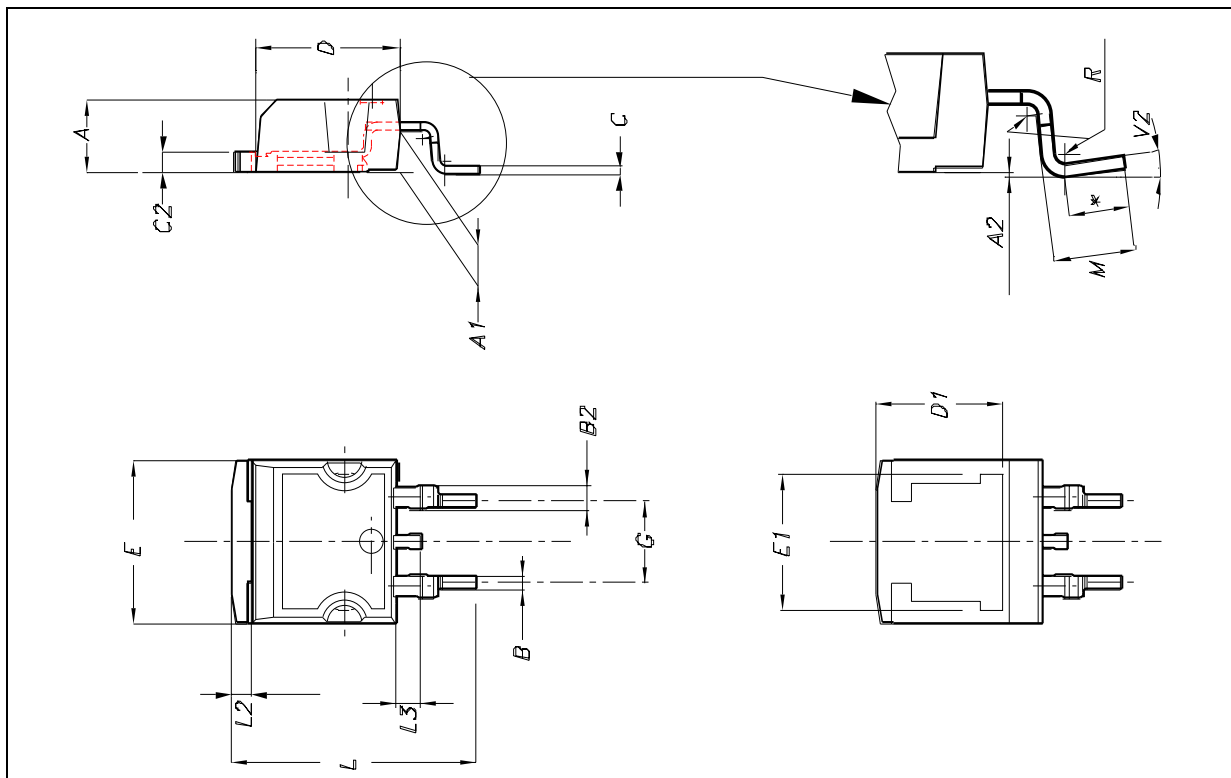


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



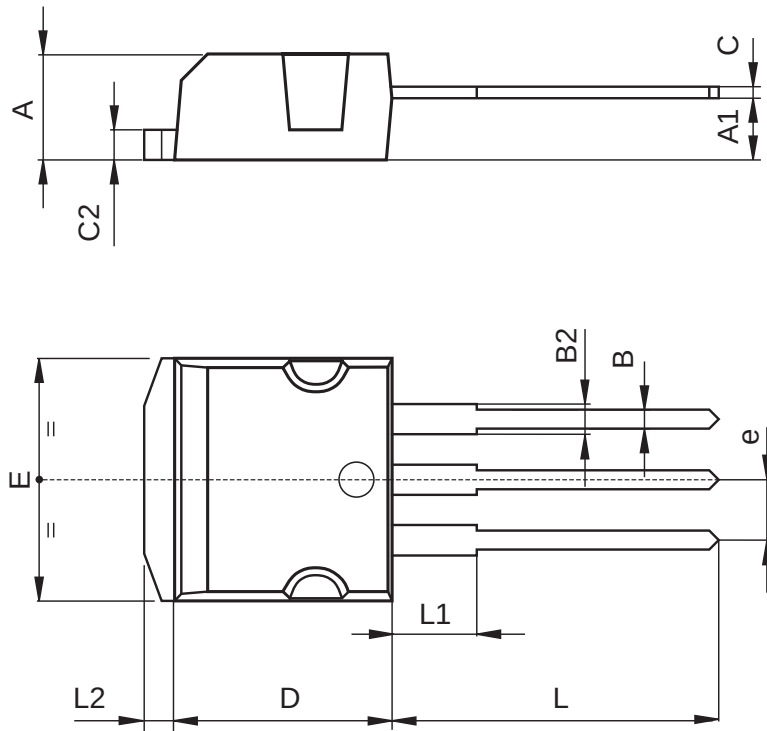
D²PAK MECHANICAL DATA

DIM.	mm.			inch.		
	MIN.	TYP.	MAX.	MIN.	TYP.	TYP.
A	4.4		4.6	0.173		0.181
A1	2.49		2.69	0.098		0.106
A2	0.03		0.23	0.001		0.009
B	0.7		0.93	0.028		0.037
B2	1.14		1.7	0.045		0.067
C	0.45		0.6	0.018		0.024
C2	1.21		1.36	0.048		0.054
D	8.95		9.35	0.352		0.368
D1		8			0.315	
E	10		10.4	0.394		0.409
E1	8.5				0.334	
G	4.88		5.28	0.192		0.208
L	15		15.85	0.591		0.624
L2	1.27		1.4	0.050		0.055
L3	1.4		1.75	0.055		0.069
M	2.4		3.2	0.094		0.126
R		0.4			0.016	
V2	0°		8°	0°		8°



TO-262 (I²PAK) MECHANICAL DATA

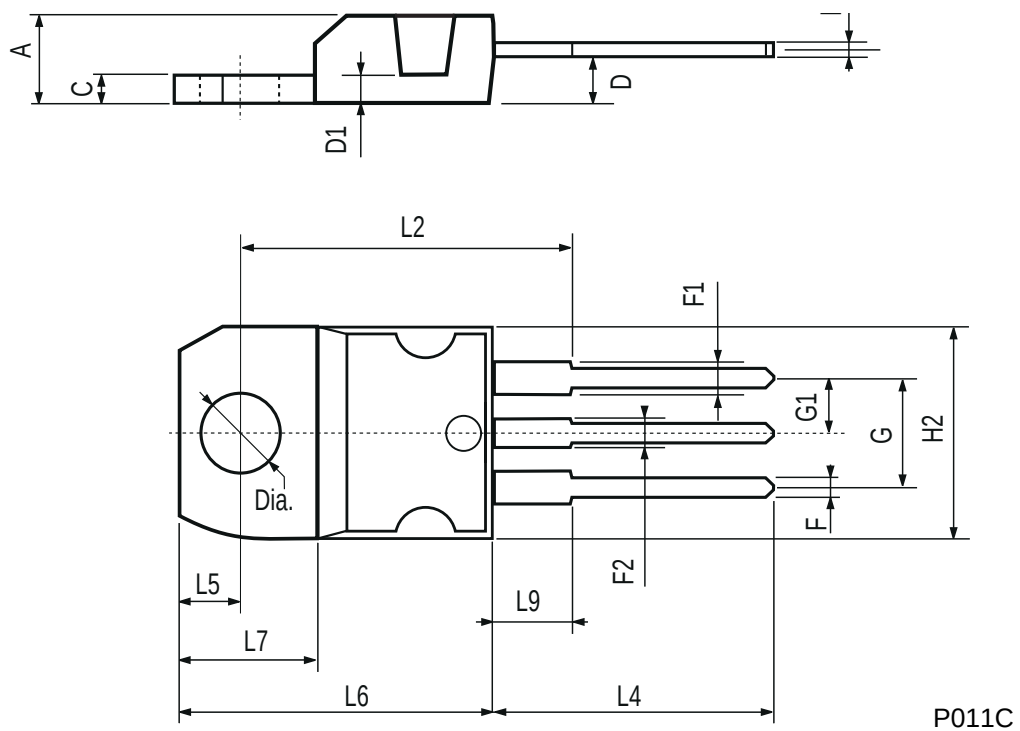
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
A1	2.49		2.69	0.098		0.106
B	0.7		0.93	0.027		0.036
B2	1.14		1.7	0.044		0.067
C	0.45		0.6	0.017		0.023
C2	1.23		1.36	0.048		0.053
D	8.95		9.35	0.352		0.368
e	2.4		2.7	0.094		0.106
E	10		10.4	0.393		0.409
L	13.1		13.6	0.515		0.531
L1	3.48		3.78	0.137		0.149
L2	1.27		1.4	0.050		0.055



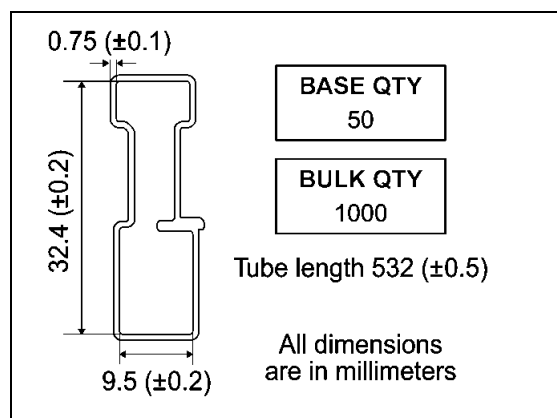
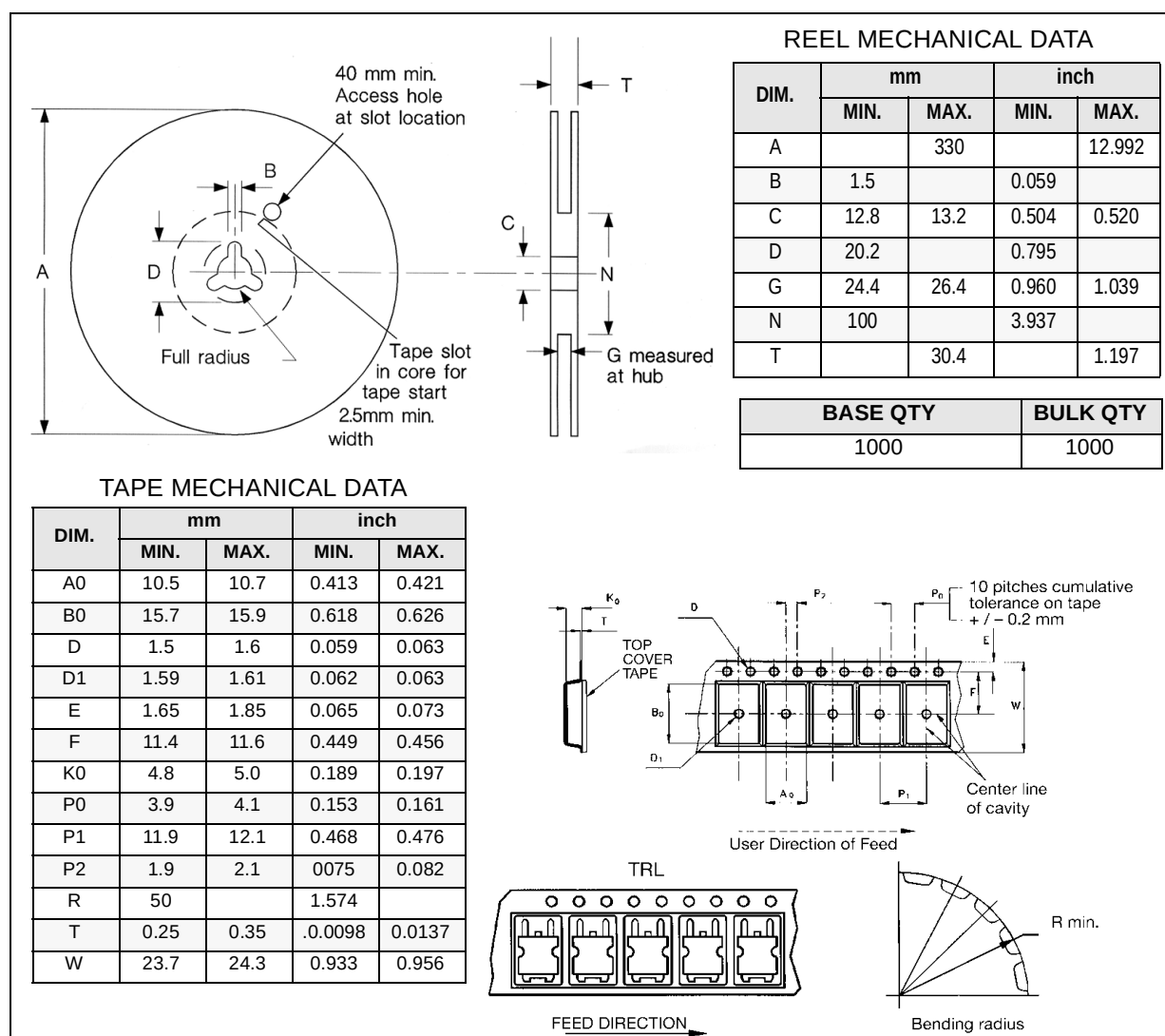
P011P5/E

TO-220 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
C	1.23		1.32	0.048		0.051
D	2.40		2.72	0.094		0.107
D1		1.27			0.050	
E	0.49		0.70	0.019		0.027
F	0.61		0.88	0.024		0.034
F1	1.14		1.70	0.044		0.067
F2	1.14		1.70	0.044		0.067
G	4.95		5.15	0.194		0.203
G1	2.4		2.7	0.094		0.106
H2	10.0		10.40	0.393		0.409
L2		16.4			0.645	
L4	13.0		14.0	0.511		0.551
L5	2.65		2.95	0.104		0.116
L6	15.25		15.75	0.600		0.620
L7	6.2		6.6	0.244		0.260
L9	3.5		3.93	0.137		0.154
DIA.	3.75		3.85	0.147		0.151



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