STP1N120

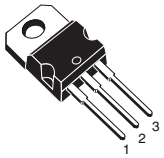
N-channel 1200V - 30Ω - 500mA - TO-220
Zener - protected SuperMESH™ Power MOSFET

PRELIMINARY DATA

General features

Type	V_{DSS}	$R_{DS(on)}$	I_D	P_W
STP1N120	1200V	< 38Ω	500mA	45W

- 100% avalanche tested
- Extremely high dv/dt capability
- ESD improved capability
- New high voltage benchmark
- Gate charge minimized

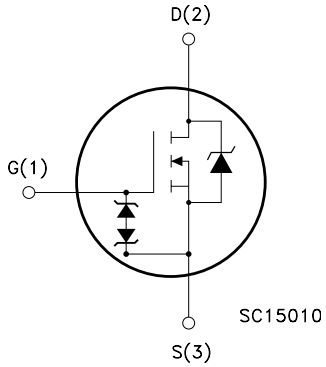


TO-220

Description

The SuperMESH™ series is obtained through an extreme optimization of ST's well established strip-based PowerMESH™ layout. In addition to pushing on-resistance significantly down, special care is taken to ensure a very good dv/dt capability for the most demanding applications. Such series complements ST full range of high voltage Power MOSFETs including revolutionary MDmesh™ products.

Internal schematic diagram



Applications

- Switching application

Order codes

Part number	Marking	Package	Packaging
STP1N120	P1N120	TO-220	Tube

Contents

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage (V_{GS}=0)	1200	V
V_{GS}	Gate-source voltage	± 30	V
I_D	Drain current (continuous) at T_C = 25°C	500	mA
I_D	Drain current (continuous) at T_C = 100°C	315	mA
I_{DM} (1)	Drain current (pulsed)	2	A
	Derating factor	0.36	W/°C
P_{TOT}	Total dissipation at T_C = 25°C	45	W
dv/dt (2)	Peak diode recovery voltage slope	Tbd	V/ns
T_j T_{stg}	Operating junction temperature Storage temperature	-55 to 150	°C

1. Pulse width limited by safe operating area
2. I_{SD} ≤1A, di/dt ≤200A/µs, V_{DD} ≤960

Table 2. Thermal data

Symbol	Parameter	Value	Unit
Rthj-case	Thermal resistance junction-case max	2.78	°C/W
Rthj-amb (1)	Thermal resistance junction-amb max	62.5	°C/W
T_l	Maximum lead temperature for soldering purpose	300	°C

1. When mounted on 1inch² FR-4 board, 2 oz Cu

Table 3. Avalanche characteristics

Symbol	Parameter	Max value	Unit
I_{AS}	Avalanche current, repetitive or not-repetitive (pulse width limited by Tj max)	Tbd	A
E_{AS}	Single pulse avalanche energy (starting Tj=25°C, I_D=I_{AS}, V_{DD}= 50V)	Tbd	mJ

2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1mA, V_{GS}= 0	1200			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max rating, V_{DS} = Max rating,Tc=125°C			1 50	µA µA
I_{GSS}	Gate body leakage current (V_{DS} = 0)	V_{GS} = ±20V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS}= V_{GS}, I_D = 50µA	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS}= 10V, I_D= 0.25A		30	38	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} =25V, f=1MHz, V_{GS}=0		130 22 3		pF pF pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD}=960V, I_D = 500mA V_{GS} =10V *(see Figure 2)*		7 Tbd Tbd		nC nC nC

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	Tbd		Tbd		ns
t_r	Rise time			Tbd		ns
$t_{d(off)}$	Turn-off delay time			Tbd		ns
t_f	Fall time			Tbd		ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
I_{SD}	Source-drain current				500	mA
I_{SDM}	Source-drain current (pulsed)				2	A
V_{SD} (1)	Forward on voltage	I_{SD}=1A, V_{GS}=0			Tbd	V
t_{rr}	Reverse recovery time	I_{SD}=1A, V_{DD}=100V		Tbd		ns
Q_{rr}	Reverse recovery charge	di/dt = 50A/µs,Tj=25°C		Tbd		nC
I_{RRM}	Reverse recovery current	*(see Figure 6)*		Tbd		A
t_{rr}	Reverse recovery time	I_{SD}=1A,V_{DD}=100V		Tbd		ns
Q_{rr}	Reverse recovery charge	di/dt=50A/µs,Tj=150°C		Tbd		nC
I_{RRM}	Reverse recovery current	*(see Figure 6)*		Tbd		A

1. Pulsed: pulse duration = 300µs, duty cycle 1.5%

Table 8. Gate-source zener diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
BV_{GSO} (1)	Gate-source breakdown voltage	Igs ± 1mA, (open drain)	30			V

1. The built-in-back zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possibile voltage transients that may occasionally be applied from gate to source. In this respect the zener voltage is appropriate to achieve an efficient and ost-effective intervention to protect the device's integrity. These integrated zener diodes thus avoid the usage of external components.

3 Test circuit

Figure 1. Switching times test circuit for resistive load

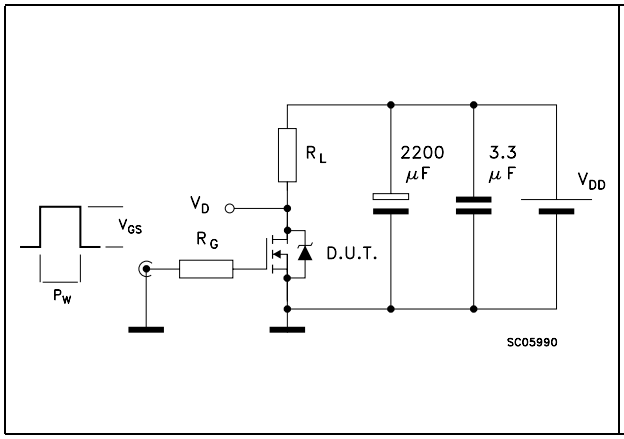


Figure 2. Gate charge test circuit

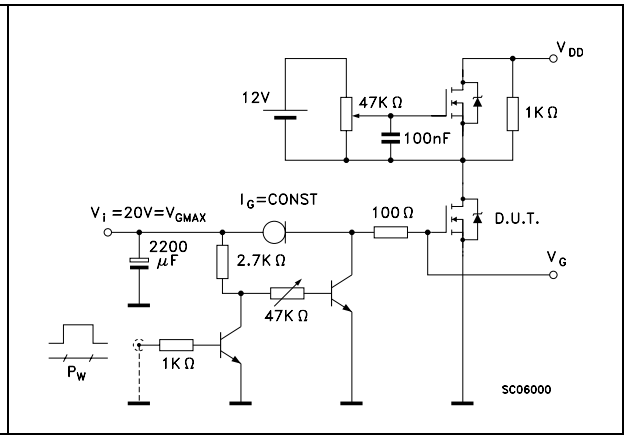


Figure 3. Test circuit for inductive load switching and diode recovery times

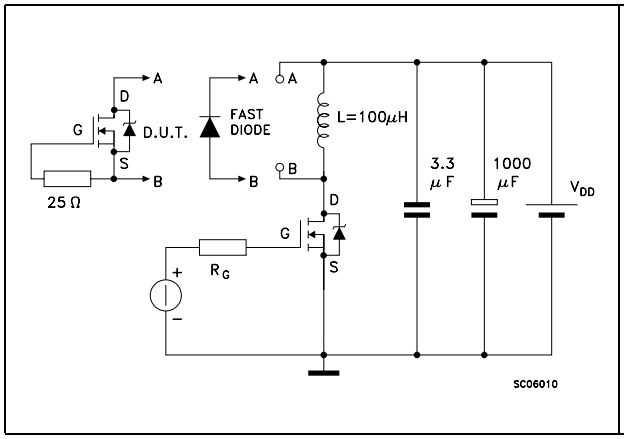


Figure 4. Unclamped inductive load test circuit

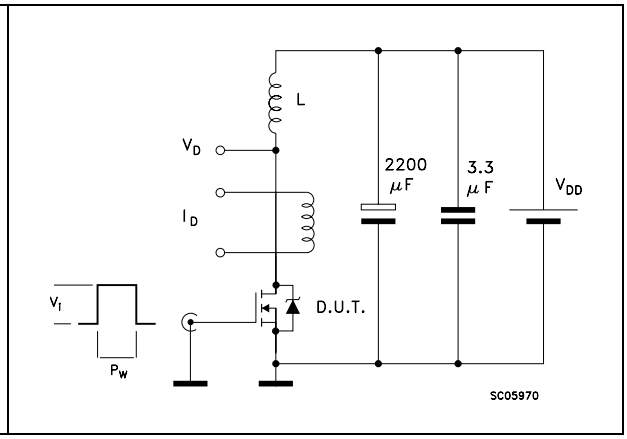


Figure 5. Unclamped inductive waveform

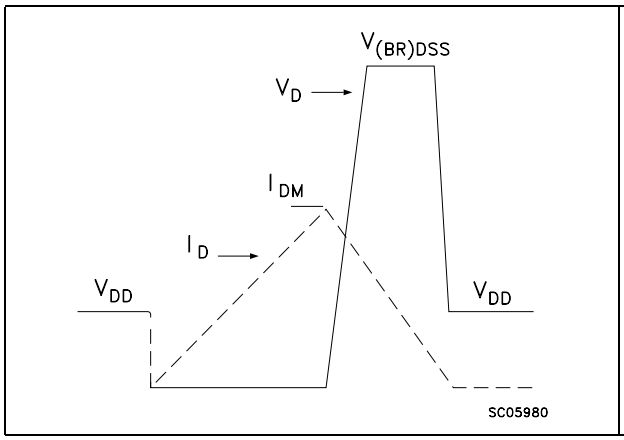
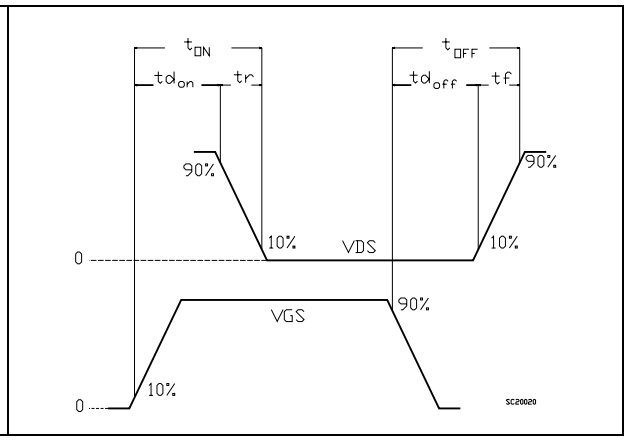


Figure 6. Switching time waveform

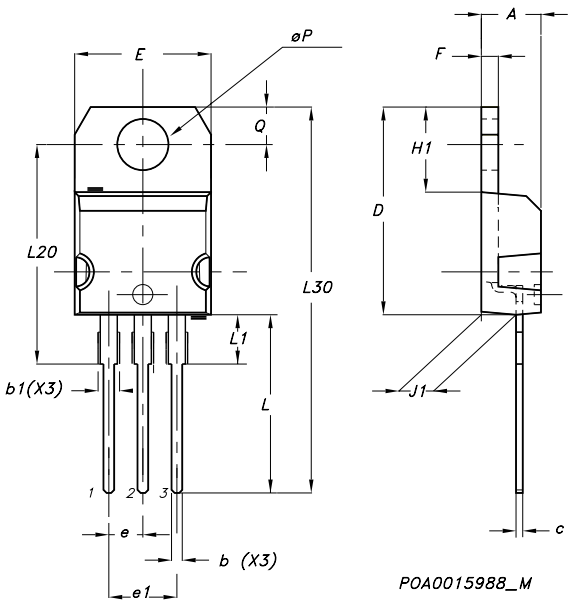


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: *www.st.com*

TO-220 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.15		1.70	0.045		0.066
c	0.49		0.70	0.019		0.027
D	15.25		15.75	0.60		0.620
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.052
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
øP	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116



5 Revision history

Table 9. Revision history

Date	Revision	Changes
14-Sep-2006	1	First release

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