SUN MICROELECTRONICS

STP2021

July 1997

PMC

DATA SHEET — Power Management Controller

DESCRIPTION

The STP2021 Power Management Controller brings power management to SBus-based systems. The STP2021 interfaces to the SBus via the byte-wide expansion bus (EBus) provided by the STP2001 Slave I/O Controller.

The STP2021 effectively shuts down the system when it is not in use by causing the processor to go into low-power mode. It generates the control signal to the processor used to stop the main processor clock, depending on system activity. Once activity is detected, the system returns to normal operation. In addition to system control, it can also be used to switch off power and/or clocks to those devices not being used.

For portable applications, the STP2021 provides an A/D interface to store and update battery voltage and D/A interface support for LCD backlight brightness control. Although it is ideal for portables, the STP2021 can also be used to reduce power consumption in line-operated applications such as desktops.

Features

- Stops processor clock when system is inactive (only DRAM refresh and SBus clock are active)
- Returns processor clock to normal speeds when activity is detected
- Switches off power and/or clocks to devices not in use
- Stores and updates the current battery voltage
- Controls the backlight display brightness
- JTAG internal boundary SCAN logic

Benefits

- Processor goes into low-power mode, reducing system power consumption
- System promptly returns to normal operation
- Reduction in overall system power consumption
- Provides the end-user with “fuel-gauge” of the battery life for portable applications
- Reduction in power consumption when system is not in use
- Improved chip and board level testability

BLOCK AND TYPICAL APPLICATION DIAGRAMS

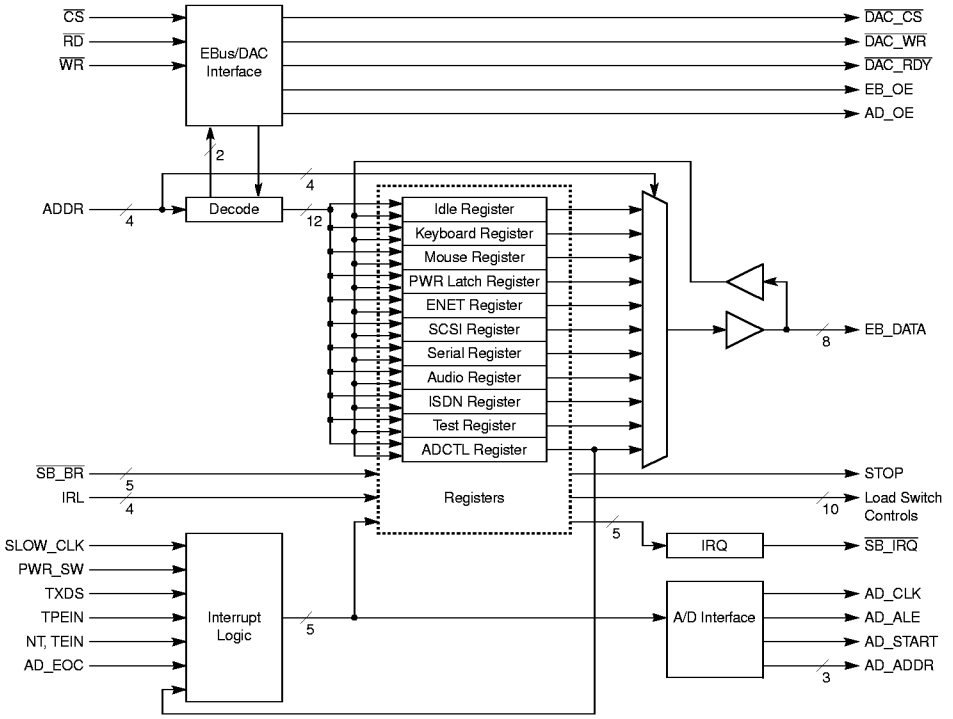


Figure 1. STP2021 Block Diagram

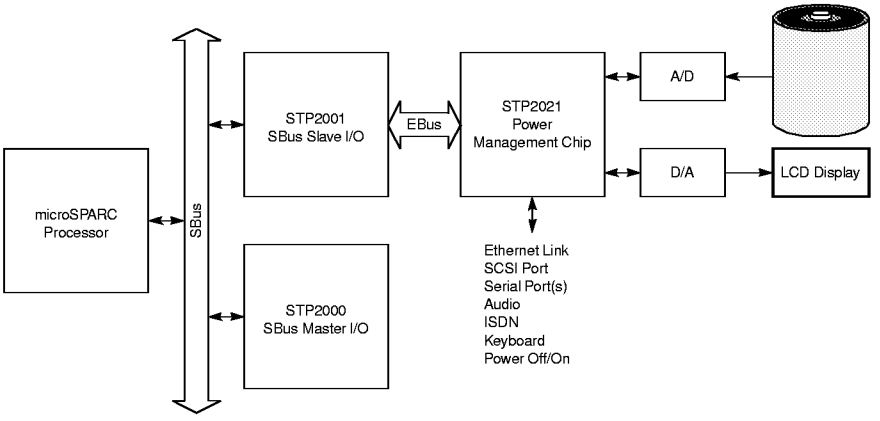


Figure 2. STP2021 Typical Application

SIGNAL DESCRIPTIONS

Clock Signals

Signal	Type	Description
CLK	Input	SBus clock input.
SLOW_CLK	Input	32 kHz clock input.

Bus Interface

Signal	Type	Description
ADDR[3:0]	Input	Address lines.
IOD[7:0]	I/O	Data lines.
$\overline{RD}$	Input	Read.
$\overline{WR}$	Input	Write.
$\overline{RDY}$	Output	Ready.
$\overline{CS}$	Input	Chip select.

Load Switch Controls

Signal	Type	Description
LINKEN	Output	Ethernet link test (0 = Link Test disabled, 1 = Link Test enabled).
PWR_CTL	Output	Power latch control.
TPE_$\overline{PDN}$	Output	TPE power down (0 = power down, 1 = normal mode).
SCSI_CTL	Output	SCSI Term power control (0 = normal mode, 1 = power down).
$\overline{SERIALA\_CTL}$	Output	Serial port A driver control (0 = power down, 1 = normal mode).
$\overline{SERIALB\_CTL}$	Output	Serial port B driver control (0 = power down, 1 = normal mode).
ENET_LBK	Output	Ethernet loopback (0 = normal loopback, 1 = power down).
AUDIO_CTL	Output	Audio control (0 = normal mode, 1 = power down).
ISDN_CTL	Output	ISDN control (0 = normal mode, 1 = power down).

IDLE Mode Configuration

Signal	Type	Description
$\overline{SB\_BR[4:0]}$	Input	SBus bus request.
IRL[3:0]	Input	Interrupt request level.
STOP	Output	Processor clock stop mode.

Interrupt Interface

Signal	Type	Description
$\overline{\text{SB\_IRQ}}$	Output	SBus Interrupt.
PWR_SW	Input	Power on/off detect.
TXDS	Input	Keyboard TXD sense.
TPEIN	Input	Ethernet sense.
NTIN	Input	ISDN sense 1 (NT connect).
TEIN	Input	ISDN sense 0 (TE connect).

A/D, D/A Interface

Signal	Type	Description
$\overline{\text{DAC\_CS}}$	Output	DAC chip select.
$\overline{\text{DAC\_WR}}$	Output	DAC write strobe.
AD_CLK	Output	A/D 781.25 kHz clock output.
AD_START	Output	A/D start.
$\overline{\text{AD\_OE}}$	Output	A/D output enable.
AD_EOC	Input	A/D end of conversion.
AD_ALE	Output	A/D address latch enable.
AD_ADDR[2:0]	Output	A/D address select.

Miscellaneous Signals

Signal	Type	Description
$\overline{\text{RST}}$	Input	Power-on reset.
TESTEN	Input	Three-states all outputs.
JTAG_DI	Input	JTAG data input.
JTAG_DO	Output	JTAG data output.
JTAG_CLK	Input	JTAG clock input.
$\overline{\text{JTAG\_RST}}$	Input	JTAG reset input

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings [1]

Symbol	Parameter	Rating	Units
V_{CC}	Power supply voltage	5.25	V
V_{IN}	Input voltage range	$GND \le V_{IN} \le V_{CC}$	V
P_D	Power dissipation	400	mW
T_J	Operating junction temperature	0 to +70	°C

1. Operation of the device at values in excess of those listed above will result in degradation or destruction of the device. All voltages are defined with respect to ground. Functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
V_{CC}	Supply voltage	4.75	5.0	5.25	V
T_A	Temperature	0	–	70	°C

Capacitance

Symbol	Parameter	Max	Units
C_{IN}	Input capacitance	8	pF
C_{OUT}	Output capacitance	10	pF

DC Characteristics (V_{CC} = 5.0V ±5%)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IL}	Input low voltage		–	–	0.8	V
V_{IH}	Input high voltage		2.0	–	–	V
V_{OH}	Output high voltage	I_{OH} = 4.0 mA	2.4	–	–	V
		I_{OH} = 100 µA	3.5	–	–	V
V_{OL}	Output low voltage	I_{OL} = -4.0 mA	–	–	0.4	V
		I_{OL} = -100 µA	–	–	0.8	V
I_{IN}	Input current	$V_{IN} = V_{CC}$ or GND	-10	1	10	µA
	Input with pull-ups	$V_{IN} = V_{CC}$	-8	-30	-100	µA

AC Characteristics

Description	Load	Min	Max	Units
CLK period		40	60	ns
$\overline{CS}$, $\overline{RD}$, $\overline{WR}$ setup to CLK		15	–	ns
CLK to $\overline{GEN\_RDY}$ low	30 pf	–	20.3	ns
CLK to $\overline{GEN\_RDY}$ high	30 pf	–	23.1	ns
CLK to STOP low	30 pf	–	19.0	ns
CLK to STOP high	30 pf	–	24.2	ns
CLK to $\overline{SB\_IRQ}$ low	50 pf	–	20.1	ns
CLK to $\overline{SB\_IRQ}$ three-state	50 pf	–	27.0	ns
AD_ALE pulse width	30 pf	321	–	ns
AD_START pulse width	30 pf	241	–	ns
$\overline{CS}$, $\overline{RD}$, $\overline{WR}$ hold to write CLK		0	–	ns
CLK to IOD valid	70 pf	–	34.5	ns
CLK to IOD three-state	70 pf	–	27	ns

TIMING DIAGRAMS

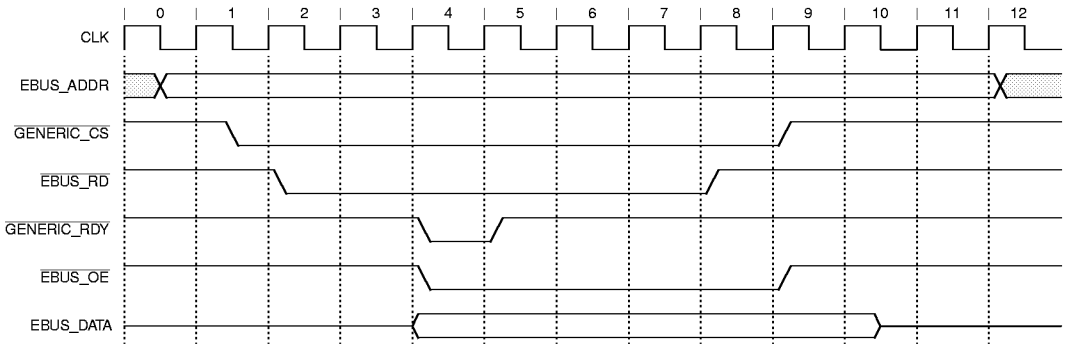


Figure 3. Read Cycle

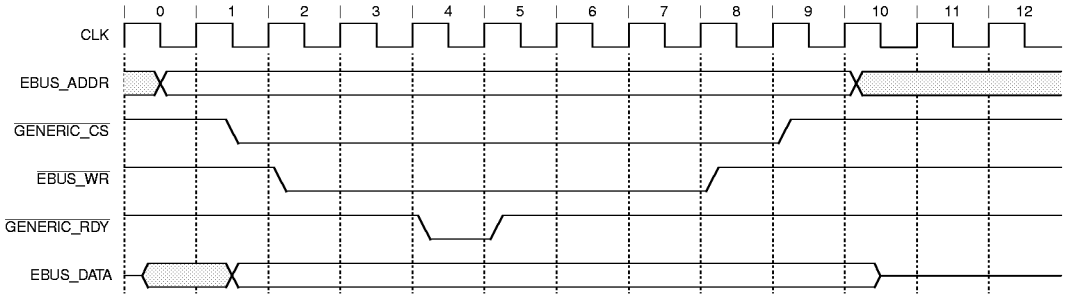


Figure 4. Write Cycle

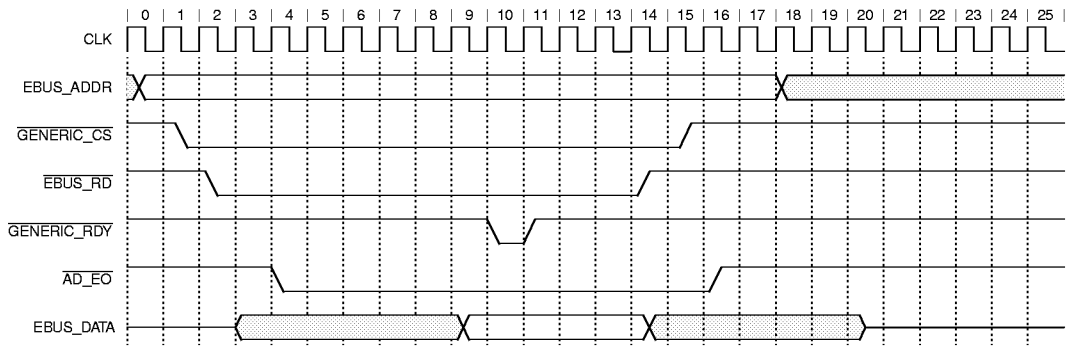


Figure 5. A/D Read Cycle

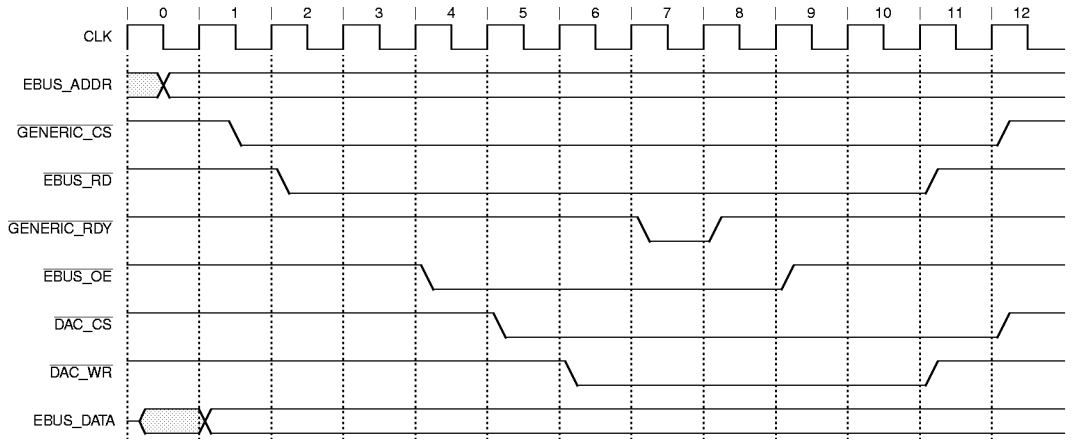
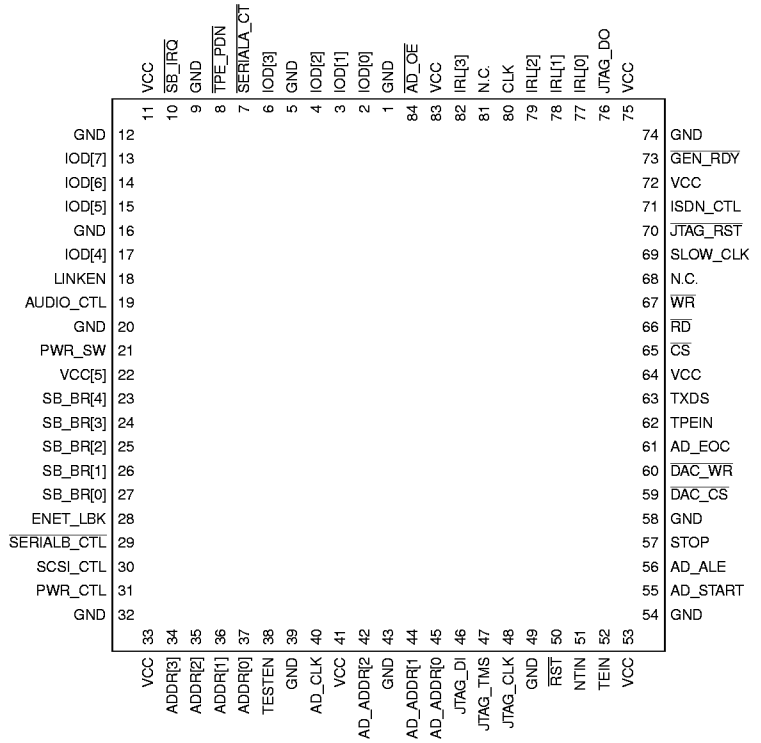


Figure 6. D/A Write Cycle

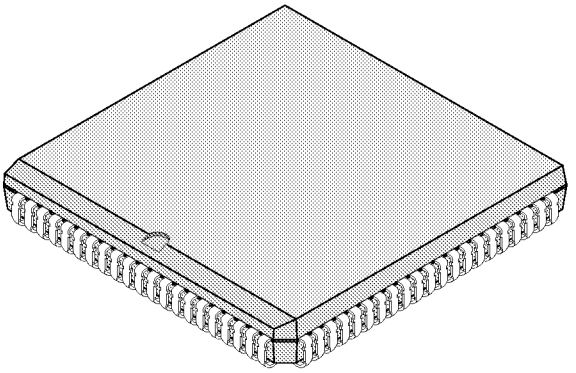
PACKAGE INFORMATION

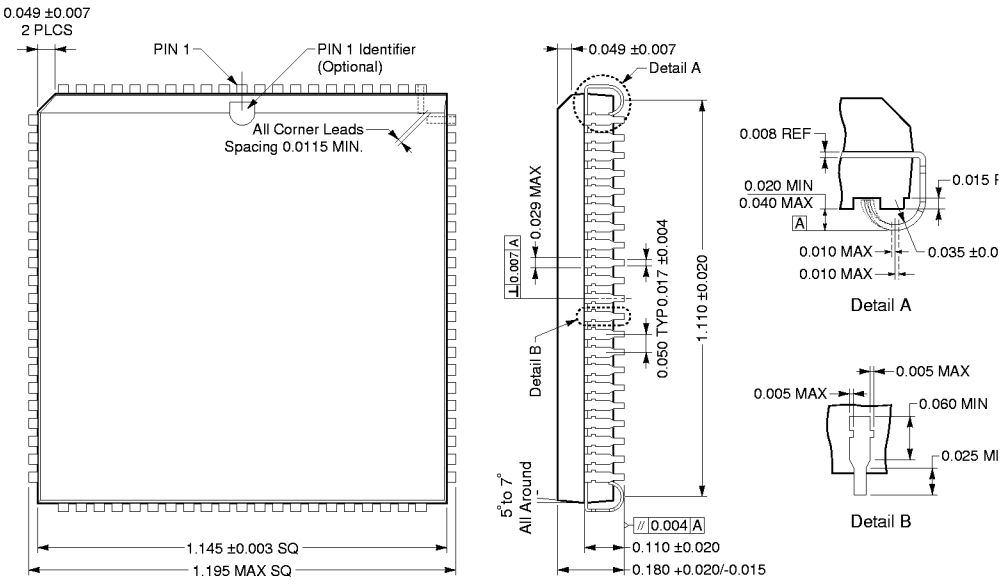
84-Lead PLCC Pin Assignment

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
1	GND	15	IOD[5]	29	SERIALB_CTL	43	GND	57	STOP	71	ISDN_CTL
2	IOD[0]	16	GND	30	SCSI_CTL	44	AD_ADDR[1]	58	GND	72	VCC
3	IOD[1]	17	IOD[4]	31	PWR_CTL	45	AD_ADDR[0]	59	DAC_CS	73	GEN_RDY
4	IOD[2]	18	LINKEN	32	GND	46	JTAG_DI	60	DAC_WR	74	GND
5	GND	19	AUDIO_CTL	33	VCC	47	JTAG_TMS	61	AD_EOC	75	VCC
6	IOD[3]	20	GND	34	ADDR[3]	48	JTAG_CLK	62	TPEIN	76	JTAG_DO
7	SERIALA_CTL	21	PWR_SW	35	ADDR[2]	49	GND	63	TXDS	77	IRL[0]
8	TPE_PDN	22	VCC	36	ADDR[1]	50	RST	64	VCC	78	IRL[1]
9	GND	23	SB_BR[4]	37	ADDR[0]	51	NTIN	65	CS	79	IRL[2]
10	SB_IRQ	24	SB_BR[3]	38	TESTEN	52	TEIN	66	RD	80	CLK
11	VCC	25	SB_BR[2]	39	GND	53	VCC	67	WR	81	N.C.
12	GND	26	SB_BR[1]	40	AD_CLK	54	GND	68	N.C.	82	IRL[3]
13	IOD[7]	27	SB_BR[0]	41	VCC	55	AD_START	69	SLOW_CLK	83	VCC
14	IOD[6]	28	ENET_LBK	42	AD_ADDR[2]	56	AD_ALE	70	JTAG_RST	84	AD_OE



84-Lead PLCC Package Dimensions





Note: Molding flash is permitted around periphery of body.
Flash shall not extend more than 0.010 beyond body.

Dimensions in Inches

ORDERING INFORMATION

Part Number	Description
STP2021PLCC	84-Pin Plastic Leaded Chip Carrier (PLCC)

Document Part Number: STP2021