SPARC Technology Business

STP2022

November 1994

STP2022

DATA SHEET — Multi-Interface Chip

DESCRIPTION

The STP2022 Multi-Interface Chip (MIC) is an integrated SBus device that provides two serial ports and an infra-red interface. The infra-red (IR) interface provides IR modulation/demodulation and input multiplexing. All necessary digital logic for this application has been integrated onto the STP2022.

The STP2022 features high data transfer rates, low interrupt level and frequency. This is achieved through large internal FIFOs which buffer both incoming and outgoing data. The STP2022 also features a programmable SBus interrupt to allow the interrupt frequency to be adjusted based on transfer rates and the system environment.

The STP2022 can be used on an SBus card to perform the address decode and transfer acknowledge for an FCode PROM or NVRAM. For additional expansion or enhancements, the STP2022 provides support for connecting 8-bit devices to the SBus.

Features

- Two full function, general purpose asynchronous serial ports.
- 16-bit, SBus slave interface.
- Large (64 byte) transmit and receive FIFOs for low interrupt priority and frequency.
- Full hardware flow control capability.
- Programmable interrupt based on FIFO water marks and time-out.
- Multi-mode IR interface.
- PROM/NVRAM and 8 bit Expansion Interface.
- JTAG internal and boundary scan logic

Benefits

- Enables low-cost IR devices to access SBus
- Low interrupt priority and frequency; high data transfer rates
- Improved chip and board level testability

BLOCK, APPLICATION AND LOGIC DIAGRAMS

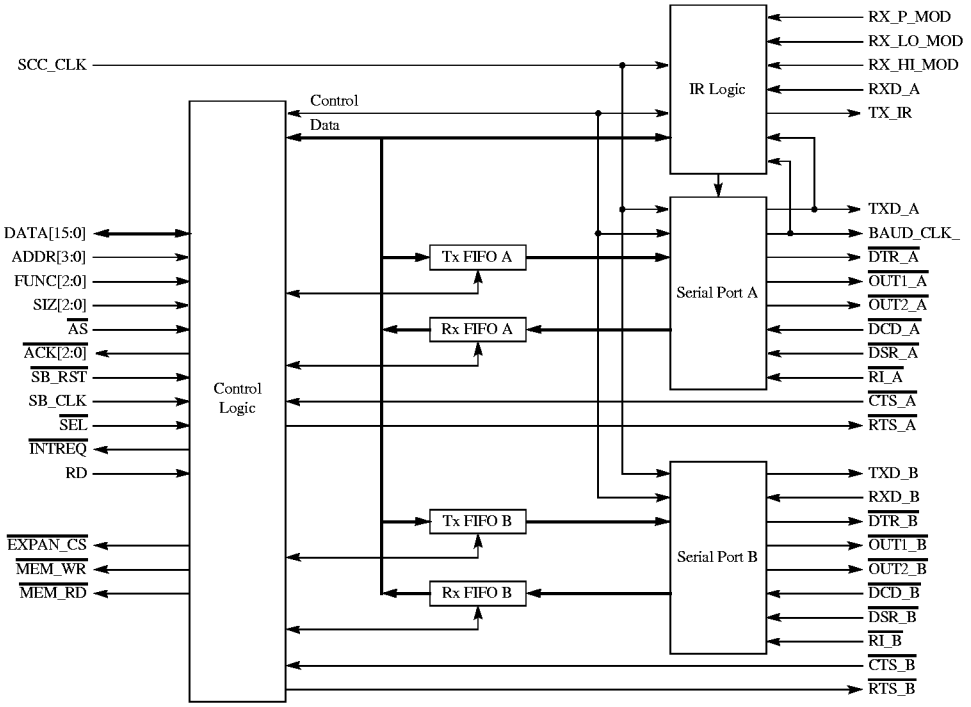


Figure 1. STP2022 Block Diagram

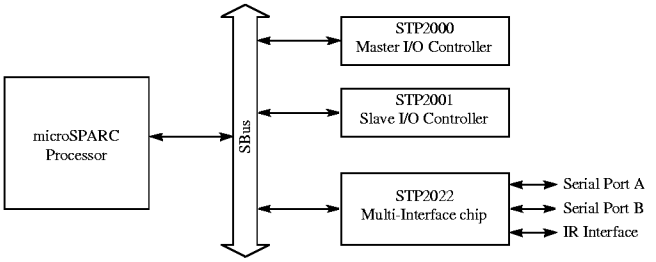


Figure 2. STP2022 Typical Application Diagram

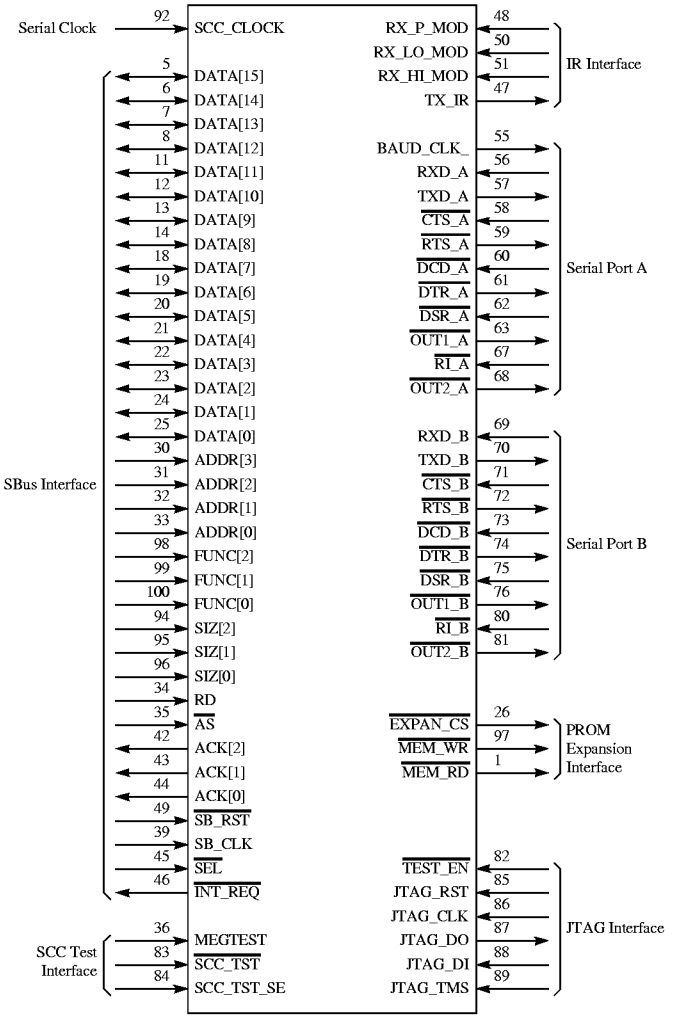


Figure 3. STP2022 Logic Symbol

SIGNAL DESCRIPTIONS

SBus Interface

Name	Type	Description
DATA[15:0]	I/O	SBus Data.
ADDR[3:0]	Input	SBus Address Bus.
FUNC[2:0]	Input	Function Select. Wired to SBus address bits.
SIZ[2:0]	Input	Transfer Size.
RD	Input	Transfer Direction.
$\overline{AS}$	Input	Address Strobe.
$\overline{ACK}$[2:0]	Output	Transfer Acknowledgment.
$\overline{SB\_RST}$	Input	SBus Reset.
SB_CLK	Input	SBus Clock.
$\overline{SEL}$	Input	Slave Select.
$\overline{INTREQ}$	Output	Interrupt Request.

Serial Controller Clock

Name	Type	Description
SCC_CLOCK	Input	Serial controller clock.

Serial Port (A)

Name	Type	Description
RXD_A	Input	Receive Serial Data A.
TXD_A	Output	Transmit Serial Data A.
$\overline{CTS\_A}$	Input	Clear to Send A.
$\overline{RTS\_A}$	Output	Request to Send A.
$\overline{DCD\_A}$	Input	Data Carrier Detect A.
$\overline{DTR\_A}$	Output	Data Terminal Ready A.
$\overline{DSR\_A}$	Input	Data Set Ready A.
$\overline{OUT1\_A}$	Output	Out 1 A.
$\overline{RI\_A}$	Input	Ring Indicator A.
$\overline{OUT2\_A}$	Output	Out 2 A.
BAUD_CLK_A	Output	Baud Clock A.

Serial Port (B)

Name	Type	Description
RXD_B	Input	Receive Serial Data B.
TXD_B	Output	Transmit Serial Data B.
$\overline{\text{CTS\_B}}$	Input	Clear to Send B.
$\overline{\text{RTS\_B}}$	Output	Request to Send B.
$\overline{\text{DCD\_B}}$	Input	Data Carrier Detect B.
$\overline{\text{DTR\_B}}$	Output	Data Terminal Ready B.
$\overline{\text{DSR\_B}}$	Input	Data Set Ready B.
$\overline{\text{OUT1\_B}}$	Output	Out 1 B.
$\overline{\text{RI\_B}}$	Input	Ring Indicator B.
$\overline{\text{OUT2\_B}}$	Output	Out 2 B.

IR Interface

Name	Type	Description
TX_IR	Output	IR Transmit Port. Encoded IR signal to be transmitted. (Output of PROCMON when $\overline{\text{TESTEN}}$ is low)
RX_P_MOD	Input	IR Receive Port, Pulse Modulation protocol to be decoded by MIC.
RX_LO_MOD	Input	IR Receive Port, Low Frequency Modulation. Standard serial data format.
RX_HI_MOD	Input	IR Receive Port, High Frequency Modulation. Standard serial data format.

PROM/Expansion Interface

Name	Type	Description
$\overline{\text{MEM\_RD}}$	Output	Prom/NVRAM Read.
$\overline{\text{MEM\_WR}}$	Output	NVRAM Write.
$\overline{\text{EXPAN\_CS}}$	Output	Expansion Bus Chip Select.

JTAG Interface

Name	Type	Description
JTAG_CLK	Input	JTAG Clock.
$\overline{\text{JTAG\_RST}}$	Input	JTAG Reset.
JTAG_DI	Input	JTAG Serial Data Input.
JTAG_DO	Output	JTAG Serial Data Input.
JTAG_TMS	Input	JTAG Test Mode. (Control for PROCMON).
$\overline{\text{TEST\_EN}}$	Input	Three-state enable for all Three-state buffers. (Select for PROCMON).

Serial Controller Test Interface

Name	Type	Description
$\overline{\text{SCC\_TST}}$	Input	Serial controller Test Mode.
SCC_TST_SEL	Input	Serial controller Test Port Select.
MEGTEST	Input	Megafunction Test Pin. Used as input to megafunction during test mode. Sometimes referred to as spare.

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings [1]

Symbol	Parameter	Rating	Units
V_{CC}	Power supply voltage	5.25	V
V_{IN}	Input voltage range	GND ð V_{IN} ð V_{CC}	V
T_J	Operating junction temperature	0 to +100	°C

1. Operation of the device at values in excess of those listed above will result in degradation or destruction of the device. All voltages are defined with respect to ground. Functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
V_{CC}	Supply voltage	4.75	5.0	5.25	V
T_A	Temperature	0	–	70	°C

Capacitance

Symbol	Parameter	Max	Units
C_{IN}	Input capacitance	3	pF
C_{OUT}	Output capacitance	2.7	pF

DC Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IL}	Input low voltage	TTL Inputs	–	–	0.8	V
		CMOS Inputs	–	–	0.3 x V_{DD}	V
V_{IH}	Input high voltage	TTL Inputs	2.0	–	–	V
		CMOS Inputs	0.7 x V_{DD}	–	–	V
VT	Switching threshold	TTL	–	1.5	–	V
		CMOS	–	2.5	–	V
VT+	Schmitt trigger, positive threshold	CMOS	–	3.0	4.0	V
VT-	Schmitt trigger, negative threshold	CMOS	1.0	1.5	–	V
V_{OH}	Output high voltage	I_{OH} = 2.0 mA	2.4	4.5	–	V
		I_{OH} = 4.0 mA	2.4	4.5	–	V
V_{OL}	Output low voltage	I_{OL} = -2.0 mA	–	0.2	0.4	V
		I_{OL} = -4.0 mA	–	0.2	0.4	V
I_{IN}	Input current	V_{IN} = V_{CC} or GND	-10	±1	10	µA
	Input current (Inputs with Pull-ups)	V_{IN} = V_{CC}	-35	-115	-350	µA

AC Characteristics: SBus Input TIming

Signal	Description	Load	Min	Max	Units
1	SBus clock period		40	60	ns
2	$\overline{AS}$, $\overline{SEL}$ setup to SB_CLK		15	–	ns
3	ADDR, FUNC, SIZ setup to SB_CLK		15	–	ns
4	RD setup to SB_CLK		15	–	ns
5	Data setup to SB_CLK		15	–	ns
6	$\overline{AS}$, $\overline{SEL}$ hold time from SB_CLK		0	–	ns
7	ADDR, FUNC, SIZ hold time from SB_CLK		0	–	ns
8	RD hold time from SB_CLK		0	–	ns
9	Data hold time from SB_CLK		0	–	ns

AC Characteristics: SBus Output Timing

Signal	Description	Load	Min	Max	Units
10	SB_CLK to $\overline{ACK}$ valid	100 pf	2.5	22.5	ns
11	SB_CLK to read data valid	100 pf	2.5	22.5	ns
12	SB_CLK to $\overline{ACK}$ three-state	100 pf	2.5	24	ns
13	SB_CLK to DATA three-state	100 pf	2.5	20	ns

AC Characteristics: PROM/Expasion Interface Timing

Signal	Description	Load	Min	Max	Units
14	SB_CLK to $\overline{MEM\_RD}$, $\overline{MEM\_WR}$, $\overline{EXPAN\_CS}$ active	50 pf	–	16	ns
15	SB_CLK to $\overline{MEM\_RD}$, $\overline{MEM\_WR}$, $\overline{EXPAN\_CS}$ inactive	50 pf	–	12	ns
16	DATA setup to $\overline{MEM\_WR}$, $\overline{EXPAN\_CS}$ (WR)	50 pf	295	–	ns
17	DATA hold from $\overline{MEM\_WR}$, $\overline{EXPAN\_CS}$ (WR)	50 pf	28	–	ns
18	$\overline{MEM\_RD}$, $\overline{EXPAN\_CS}$ (RD) to DATA valid (8 clks x 40ns - 17.5 ns - #14)	50 pf	–	286.5	ns
19	$\overline{MEM\_RD}$, $\overline{EXPAN\_CS}$ (RD) to DATA three-state (35 ns - #15)	50 pf	–	23	ns

TIMING DIAGRAMS

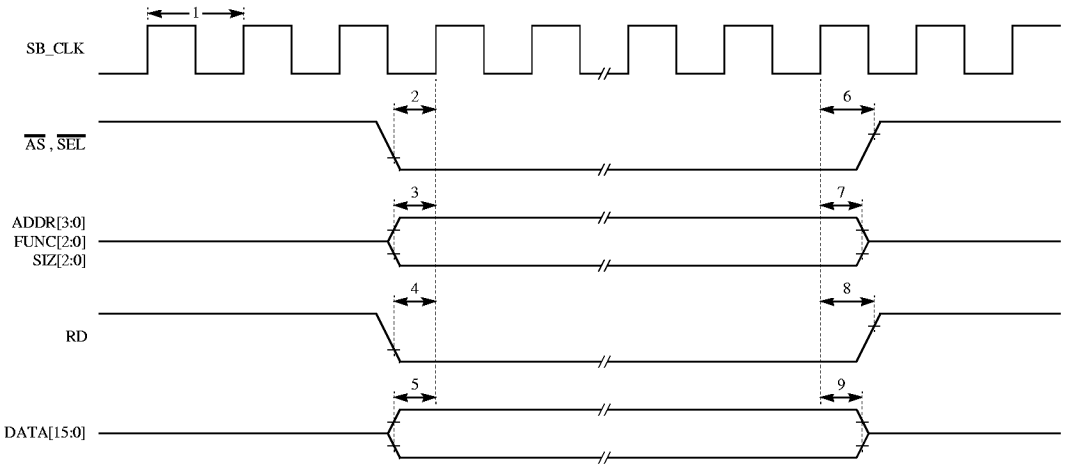


Figure 4. SBus Input Timing

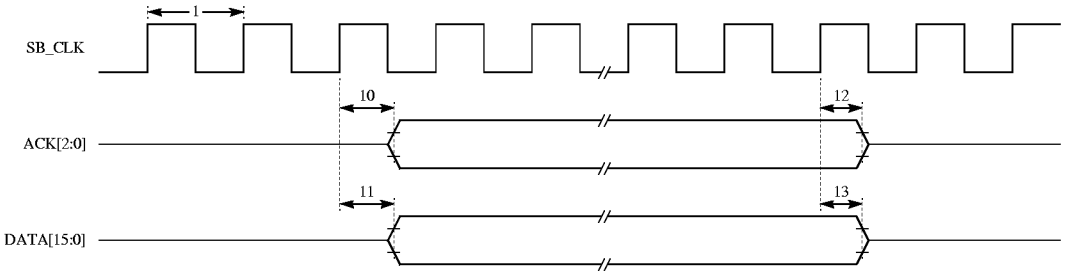
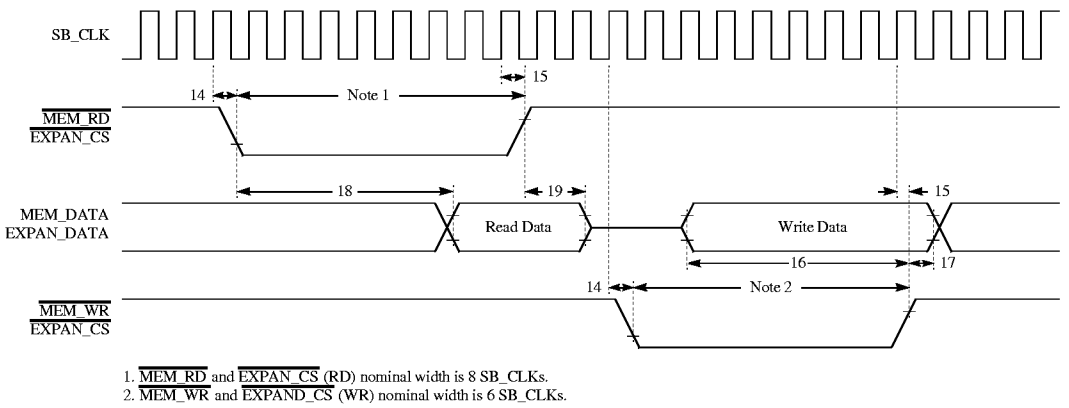


Figure 5. SBus Output Timing



1. MEM_RD and EXPAN_CS (RD) nominal width is 8 SB_CLKs.
2. MEM_WR and EXPAND_CS (WR) nominal width is 6 SB_CLKs.

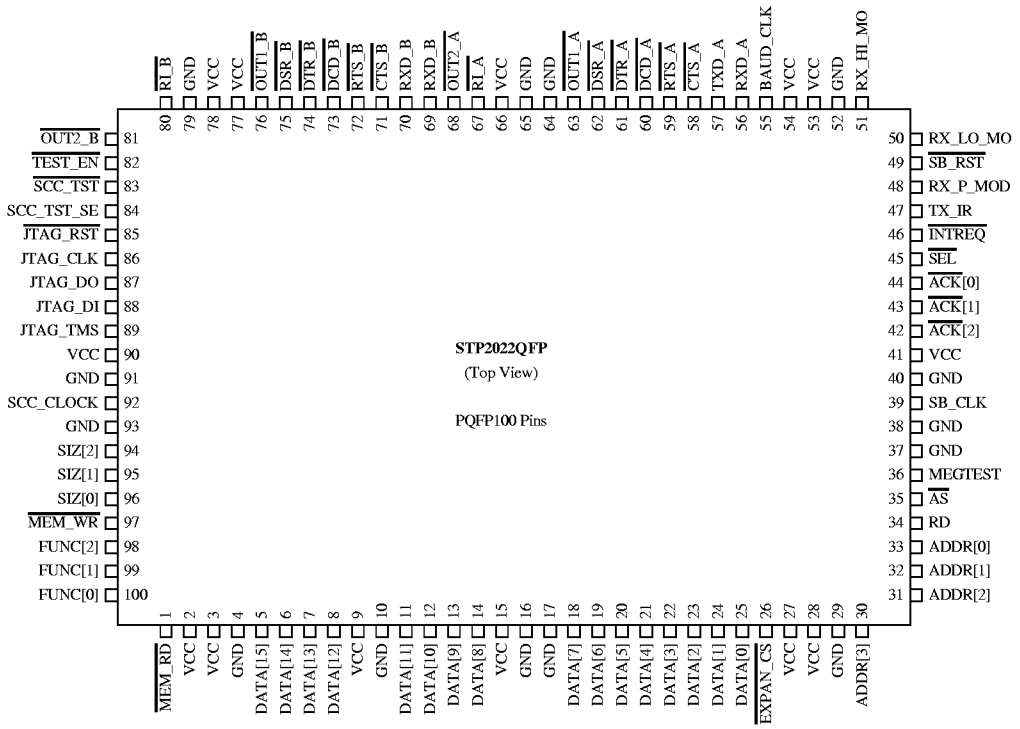
Figure 6. PROM/Expansion Interface Timing

PACKAGE INFORMATION

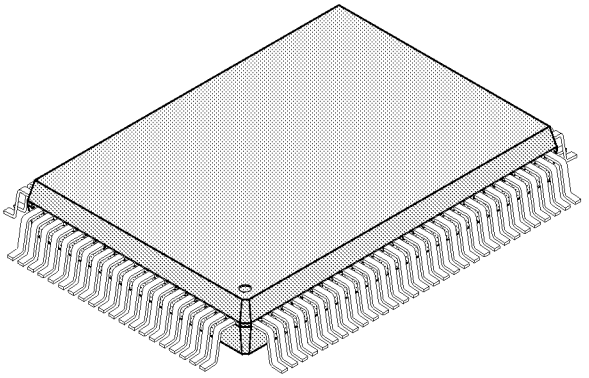
100-Pin PQFP Pin Assignment

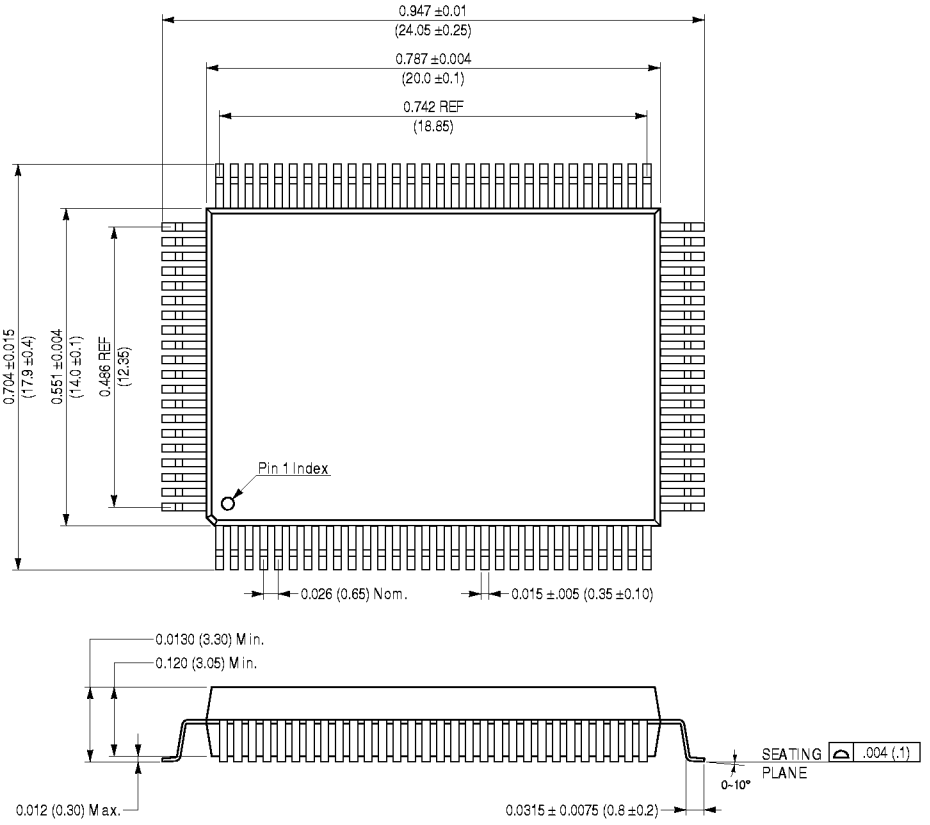
Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
1	MEM_RD	21	DATA[4]	41	VCC	61	DTR_A	81	OUT2_B
2	VCC	22	DATA[3]	42	ACK[2]	62	DSR_A	82	TEST_EN
3	VCC	23	DATA[2]	43	ACK[1]	63	OUT1_A	83	SCC_TST
4	GND	24	DATA[1]	44	ACK[0]	64	GND	84	SCC_TST_SEL
5	DATA[15]	25	DATA[0]	45	SEL	65	GND	85	JTAG_RST
6	DATA[14]	26	EXPAN_CS	46	INTREQ	66	VCC	86	JTAG_CLK
7	DATA[13]	27	VCC	47	TX_IR	67	RI_A	87	JTAG_DO
8	DATA[12]	28	VCC	48	RX_P_MOD	68	OUT2_A	88	JTAG_DI
9	VCC	29	GND	49	SB_RST	69	RXD_B	89	JTAG_TMS
10	GND	30	ADDR[3]	50	RX_LO_MOD	70	TXD_B	90	VCC
11	DATA[11]	31	ADDR[2]	51	RX_HI_MOD	71	CTS_B	91	GND
12	DATA[10]	32	ADDR[1]	52	GND	72	RTS_B	92	SCC_CLOCK
13	DATA[9]	33	ADDR[0]	53	VCC	73	DCD_B	93	GND
14	DATA[8]	34	RD	54	VCC	74	DTR_B	94	SIZ[2]
15	VCC	35	AS	55	BAUD_CLK_A	75	DSR_B	95	SIZ[1]
16	GND	36	MEGTEST (spare)	56	RXD_A	76	OUT1_B	96	SIZ[0]
17	GND	37	GND	57	TXD_A	77	VCC	97	MEM_WR
18	DATA[7]	38	GND	58	CTS_A	78	VCC	98	FUNC[2]
19	DATA[6]	39	SB_CLK	59	RTS_A	79	GND	99	FUNC[1]
20	DATA[5]	40	GND	60	DCD_A	80	RI_B	100	FUNC[0]

100-Pin PQFP Pinout



100-Pin PQFP Package Dimensions





Dimensions in inches, dimensions in brackets in (millimeters).

ORDERING INFORMATION

Part Number	Description
STP2022PQFP	100-Pin Plastic Quad Flat Pack (PQFP)