

**DESCRIPTION**

The STP2024 System Logic Chip provides additional features for SBus based systems. It has two major logic blocks: an audio DMA controller and a glue logic block. The DMA controller consumes the bulk of the logic, providing 32-bit SBus DVMA and slave ports. It is designed to interface to a CODEC with an 8-bit interface, such as the CS4231 from Crystal Technologies, for system audio functions. The glue logic contains various useful system functions such as power management, SBus control and Boundary SCAN/JTAG capabilities.

The power management portion contains five read/write bits - each associated with output pins. The STP2024 effectively shuts down the system when not in use by putting the processor input a low power, standby mode. Once activity is detected, the system returns to normal operation. In addition, it can be used to control fan speed and power to the AC convenience outlet, CODEC and two general purpose ports.

**Features**

- Audio DMA Controller
- SBus Master device
- Power Management functions
- SBus Slot Select Decodes
- Dual SBus mastership for STP2000 (Master I/O Controller)
- Scan Chain Splice
- JTAG TAP

**Benefits**

- Independent Play and Capture pipeline channels, each with 21 bytes of buffering.
- Implementation meets SBus Specification B.0 at 25 MHz operation.
- Reduces overall system power consumption.
- Allows other SBus slaves to coexist in STP2024 address space.
- Return a sense of arbitration fairness to highly integrated I/O devices for a beneficial effect on I/O performance.
- Provides the ability to "splice" in an additional external scan chain into the STP2024's own scan chain.
- Test and diagnostic functionality via IEEE 1149.1 compliant internal and boundary scan controller.

## BLOCK AND APPLICATION DIAGRAMS

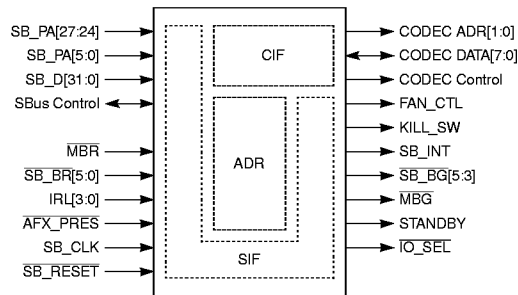


Figure 1. STP2024 Block Diagram

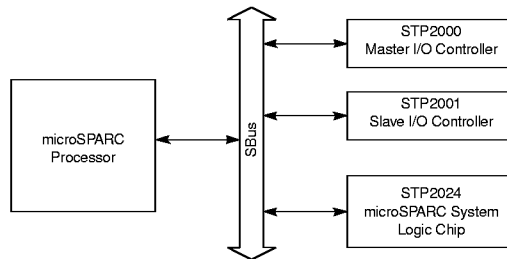


Figure 2. STP2024 Typical Application Diagram

## SIGNAL DESCRIPTIONS

Signal	Type	Description
SB_CLK	Input	SBus clock. The main clock to the STP2024. All internal flip-flops are clocked by this one clock.
SB_RESET	Input	SBus reset. The main reset to the STP2024. All internal flip-flops are synchronously reset by this input. The $\overline{\text{COD\_PDWN}}$ output is also forced low (active) by this input.
SB_DATA[31:0]	I/O	Bidirectional SBus data pins. This 32-bit bus provides the PIO and DVMA access path in and out of the STP2024.
SB_PA[27:24, 5:2]	Input	SBus Address input pins. Bits 27-24, in conjunction with SB_AS and SB_SEL provide STP2024 slot decodes. Selecting either Audio, Power Management, microSPARC II local bus functional blocks, or IO_SEL generic select output. Bits 5-2 provide specific register selection.
SB_AS	Input	SBus address strobe input pin. Registered asserted state of this signal along with SB_SEL indicates the STP2024 is selected for PIO operation.
SB_SEL	Output	SBus slave select. When asserted indicates the STP2024 slot has been selected.
SB_READ	I/O	Bidirectional SBus read/write pin. This pin indicates whether the current transfer is a read or a write operation.
SB_SIZ[2:0]	I/O	Bidirectional SBus transfer size description pins. These three bits describe (encoded) the size of the data transfer, of the current SBus operation.
SB_ACK[2:0]	I/O	Bidirectional SBus transfer acknowledgment pins. These three bits indicate an slave acknowledgment of the current SBus cycle by returning an encoded status.
SB_BR [4]	Output	SBus Bus Request. The STP2024's Audio DMA engine asserts this output whenever the playback pipeline needs to be filled or whenever the capture pipeline needs to be emptied. Assertion of this bit will cause de-assertion of the STANDBY bit.
SB_BG [4]	Input	SBus Bus Grant. This input pin indicates that the pending bus request has been granted.
SB_INT	Output	SBus interrupt. An open drain output. Asserted when playback or capture DMA engines need attention. Also asserted on STP2024 detected errors.
SB_BR [5, 3]	Output	SBus Bus Request. The STP2000 Master I/O dual bus master logic asserts either one of these bus request outputs whenever the MBR input is asserted. Note that SB_BR [3] is the primary output.
SB_BG [5, 3]	Input	SBus Bus Grant. These input pins indicates that the pending bus request has been granted. The STP2000 Master I/O dual bus master logic muxes through the proper grant to the MBG output.
MBR	Input	Master I/O Bus Request. SBus Bus Request from the STP2000 Master I/O. The STP2000 dual bus master logic asserts either SB_BR[5] or SB_BR[3] outputs whenever this input pin is asserted. Assertion of this bit will cause de-assertion of the STANDBY bit.
MBG	Output	Master I/O Bus Grant. STP2000 Master I/O dual bus master logic selects either SB_BG [5] or SB_BG [3] and muxes it through to this output pin.
SB_BR [2:0]	Input	SBus Bus Request. Assertion of any of these inputs will cause de-assertion of the STANDBY bit.
CPU_IR[3:0]	Input	Encode CPU interrupt lines. Assertion of any of these inputs will cause de-assertion of the STANDBY bit.

## SIGNAL DESCRIPTIONS (CONTINUED)

Signal	Type	Description
COD_DATA[7:0]	I/O	Codec Data bus. Byte wide, bidirectional data bus from/to the STP2024 from/to the Codec chip.
COD_PREQ	Input	Codec Play Request. This input indicates that the Codec is requesting data from the playback pipeline.
COD_CREQ	Input	Codec Capture Request. This input indicates that the Codec is requesting to send data to the capture pipeline.
COD_PACK	Output	Codec Playback Acknowledge. In response to a COD_PREQ this output indicates that play data will be written on the COD_DATA bus.
COD_CACK	Output	Codec Capture Acknowledge. In response to a COD_CREQ this output indicates that capture data will be sampled from the COD_DATA bus.
COD_PDWN	Output	Codec Power Down. This output places the Codec in reset/powerdown mode. Asserted by either CSR[5] or SB_RESET.
COD_CS	Output	Codec Chip Select. This output selects the Codec during PIO slave cycles.
COD_IOR	Output	Codec IO Read. This output indicates that the current operation to the Codec is a read.
COD_IOW	Output	Codec IO Write. This output indicates that the current operation to the Codec is a write.
COD_ADR[1:0]	Output	Codec Address. This output selects one of four 8-bit internal registers in the Codec during slave PIO cycles. These bits are directly driven from the SB_PA[3:2] input pins.
BPA	Output	Bit Port A. A generic output sourced from the PIO accessible BPA register.
BPB	Output	Bit Port B. A generic output sourced from the PIO accessible BPB register.
STANDBY	Output	Standby. A Power Management register output pin. Asserted by PIO write operations. De-asserted by any SB_BR or CPU_IR input.
KILL_COUTLET	Output	Kill Convenience Outlet. A Power Management register output pin. Asserted and de-asserted by PIO write operations
FAN_CTL	Output	Fan Control. A Power Management register output pin. Asserted and de-asserted by PIO write operations
TCK	Input	JTAG Clock. Test input clock for JTAG controller and scan registers.
TRSTN	Input	JTAG Reset pin.
TDI	Input	JTAG Data Input pin.
TDO	Output	JTAG Data Output pin.
TMS	Input	JTAG Mode Select input pin.
AFX_TDO	Input	An input pin from capable of receiving a JTAG scannable bit stream which can then be <i>spliced</i> into the STP2024's internal scan chain.
AFX_TDI	Output	An output pin which is either the STP2024's JTAG scan bit stream (if scan chain splice is active) or the generic bit port register, bpc.
AFX_PRESENT	Input	microSPARC-II local bus Present. An input pin which is PIO readable.
PNAND_OUT	Output	A series of serial connections of all STP2024 input and bidirectional pins, through NAND gates. Ends at this output pin. Used for test purposes only.

## ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings <sup>[1]</sup>

Symbol	Name	Rating	Units
V <sub>CC</sub>	Power supply voltage	+7.0	V
V <sub>IN</sub>	Input voltage (any pin)	GND ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>	V
P <sub>D</sub>	Power dissipation	500	mW
T <sub>J</sub>	Operating junction temperature	0 to +105	°C
T <sub>S</sub>	Storage temperature	-40 to +125	°C
	Static Discharge Voltage	2000	V

1. Operation of the device at values in excess of those listed above will result in degradation or destruction of the device. All voltages are defined with respect to ground. Functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### Recommended Operating Conditions

Symbol	Name	Min	Nom	Max	Units
V <sub>CC</sub>	Supply Voltage	4.75	5.0	5.25	V
V <sub>IN</sub>	DC input voltage	0	–	V <sub>CC</sub>	V
P <sub>D</sub>	Power dissipation	–	370	500	mW
T <sub>A</sub>	Operating Free-Air Temperature	0	–	70	°C

### Capacitance

Symbol	Description	PQCL Max	Units
C <sub>IN</sub>	Input Capacitance	3	pF
C <sub>OUT</sub>	Output Capacitance	2.7	pF
C <sub>BI</sub>	Bidirectional Capacitance	3	pF

**DC Characteristics ( $V_{CC} = 5.0V \pm 5\%$ )**

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$V_{IH}$	Minimum High Level Input Voltage		2.0	–	–	V
$V_{IL}$	Maximum Low Level Input Voltage		–	–	0.8	V
$V_{OH}$	Minimum High Level Output Voltage	$I_{OH} = -4.0 \text{ mA}, V_{CC} = \text{min},$ $I_{OH} = -6.0 \text{ mA}, V_{CC} = \text{min},$ [1] $I_{OH} = -8.0 \text{ mA}, V_{CC} = \text{min},$ [2]	2.4	4.5	–	V V V
$V_{OL}$	Minimum High Level Output Voltage	$I_{OL} = 4.0 \text{ mA}, V_{CC} = \text{min},$ $I_{OL} = 6.0 \text{ mA}, V_{CC} = \text{min},$ [1] $I_{OL} = 8.0 \text{ mA}, V_{CC} = \text{min},$ [2]	–	0.2	0.4	V V V
$I_{IN}$	Minimum Input Current	$V_{IN} = V_{CC} \text{ or GND}$	-10	–	+10	$\mu\text{A}$
$I_{OZ}$	Maximum Output Leakage Current	$V_{OUT} = V_{CC} \text{ or GND}$ Output Disabled	-10	–	+10	$\mu\text{A}$

1. SB\_INT\_1 output only.

2. SB\_DATA[31:0], SB\_SIZ[2:0], SB\_ACK[2:0], SB\_READ outputs only.

**AC Characteristics: Input Pins**

Signal	Parameter	Conditions	Reference Edge	Min	Max	Unit
SB_CLK	t <sub>CLK</sub>			16	25	MHz
	t <sub>CH</sub>			17	–	ns
	t <sub>CL</sub>			17	–	ns
	t <sub>CR</sub>			1	3	ns
	t <sub>CF</sub>			1	3	ns
TCK	t <sub>CH</sub>	JTAG_CLK		25	–	ns
	t <sub>CL</sub>	T <sub>CYC</sub> >=100ns		25	–	ns
	t <sub>CR</sub>			–	10	ns
	t <sub>CF</sub>			–	10	ns
SB_RESET	t <sub>S</sub>		SB_CLK+	15	–	ns
	t <sub>HI</sub>		SB_CLK+	–	1	ns
TRSTN	t <sub>S</sub>	2 cycles	TCK+	10	–	ns
	t <sub>HI</sub>		TCK+	0	–	ns
TDI	t <sub>S</sub>		TCK+	10	–	ns
	t <sub>HI</sub>		TCK+	0	–	ns
TMS	t <sub>S</sub>		TCK+	10	–	ns
	t <sub>HI</sub>		TCK+	0	–	ns
AFX_TDO	t <sub>S</sub>		TCK+	10	–	ns
	t <sub>HI</sub>		TCK+	0	–	ns
AFX_PRESENT		DC level		N/A	N/A	ns
SB_PA[27:24, 5:2]	t <sub>S</sub>		SB_CLK+	15	–	ns
	t <sub>HI</sub>		SB_CLK+	–	1	ns
SB_AS	t <sub>S</sub>		SB_CLK+	15	–	ns
	t <sub>HI</sub>		SB_CLK+	–	1	ns
SB_SEL	t <sub>S</sub>		SB_CLK+	15	–	ns
	t <sub>HI</sub>		SB_CLK+	–	1	ns
SB_BR [2:0]	t <sub>S</sub>		SB_CLK+	15	–	ns
	t <sub>HI</sub>		SB_CLK+	–	1	ns
SB_BG [5:3]	t <sub>S</sub>		SB_CLK+	15	–	ns
	t <sub>HI</sub>		SB_CLK+	–	1	ns
CPU_IR[3:0]	t <sub>S</sub>		SB_CLK+	15	–	ns
	t <sub>HI</sub>		SB_CLK+	–	1	ns
MBR	t <sub>S</sub>		SB_CLK+	15	–	ns
	t <sub>HI</sub>		SB_CLK+	–	1	ns
COD_PREQ	t <sub>S</sub>		SB_CLK+	N/A	N/A	ns
	t <sub>HI</sub>		SB_CLK+			ns
COD_CREQ	t <sub>S</sub>		SB_CLK+	N/A	N/A	ns
	t <sub>HI</sub>		SB_CLK+			ns

**AC Characteristics: Bidirectional Pins**

Signal	Parameter	Conditions	Reference Edge	Min	Max	Unit
SB_DATA[31:0]	t <sub>DO</sub>	70C, 4.75V, 100pf	SB_CLK+	–	22.5	ns
	t <sub>HO</sub>	0C, 5.25V, 100pf	SB_CLK+	5.4	–	ns
	t <sub>SI</sub>		SB_CLK+	15	–	ns
	t <sub>HI</sub>		SB_CLK+	–	1	ns
SB_SIZ[2:0]	t <sub>DO</sub>	70C, 4.75V, 100pf	SB_CLK+	–	20.9	ns
	t <sub>HO</sub>	0C, 5.25V, 100pf	SB_CLK+	5.6	–	ns
	t <sub>SI</sub>		SB_CLK+	15	–	ns
	t <sub>HI</sub>		SB_CLK+	–	1	ns
SB_READ	t <sub>DO</sub>	70C, 4.75V, 100pf	SB_CLK+	–	20.6	ns
	t <sub>HO</sub>	0C, 5.25V, 100pf	SB_CLK+	4.7	–	ns
	t <sub>SI</sub>		SB_CLK+	15	–1	ns
	t <sub>HI</sub>		SB_CLK+	–	–	ns
SB_ACK[2:0]	t <sub>DO</sub>	70C, 4.75V, 100pf	SB_CLK+	–	20	ns
	t <sub>HO</sub>	0C, 5.25V, 100pf	SB_CLK+	5.0	–	ns
	t <sub>SI</sub>		SB_CLK+	15	–	ns
	t <sub>HI</sub>		SB_CLK+	–	1	ns
COD_DATA[7:0]	t <sub>DO</sub>	70C, 4.75V, 15pf	SB_CLK+	–	10.7	ns
	t <sub>HO</sub>	0C, 5.25V, 15pf	SB_CLK+	–	–	ns
	t <sub>SI</sub>		COD_IOW	22	–	ns
	t <sub>HI</sub>		COD_IOW	–	0	ns



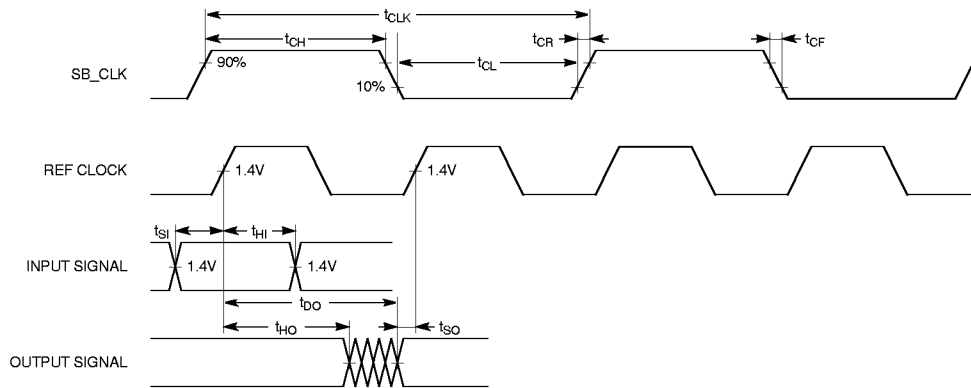
**AC Characteristics: Output Pins**

Signal	Parameter	Conditions	Reference Edge	Min	Max	Unit
SB_BR[4]	t <sub>DO</sub>	70C, 4.75V, 60pf	SB_CLK+	–	21	ns
	t <sub>HO</sub>	70C, 4.75V, 60pf	SB_CLK+	5.5	–	ns
SB_BR[5, 3]	t <sub>DO</sub>	70C, 4.75V, 20pf	SB_CLK+	–	20.7	ns
	t <sub>HO</sub>	70C, 4.75V, 20pf	SB_CLK+	2.5	–	ns
	t <sub>DO</sub>	70C, 5.0V, 20pf	MBR̄	–	7.6	ns
MBG	t <sub>DO</sub>	70C, 4.75V, 20pf	SB_CLK+	–	20	ns
	t <sub>HO</sub>	70C, 4.75V, 20pf	SB_CLK+	3.4	–	ns
	t <sub>DO</sub>	70C, 5.0V, 20pf	SB_BḠ [5,3]	–	7.6	ns
SB_INT	t <sub>DO</sub>	70C, 4.75V, 100pf, L-H	SB_CLK+	–	12.3	ns
		70C, 4.75V, 100pf, H-L	SB_CLK+	–	21.5	ns
	t <sub>HO</sub>	0C, 5.25V, 100pf, L-H	SB_CLK+	4.0	–	ns
		0C, 5.25V, 100pf, H-L	SB_CLK+	6.3	–	ns
BPA	t <sub>DO</sub>	70C, 4.75V, 15pf	SB_CLK+	–	13	ns
	t <sub>HO</sub>	0C, 5.25V, 15pf	SB_CLK+	4.0	–	ns
BPB	t <sub>DO</sub>	70C, 4.75V, 15pf	SB_CLK+	–	13	ns
	t <sub>HO</sub>	0C, 5.25V, 15pf	SB_CLK+	4.0	–	ns
STANDBY	t <sub>DO</sub>	70C, 4.75V, 15pf	SB_CLK+	–	13	ns
	t <sub>HO</sub>	0C, 5.25V, 15pf	SB_CLK+	4.2	–	ns
KILL_COUTLET	t <sub>DO</sub>	70C, 4.75V, 30pf	SB_CLK+	–	13	ns
	t <sub>HO</sub>	0C, 5.25V, 30pf	SB_CLK+	4.0	–	ns
FAN_CTL	t <sub>DO</sub>	70C, 4.75V, 30pf	SB_CLK+	–	13	ns
	t <sub>HO</sub>	0C, 5.25V, 30pf	SB_CLK+	4.2	–	ns
IO_SEL	t <sub>DO</sub>	70C, 4.75V, 15pf	SB_PA[27:25]	–	9.9	ns
	t <sub>HO</sub>	0C, 5.25V, 15pf	SB_PA[27:25]	3.7	–	ns
AFX_TDI	t <sub>DO</sub>	70C, 4.75V, 15pf	SB_CLK+	–	13	ns
	t <sub>HO</sub>	0C, 5.25V, 15pf	SB_CLK+	4.1	–	ns
TDO	t <sub>DO</sub>	70C, 4.75V, 15pf	TCK+	–	–	ns
	t <sub>HO</sub>	0C, 5.25V, 15pf	TCK+	8.3	–	ns
PNAND_OUT	t <sub>DO</sub>	70C, 4.75V, 15pf	SB_READ+	–	200.6	ns
	t <sub>HO</sub>	0C, 5.25V, 15pf	SB_READ+	–	–	ns
COD_CS	t <sub>DO</sub>	70C, 4.75V, 15pf	SB_CLK+	–	12.5	ns
	t <sub>HO</sub>	0C, 5.25V, 15pf	SB_CLK+	4.0	–	ns
COD_ADR[1:0]	t <sub>DO</sub>	70C, 4.75V, 15pf	SB_PA[3:2]	–	8.4	ns
	t <sub>HO</sub>	0C, 5.25V, 15pf	SB_PA[3:2]	2.3	–	ns
COD_IOW	t <sub>DO</sub>	70C, 4.75V, 15pf	SB_CLK+	–	14.8	ns
	t <sub>HO</sub>	0C, 5.25V, 15pf	SB_CLK+	4.4	–	ns
COD_IOR	t <sub>DO</sub>	70C, 4.75V, 15pf	SB_CLK+	–	15.1	ns
	t <sub>HO</sub>	0C, 5.25V, 15pf	SB_CLK+	4.4	–	ns

**AC Characteristics: Output Pins (Continued)**

Signal	Parameter	Conditions	Reference Edge	Min	Max	Unit
COD_PACK	t <sub>DO</sub>	70C, 4.75V, 15pf	SB_CLK+	–	13.8	ns
	t <sub>HO</sub>	0C, 5.25V, 15pf	SB_CLK+	4.0	–	ns
COD_CACK	t <sub>DO</sub>	70C, 4.75V, 15pf	SB_CLK+	–	13.8	ns
	t <sub>HO</sub>	0C, 5.25V, 15pf	SB_CLK+	4.0	–	ns
COD_PDWN	t <sub>DO</sub>	70C, 4.75V, 15pf	SB_CLK+	–	12.7	ns
	t <sub>HO</sub>	0C, 5.25V, 15pf	SB_CLK+	4.4	–	ns

## TIMING DIAGRAMS



### Parameter Definitions

- $t_{SI}$  : Required setup time of a chip input referenced to a given (clock) edge.
- $t_{HI}$  : Required hold time of a chip input referenced to a given (clock) edge.
- $t_{HO}$  : Guaranteed hold time of an output referenced to a given (clock) edge.
- $t_{SO}$  : Guaranteed setup time of an output referenced to a next given (clock) edge.
- $t_{DO}$  : Guaranteed propagation time of an output referenced to a given (clock) edge.
- $t_{CH}$  : Required clock high time.
- $t_{CL}$  : Required clock low time.
- $t_{CR}$  : Required clock rise time.
- $t_{CF}$  : Required clock fall time.

**Figure 3. Clock & I/O Waveforms**

## PACKAGING INFORMATION

### 120-Pin PQFP Pin Assignment

Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name
1	SB_DATA[24]	31	GND	61	V <sub>CC</sub>	91	SB_DATA[0]
2	SB_DATA[25]	32	SB_AS	62	COD_PDWN	92	SB_DATA[1]
3	SB_DATA[26]	33	SB_SEL	63	COD_PREQ	93	SB_DATA[2]
4	SB_DATA[27]	34	SB_BR[4]	64	COD_CREQ	94	SB_DATA[3]
5	SB_DATA[28]	35	SB_BG[3]	65	COD_IOW	95	SB_DATA[4]
6	SB_DATA[29]	36	SB_BG[5]	66	COD_IOR	96	SB_DATA[5]
7	V <sub>CC</sub>	37	MBG	67	COD_PACK	97	SB_DATA[6]
8	GND	38	SB_BR[0]	68	COD_CACK	98	SB_DATA[7]
9	SB_DATA[30]	39	SB_BR[1]	69	COD_CS	99	SB_DATA[8]
10	SB_DATA[31]	40	SB_BR[2]	70	MBR	100	SB_DATA[9]
11	SB_ACK[2]	41	SB_BR[3]	71	IO_SEL	101	V <sub>CC</sub>
12	SB_ACK[1]	42	SB_BR[5]	72	BPA	102	GND
13	SB_ACK[0]	43	SB_INT	73	STANDBY	103	GND
14	GND	44	COD_ADR[0]	74	FAN_CTL	104	SB_DATA[10]
15	SB_SIZ[2]	45	COD_ADR[1]	75	GND	105	SB_DATA[11]
16	SB_SIZ[1]	46	COD_DATA[0]	76	GND	106	SB_DATA[12]
17	SB_SIZ[0]	47	GND	77	V <sub>CC</sub>	107	SB_DATA[13]
18	SB_PA[27]	48	GND	78	KILL_COUT	108	SB_DATA[14]
19	SB_PA[26]	49	V <sub>CC</sub>	79	BPB	109	SB_DATA[15]
20	SB_PA[25]	50	COD_DATA[1]	80	TDI	110	SB_DATA[16]
21	SB_PA[24]	51	COD_DATA[2]	81	TCK	111	SB_DATA[17]
22	SB_PA[5]	52	COD_DATA[3]	82	TMS	112	SB_DATA[18]
23	SB_PA[4]	53	COD_DATA[4]	83	TDO	113	SB_DATA[19]
24	SB_PA[3]	54	COD_DATA[5]	84	AFX_TDO	114	V <sub>CC</sub>
25	SB_PA[2]	55	COD_DATA[6]	85	AFX_TDI	115	GND
26	PNAND_OUT	56	COD_DATA[7]	86	AFX_PRES	116	SB_DATA[20]
27	TRSTN	57	CPU_IR3	87	SB_RESET	117	SB_DATA[21]
28	SB_READ	58	CPU_IR2	88	SB_CLK	118	SB_DATA[22]
29	BS_BG[4]	59	CPU_IR1	89	V <sub>CC</sub>	119	SB_DATA[23]
30	V <sub>CC</sub>	60	CPU_IR0	90	V <sub>CC</sub>	120	V <sub>CC</sub>

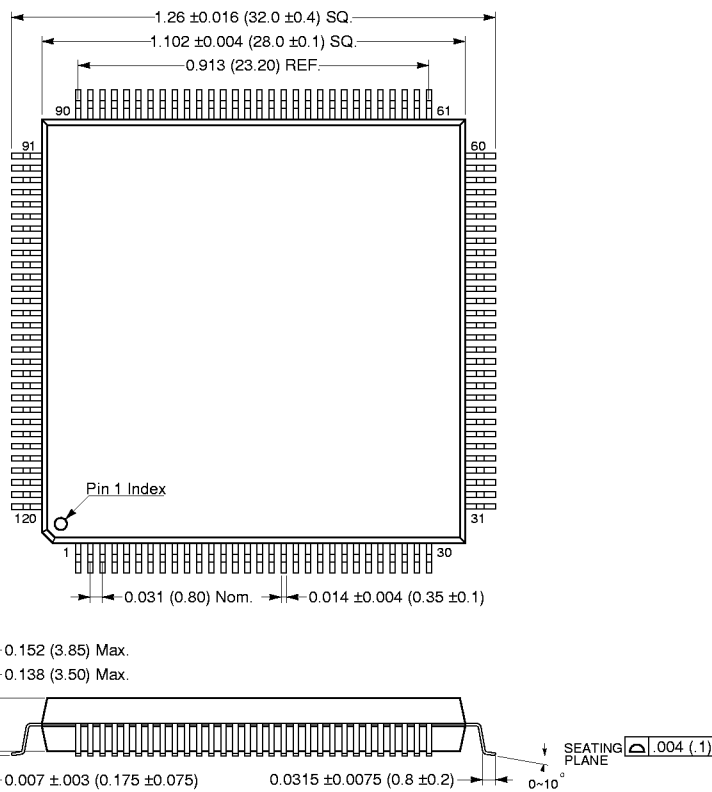
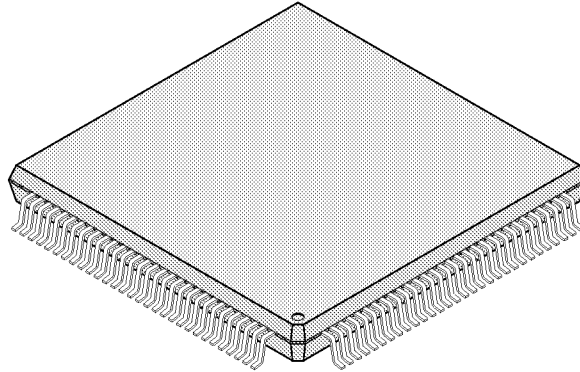
120-Pin PQFP Package Pinout

SB_DATA[24]	1	SB_DATA[90]	VCC
SB_DATA[25]	2	SB_DATA[91]	91
SB_DATA[26]	3	SB_DATA[92]	92
SB_DATA[27]	4	SB_DATA[93]	93
SB_DATA[28]	5	SB_DATA[94]	94
SB_DATA[29]	6	SB_DATA[95]	95
VCC	7	SB_DATA[96]	96
GND	8	SB_DATA[97]	97
SB_DATA[30]	9	SB_DATA[98]	98
SB_DATA[31]	10	SB_DATA[99]	99
SB_ACK[2]	11	SB_DATA[100]	100
SB_ACK[1]	12	VCC	101
SB_ACK[0]	13	GND	102
GND	14	GND	103
SB_SIZ[2]	15	SB_DATA[104]	104
SB_SIZ[1]	16	SB_DATA[105]	105
SB_SIZ[0]	17	SB_DATA[106]	106
SB_PA[27]	18	SB_DATA[107]	107
SB_PA[26]	19	SB_DATA[108]	108
SB_PA[25]	20	SB_DATA[109]	109
SB_PA[24]	21	SB_DATA[110]	110
SB_PA[5]	22	SB_DATA[111]	111
SB_PA[4]	23	SB_DATA[112]	112
SB_PA[3]	24	SB_DATA[113]	113
SB_PA[2]	25	VCC	114
FNAND_OU	26	GND	115
TRSTN	27	SB_DATA[116]	116
SB_READ	28	SB_DATA[117]	117
BS_BG4	29	SB_DATA[118]	118
VCC	30	SB_DATA[119]	119
		VCC	120
		60	CPU_IR[0]
		59	CPU_IR[1]
		58	CPU_IR[2]
		57	CPU_IR[3]
		56	COD_DATA[7]
		55	COD_DATA[6]
		54	COD_DATA[5]
		53	COD_DATA[4]
		52	COD_DATA[3]
		51	COD_DATA[2]
		50	COD_DATA[1]
		49	VCC
		48	GND
		47	GND
		46	COD_ADR[2]
		45	COD_ADR[1]
		44	COD_ADR[0]
		43	SB_INT
		42	SB_BR[5]
		41	SB_BR[3]
		40	SB_BR[2]
		39	SB_BR[1]
		38	SB_BR[0]
		37	MBG
		36	SB_BG[5]
		35	SB_BG[3]
		34	SB_BR[4]
		33	SB_SEL
		32	SB_AS
		31	GND
		61	VCC
		62	COD_PDWN
		63	COD_PREG
		64	COD_CREG
		65	COD_IOW
		66	COD_IOR
		67	COD_PACK
		68	COD_CACK
		69	COD_CS
		70	MBR
		71	IO_SEL
		72	BPA
		73	STANDBY
		74	FAN_CTL
		75	GND
		76	GND
		77	VCC
		78	KILL_COUT
		79	BPB
		80	TDI
		81	TCK
		82	TMS
		83	TDO
		84	AFX_TDO
		85	AFX_TDI
		86	AFX_PRES
		87	SB_RESET
		88	SB_CLK
		89	VCC
		90	VCC

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### 120-Pin PQFP Package Dimensions



Dimensions in inches, dimensions in brackets in (millimeters).

*APC*  
*System Logic Chip*

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## ORDERING INFORMATION

Part Number	Description
STP1024PQFP	120-Pin Plastic Quad Flat Pack (PQFP)

Document Part Number: STP2024