STANSON

STP2327

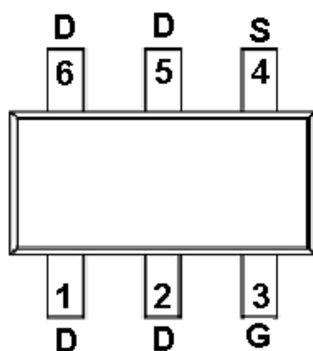
P Channel Enhancement Mode MOSFET

-1.5A

DESCRIPTION

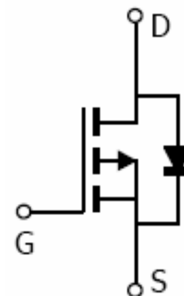
STP2327 is the P-Channel logic enhancement mode power field effect transistor which is produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management, other battery powered circuits, and low in-line power loss are required. The product is in a very small outline surface mount package.

PIN CONFIGURATION
SOT-23-6L

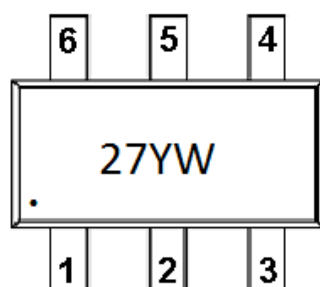


FEATURE

- -100V/-1.5.0A, $R_{DS(ON)}$ = 520m-ohm (Typ.) @VGS = -10V
- -100V/-0.5.0A, $R_{DS(ON)}$ = 600m-ohm @VGS = -4.5V
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- SOT-23-6L package design



PART MARKING



Y: Year Code   A: date Code

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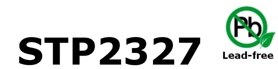
120 Bentley Square, Mountain View, Ca 94040 USA
www.stansontech.com



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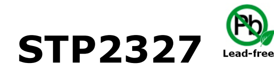
ABSOULTE MAXIMUM RATINGS (Ta = 25℃ Unless otherwise noted)

Parameter		Symbol	Typical	Unit
Drain-Source Voltage		V_{DSS}	-100	V
Gate-Source Voltage		V_{GSS}	±20	V
Continuous Drain CurrentTJ=150℃)	T_A=25℃ T_A=70℃	I_D	-1.5 -1.2	A
Pulsed Drain Current		I_{DM}	-4.5	A
Continuous Source Current (Diode Conduction)		I_S	-1.0	A
Power Dissipation	T_A=25℃ T_A=70℃	P_D	1.25 0.8	W
Operation Junction Temperature		T_J	150	℃
Storgae Temperature Range		T_{STG}	-55/150	℃
Thermal Resistance-Junction to Ambient		$R_{\theta JA}$	100	℃/W



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ELECTRICAL CHARACTERISTICS (Ta = 25℃ Unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V,I_D=-250uA	-100			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=VGS,I_D=-250uA	-1.0		-2.5	V
Gate Leakage Current	I_{GSS}	V_{DS}=0V,V_{GS}=±20V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-80V,V_{GS}=0V			-1	uA
		V_{DS}=-80V,V_{GS}=0V T_J=55℃			-5	
Drain-source On-Resistance	$R_{DS(on)}$	V_{GS}=-10V,I_D=-0.8A V_{GS}=-4.5V,I_D=-0.4A		0.520 0.600	0.640 0.700	Ω
Forward Transconductance	g_{fs}	V_{DS}=-10V,I_D=-1.0A		2.9		S
Diode Forward Voltage	V_{SD}	I_S=-1.0A,V_{GS}=0V			-1.0	V
Dynamic						
Total Gate Charge	Q_g	V_{DS}=-50V V_{GS}=-10V I_D≡-1.0A		10		nC
Gate-Source Charge	Q_{gs}			1.75		
Gate-Drain Charge	Q_{gd}			1.25		
Input Capacitance	C_{iss}	V_{DS}=-15V V_{GS}=0V F=1MHz		553		pF
Output Capacitance	C_{oss}			29		
Reverse Transfer Capacitance	C_{rss}			20		
Turn-On Time	$t_{d(on)}$	V_{DD}=-50V R_L=3.3Ω I_D=-0.5A V_{GS}=-10V R_G=3.5Ω		2		nS
	t_r			19		
Turn-Off Time	$t_{d(off)}$			20		
	t_f			19		

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TYPICAL CHARACTERISTICS

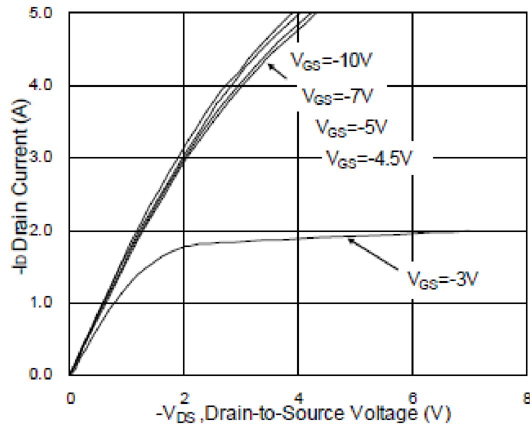


Fig 1 Output Characteristics

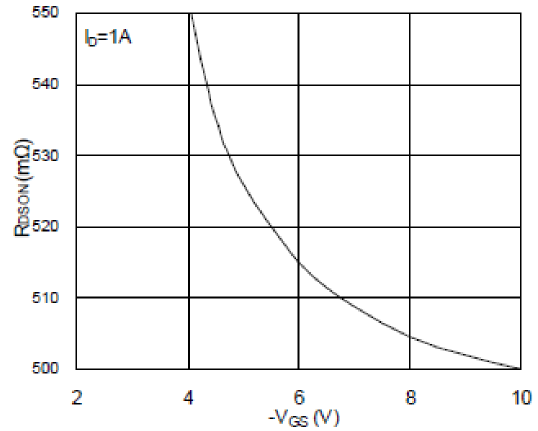


Fig. 2 On-Resistance vs Gate Source Voltage

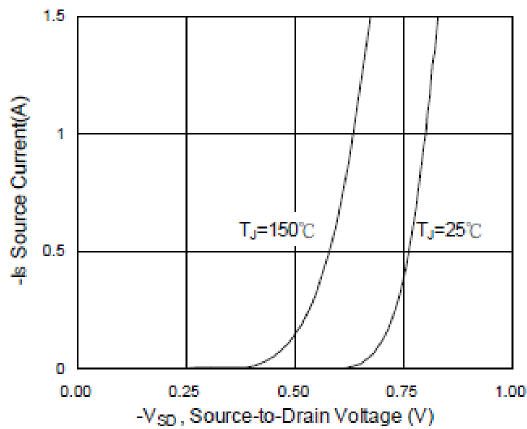


Fig 3 Source-Drain Forward Voltage

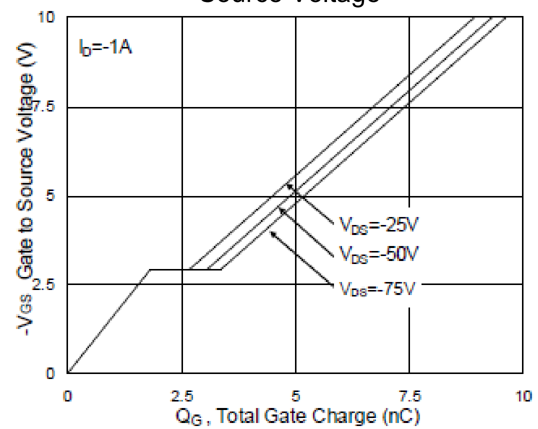


Fig. 4 Gate Charge

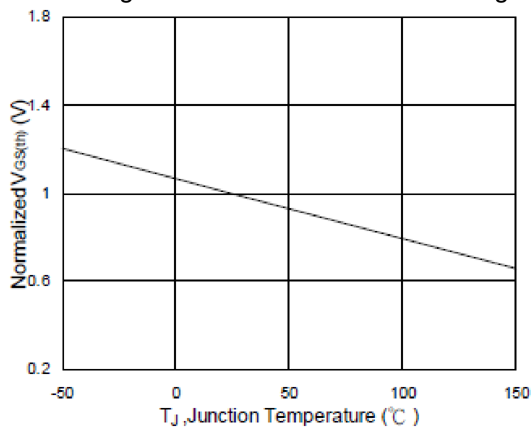


Fig. 5 Gate Voltage vs Junction temperature

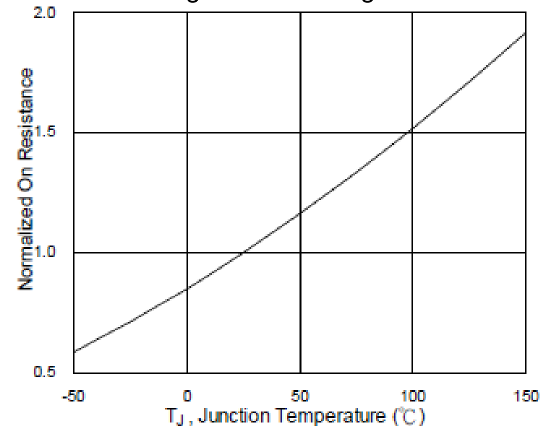
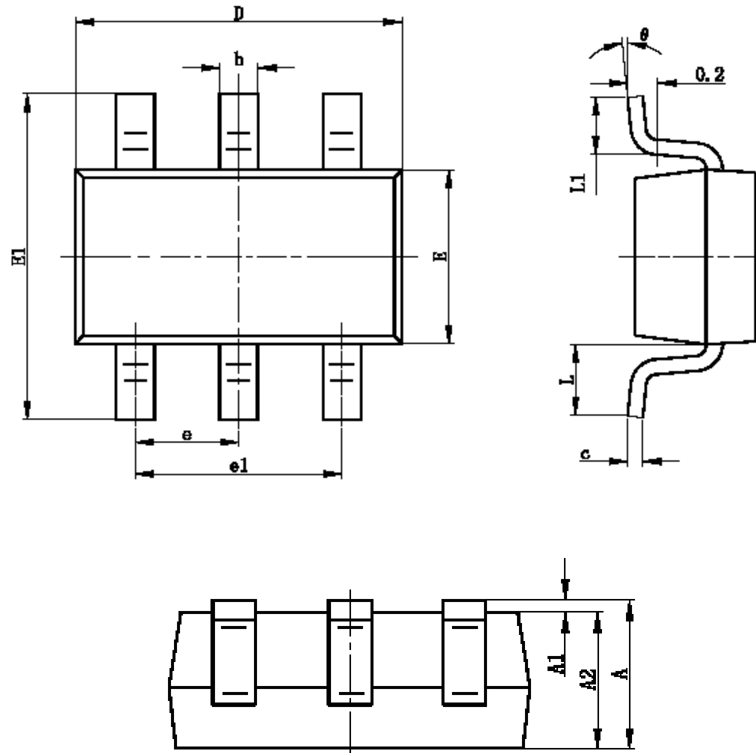


Fig. 6 On-Resistance vs Junction

SOT-23-6L PACKAGE OUTLINE



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.400	0.012	0.016
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950TYP		0.037TYP	
e1	1.800	2.000	0.071	0.079
L	0.700REF		0.028REF	
L1	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°