



STP30NS15LFP

N-CHANNEL 150V - 0.085 Ω - 10A TO-220FP
MESH OVERLAY™ POWER MOSFET

TYPE	V _{DSS}	R _{DS(on)}	I _D
STP30NS15LFP	150 V	<0.1 Ω	10 A

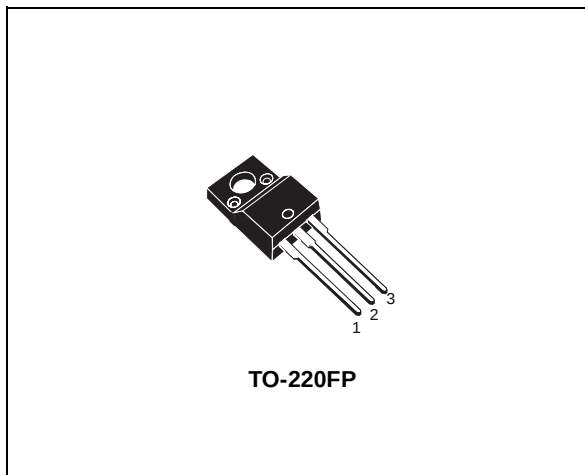
- TYPICAL R_{DS(on)} = 0.085 Ω
- EXTREMELY HIGH dv/dt CAPABILITY
- 100% AVALANCHE TESTED

DESCRIPTION

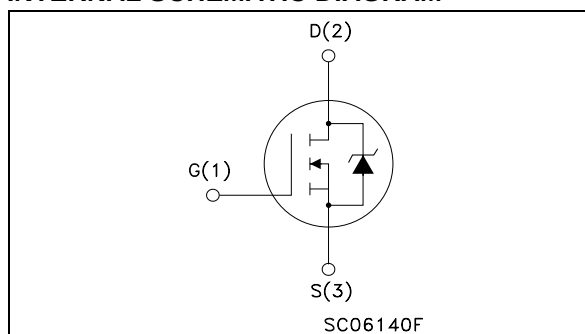
Using the latest high voltage MESH OVERLAY™ process, STMicroelectronics has designed an advanced family of power MOSFETs with outstanding performances. The new patent pending strip layout coupled with the Company's proprietary edge termination structure, gives the lowest R_{DS(on)} per area, exceptional avalanche and dv/dt capabilities and unrivalled gate charge and switching characteristics.

APPLICATIONS

- SWITCHING "S" CAPACITOR



INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source Voltage (V _{GS} = 0)	150	V
V _{DGR}	Drain-gate Voltage (R _{GS} = 20 k Ω)	150	V
V _{GS}	Gate- source Voltage	± 15	V
I _D	Drain Current (continuous) at T _C = 25°C	10	A
I _D	Drain Current (continuous) at T _C = 100°C	7	A
I _{DM} (●)	Drain Current (pulsed)	40	A
P _{tot}	Total Dissipation at T _C = 25°C	30	W
	Derating Factor	0.2	W/°C
E _{AS} (1)	Single Pulse Avalanche Energy	300	mJ
dv/dt (2)	Peak Diode Recovery voltage slope	2.4	V/ns
T _{stg}	Storage Temperature	-55 to 175	°C
T _j	Operating Junction Temperature		

(●) Pulse width limited by safe operating area.

(1) Starting T_j = 25 °C, I_D = 15A, V_{DD} = 75V

(2) I_{SD} $\leq$ 35A, di/dt $\leq$ 300A/ μ s, V_{DD} $\leq$ V_{(BR)DSS}, T_j $\leq$ T_{JMAX}.

STP30NS15LFP

THERMAL DATA

R _{thj-case}	Thermal Resistance Junction-case	Max	5	°C/W
R _{thj-amb}	Thermal Resistance Junction-ambient	Max	62.5	°C/W
T _I	Maximum Lead Temperature For Soldering Purpose	Typ	300	°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25 °C unless otherwise specified)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source Breakdown Voltage	I _D = 250 µA, V _{GS} = 0	150			V
I _{DSS}	Zero Gate Voltage Drain Current (V _{GS} = 0)	V _{DS} = Max Rating V _{DS} = Max Rating T _C = 125°C			1 10	µA µA
I _{GSS}	Gate-body Leakage Current (V _{DS} = 0)	V _{GS} = ± 15V			±100	nA

ON (1)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} I _D = 250 µA	1	2	3	V
R _{DS(on)}	Static Drain-source On Resistance	V _{GS} = 10 V I _D = 5 A V _{GS} = 5 V I _D = 5 A		0.085 0.1	0.1 0.112	Ω Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g _{fs} (*)	Forward Transconductance	V _{DS} = 20 V I _D = 7 A		6		S
C _{iss} C _{oss} C _{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V _{DS} = 25V, f = 1 MHz, V _{GS} = 0		1080 170 105		pF pF pF

ELECTRICAL CHARACTERISTICS (continued)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on Delay Time Rise Time	$V_{DD} = 75\text{ V}$ $I_D = 5\text{ A}$ $R_G = 4.7\ \Omega$ $V_{GS} = 4.5\text{ V}$ (Resistive Load, Figure 1)		25 95		ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	$V_{DD}=120\text{V}$ $I_D=10\text{A}$ $V_{GS}=5\text{V}$ (see test circuit, Figure 2)		40 7.5 20	54	nC nC nC

SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$ t_f	Turn-off Delay Time Fall Time	$V_{DD} = 75\text{ V}$ $I_D = 5\text{ A}$ $R_G = 4.7\ \Omega$, $V_{GS} = 5\text{ V}$ (Resistive Load, Figure 1)		55 30		ns ns
$t_r(v_{off})$ t_f t_c	Off-voltage Rise Time Fall Time Cross-over Time	$V_{clamp} = 120\text{ V}$ $I_D = 10\text{ A}$ $R_G = 4.7\ \Omega$, $V_{GS} = 4.5\text{ V}$ (Inductive Load, Figure 3)		15 30 50		ns ns ns

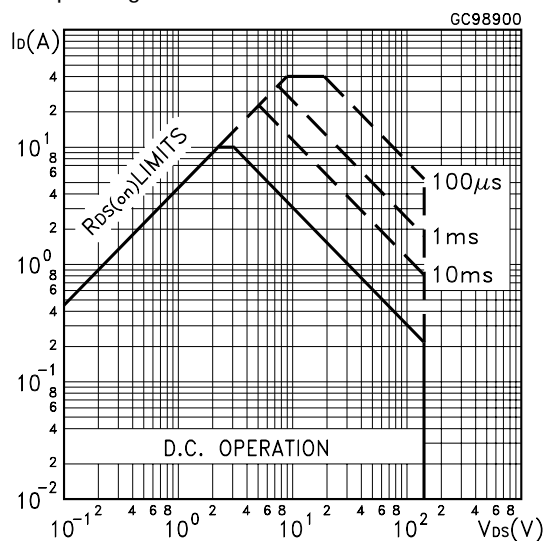
SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} $I_{SDM}(\bullet)$	Source-drain Current Source-drain Current (pulsed)				10 40	A A
V_{SD}^*	Forward On Voltage	$I_{SD} = 10\text{ A}$ $V_{GS} = 0$			1.3	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 10\text{ A}$ $di/dt = 100\text{ A}/\mu\text{s}$ $V_r = 30\text{ V}$ $T_J = 150^\circ\text{C}$ (Inductive Load, Figure 3)		160 950 12		ns nC A

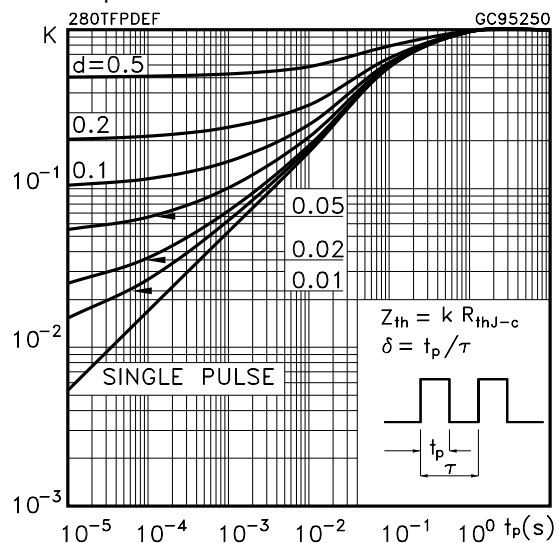
(*) Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %.

(•) Pulse width limited by safe operating area.

Safe Operating Area

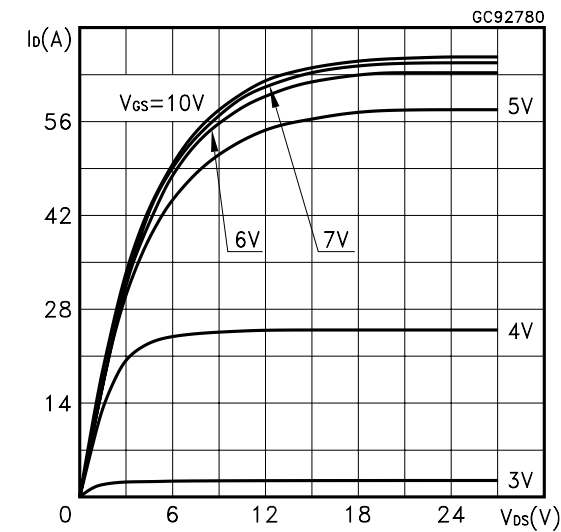


Thermal Impedance

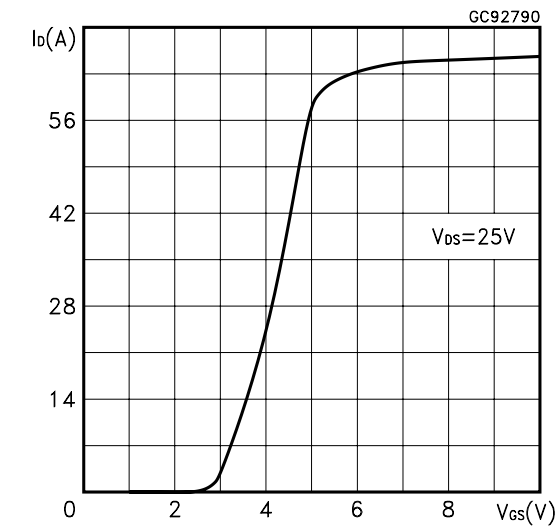


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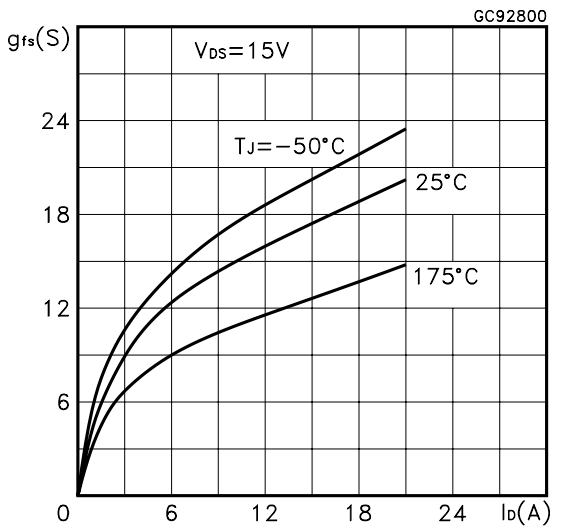
Output Characteristics



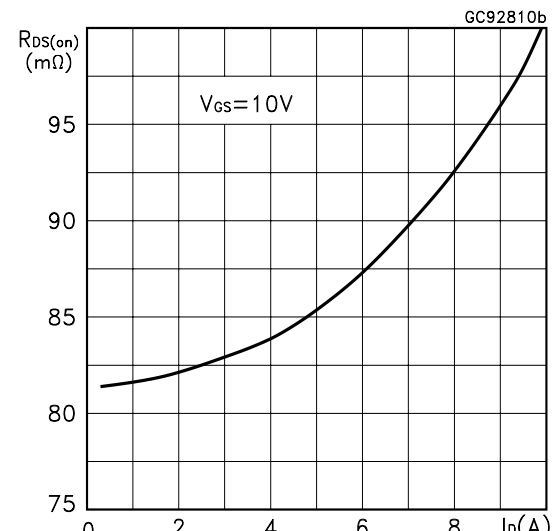
Transfer Characteristics



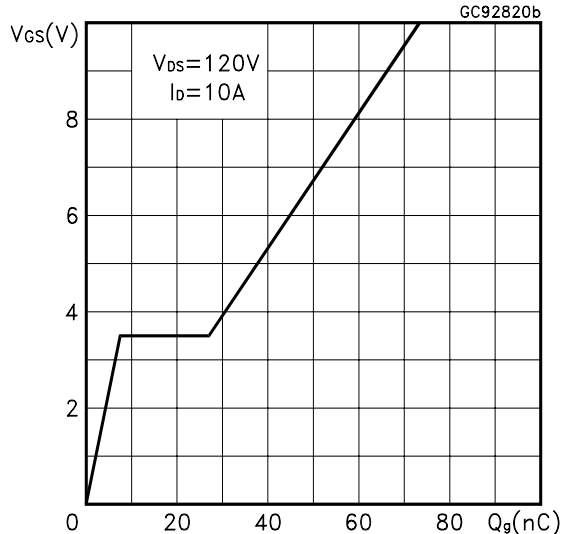
Transconductance



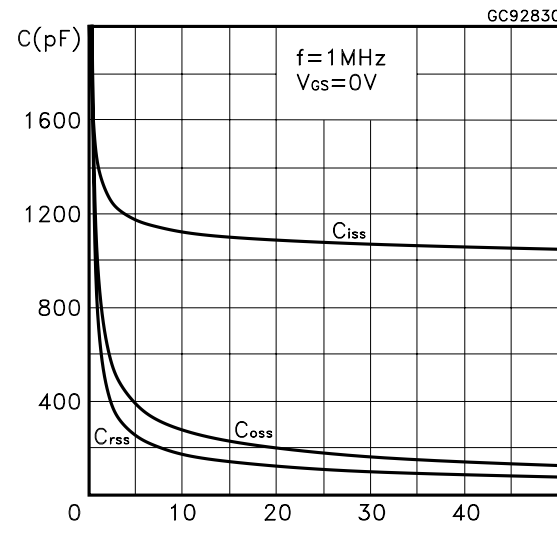
Static Drain-source On Resistance



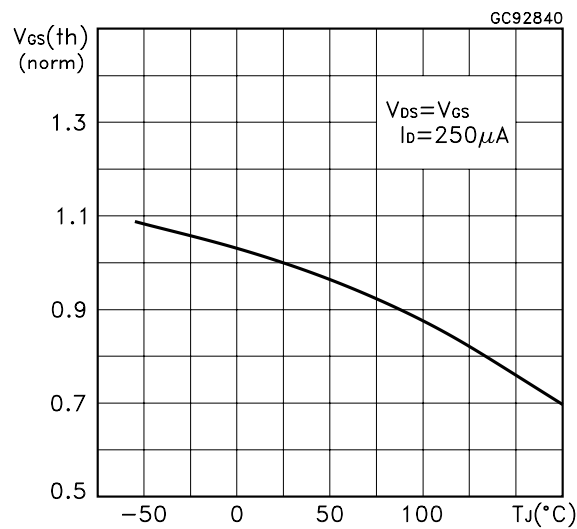
Gate Charge vs Gate-source Voltage



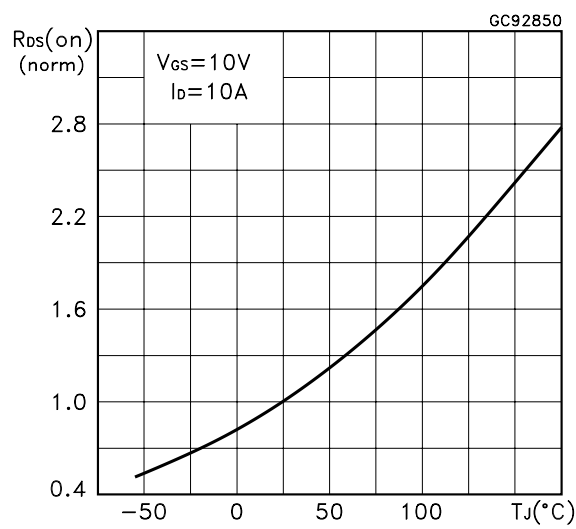
Capacitance Variations



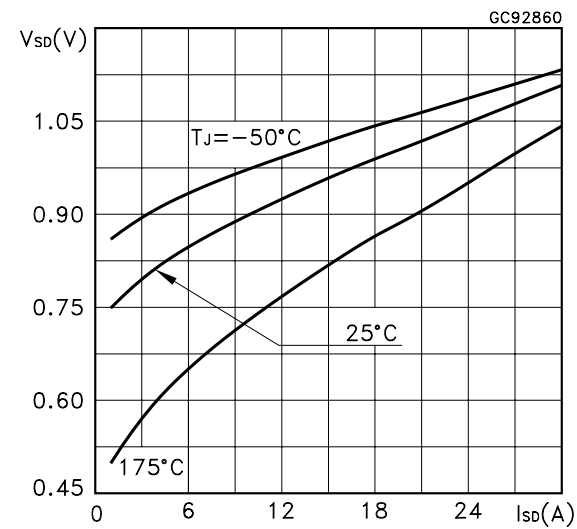
Normalized Gate Threshold Voltage vs Temperature



Normalized on Resistance vs Temperature



Source-drain Diode Forward Characteristics



Normalized Breakdown Voltage vs Temperature

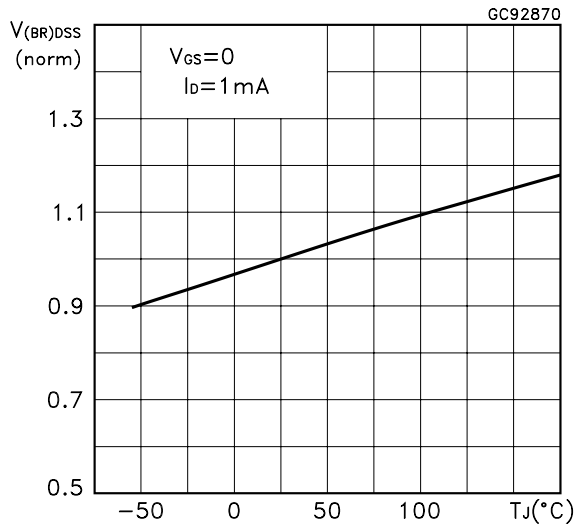


Fig. 1: Switching Times Test Circuits For Resistive Load

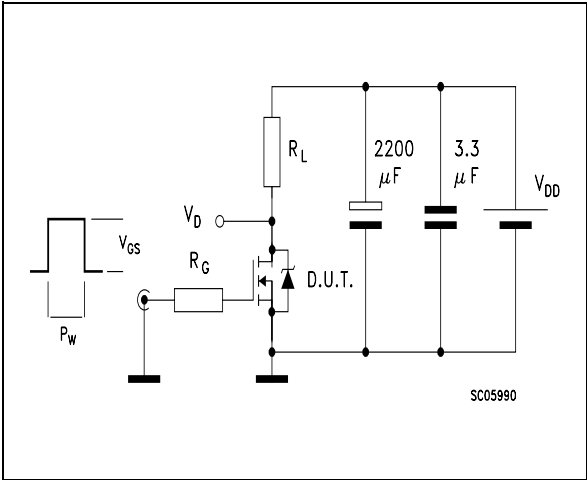


Fig. 2: Gate Charge test Circuit

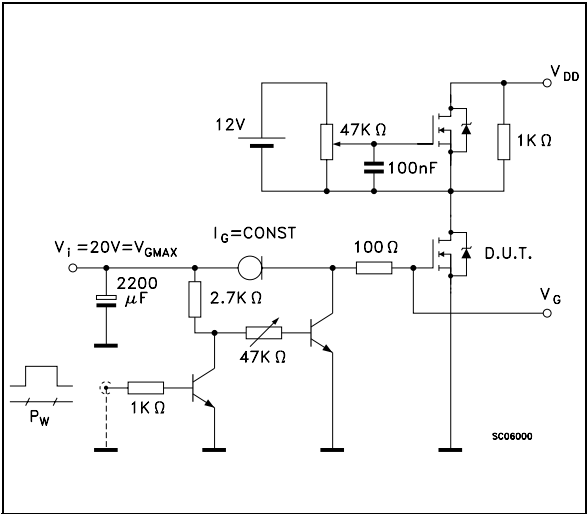
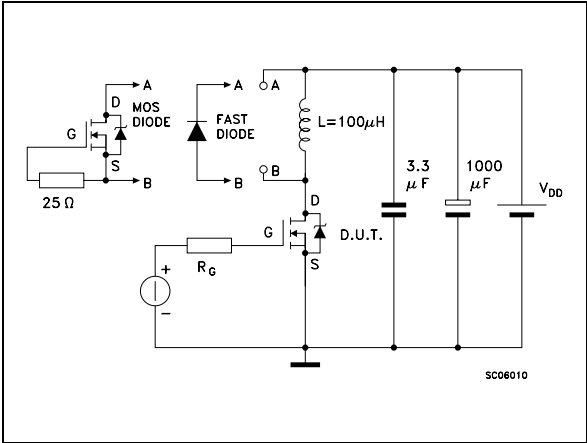
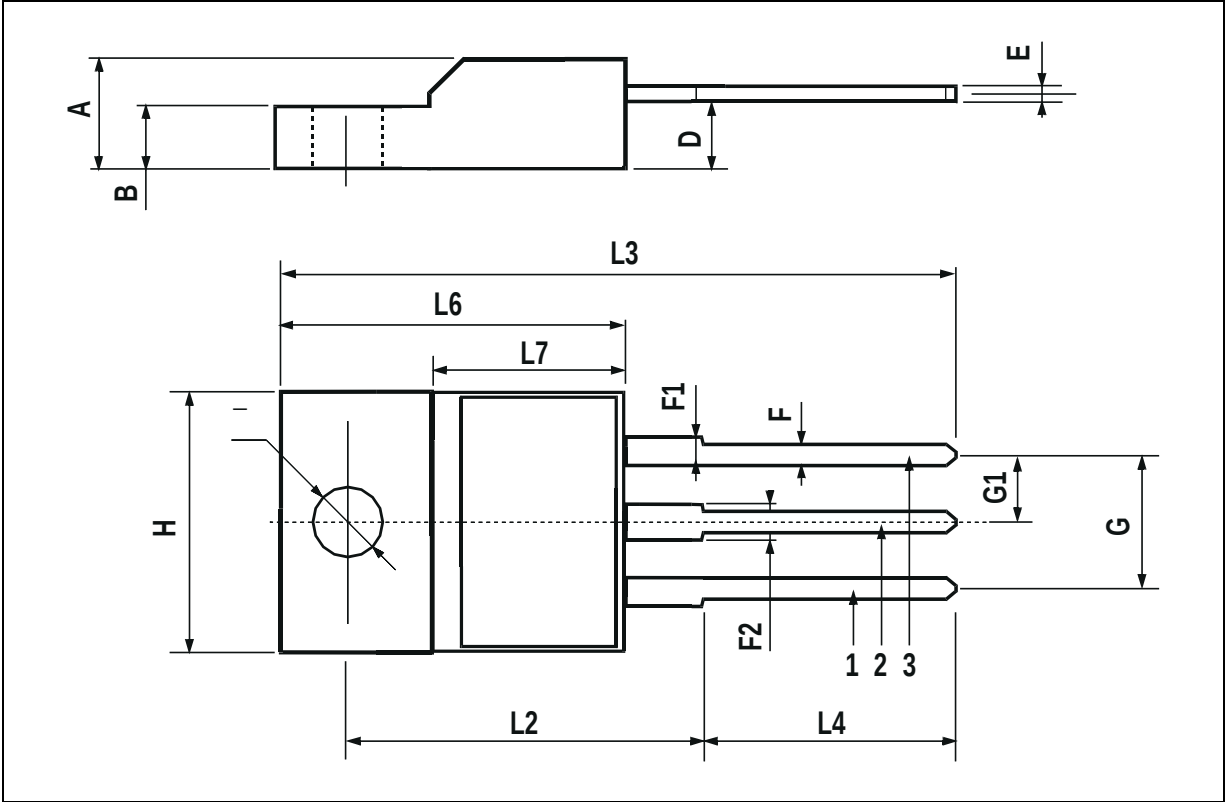


Fig. 3: Test Circuit For Diode Recovery Behaviour



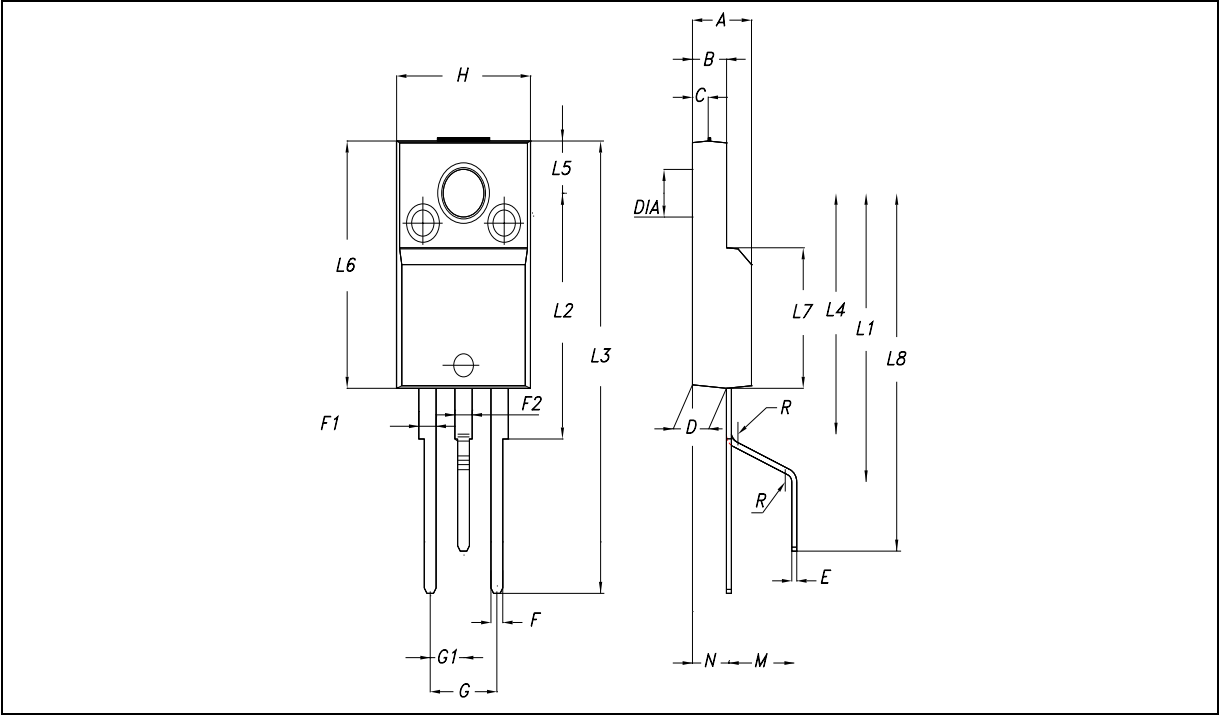
TO-220FP MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
B	2.5		2.7	0.098		0.106
D	2.5		2.75	0.098		0.108
E	0.45		0.7	0.017		0.027
F	0.75		1	0.030		0.039
F1	1.15		1.7	0.045		0.067
F2	1.15		1.7	0.045		0.067
G	4.95		5.2	0.195		0.204
G1	2.4		2.7	0.094		0.106
H	10		10.4	0.393		0.409
L2		16			0.630	
L3	28.6		30.6	1.126		1.204
L4	9.8		10.6	0.385		0.417
L6	15.9		16.4	0.626		0.645
L7	9		9.3	0.354		0.366
Ø	3		3.2	0.118		0.126



TO-220FP(023Y) MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
B	2.5		2.7	0.009		0.106
C	1		1.4	0.039		0.055
D	2.4		2.75	0.094		0.108
E	0.4		0.7	0.015		0.027
F	0.75		1	0.029		0.039
F1	1.15		1.7	0.045		0.066
F2	1.15		1.7	0.045		0.066
G	4.68		5.48	0.184		0.215
G1	2.24		2.84	0.088		0.111
H	10		10.4	0.393		0.409
L1	18.4		19.2	0.724		0.755
L2		16			0.629	
L3	29		30	1.14		1.18
L4	15.3		16.1	0.60		0.63
L5		3.4			0.133	
L6	15.9		16.4	0.625		0.665
L7	9		9.3	0.354		0.366
L8	22.5		23.6	0.885		0.929
M	4.6		5.4	0.181		0.212
N	2.29		3.29	0.090		0.129
Dia	3		3.2			



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