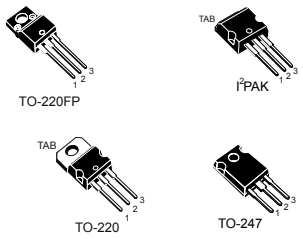
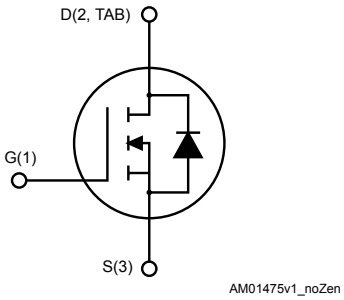
STF32N65M5, STI32N65M5
STP32N65M5, STW32N65M5

Datasheet

N-channel 650 V, 95 mΩ typ., 24 A MDmesh™ M5 Power MOSFETs in TO-220FP, I²PAK, TO-220 and TO-247 packages





Features

Order codes	V_{DS} at $T_{jmax.}$	$R_{DS(on)}$ max.	I_D	Package
STF32N65M5	710 V	119 mΩ	24 A	TO-220FP
STI32N65M5				I²PAK
STP32N65M5				TO-220
STW32N65M5				TO-247

- Extremely low $R_{DS(on)}$
- Low gate charge and input capacitance
- Excellent switching performance
- 100% avalanche tested

Applications

- Switching applications

Description

These devices are N-channel Power MOSFETs based on the MDmesh™ M5 innovative vertical process technology combined with the well-known PowerMESH™ horizontal layout. The resulting products offer extremely low on-resistance, making them particularly suitable for applications requiring high power and superior efficiency.

Product status link
STF32N65M5
STI32N65M5
STP32N65M5
STW32N65M5

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		I^2PAK, TO-220, TO-247	TO-220FP	
V_{GS}	Gate-source voltage	±25		V
I_D	Drain current (continuous) at T_C = 25 °C	24		A
I_D	Drain current (continuous) at T_C = 100 °C	15		A
I_{DM} (1)	Drain current (pulsed)	96		A
P_{TOT}	Total power dissipation at T_C = 25 °C	150	35	W
dv/dt (2)	Peak diode recovery voltage slope	15		V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat-sink (t = 1 s, T_C = 25 °C)		2500	V
T_j	Operating junction temperature range	-55 to 150		°C
T_{stg}	Storage temperature range			

1. *Pulse width limited by safe operating area.*
2. *I_{SD} ≤ 24 A, di/dt ≤ 400 A/µs, $V_{DS(peak)}$ ≤ $V_{(BR)DSS}$.*

Table 2. Thermal data

Symbol	Parameter	Value				Unit
		I^2PAK	TO-220	TO-247	TO-220FP	
$R_{thj\text{-}case}$	Thermal resistance junction-case	0.83			3.6	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient	62.5		50	62.5	°C/W

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_j Max)	8	A
E_{AS}	Single pulse avalanche energy (starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	650	mJ

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0 V	650			V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 650 V, V_{GS} = 0 V,			1	µA
		V_{DS} = 650 V, V_{GS} = 0 V, T_C = 125 °C (1)			100	µA
I_{GSS}	Gate body leakage current	V_{DS} = 0 V, V_{GS} = ±25 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10 V, I_D = 12 A		95	119	mΩ

1. *Defined by design, not subject to production test.*

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0 V	-	3320	-	pF
C_{oss}	Output capacitance			75		
C_{rss}	Reverse transfer capacitance			5		
$C_{o(tr)}$ (1)	Equivalent capacitance time related	V_{GS} = 0 V, V_{DS} = 0 to 520 V	-	210	-	pF
$C_{o(er)}$ (2)	Equivalent capacitance energy related		-	70	-	pF
Rg	Gate input resistance	f = 1 MHz, I_D= 0 A	-	2	-	Ω
Q_g	Total gate charge	V_{DD} = 520 V, I_D = 12 A, V_{GS} = 0 to 10 V (see Figure 19. Test circuit for gate charge behavior)	-	72	-	nC
Q_{gs}	Gate-source charge			17		
Q_{gd}	Gate-drain charge			29		

1. *$C_{o(tr)}$ time related is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.*
2. *$C_{o(er)}$ energy related is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.*

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$	Turn-off delay time	V_{DD} = 400 V, I_D = 15 A, R_G = 4.7 Ω, V_{GS} = 10 V (see Figure 20. Test circuit for inductive load switching and diode recovery times and Figure 23. Switching time waveform)	-	53	-	ns
t_r	Rise time			12		
t_c	Cross time			29		
t_f	Fall time			16		

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		24	A
I_{SDM} (1)	Source-drain current (pulsed)				96	
V_{SD} (2)	Forward on voltage	I_{SD} = 24 A, V_{GS} = 0 V	-		1.5	V
t_{rr}	Reverse recovery time	I_{SD} = 24 A, di/dt = 100 A/µs	-	375		ns
Q_{rr}	Reverse recovery charge	V_{DD} = 60 V (see Figure 20. Test circuit for inductive load switching and diode recovery times)		6		µC
I_{RRM}	Reverse recovery current			33		A
t_{rr}	Reverse recovery time	I_{SD} = 24 A, di/dt = 100 A/µs	-	440		ns
Q_{rr}	Reverse recovery charge	V_{DD} = 60 V, Tj = 150 °C		8		µC
I_{RRM}	Reverse recovery current	(see Figure 20. Test circuit for inductive load switching and diode recovery times)		36		A

1. *Pulse width limited by safe operating area.*
2. *Pulsed: pulse duration = 300 µs, duty cycle 1.5%.*

2.1 Electrical characteristics curves

Figure 1. Safe operating area for TO-220FP

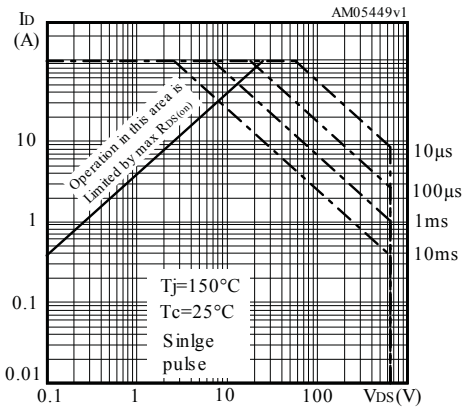


Figure 2. Thermal impedance for TO-220FP

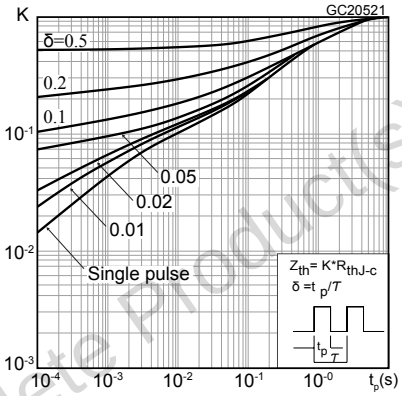


Figure 3. Safe operating area for I²PAK, TO-220

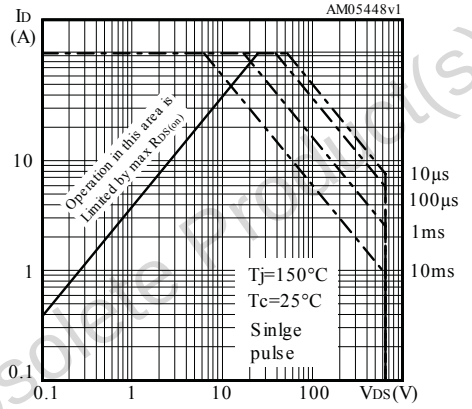


Figure 4. Thermal impedance for I²PAK, TO-220

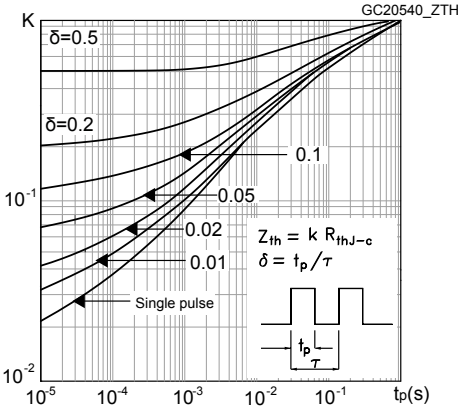


Figure 5. Safe operating area for TO-247

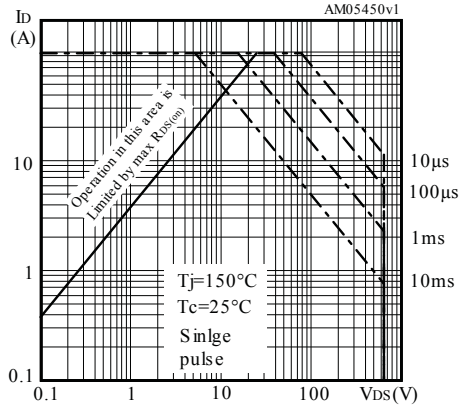


Figure 6. Thermal impedance for TO-247

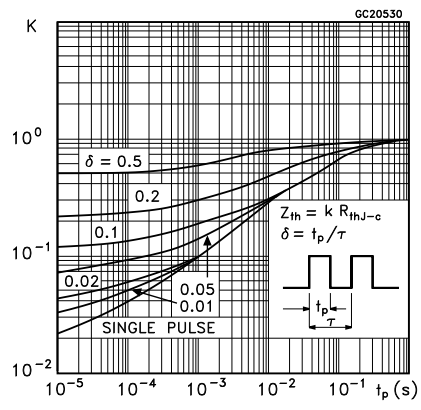


Figure 7. Output characterisics

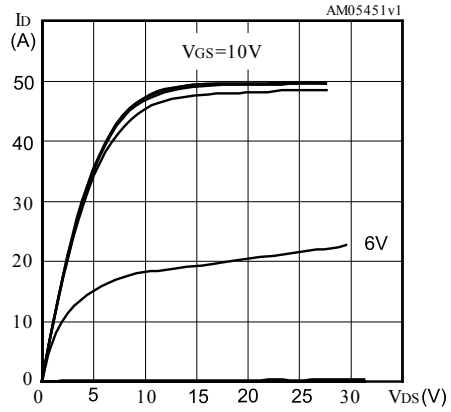


Figure 8. Transfer characteristics

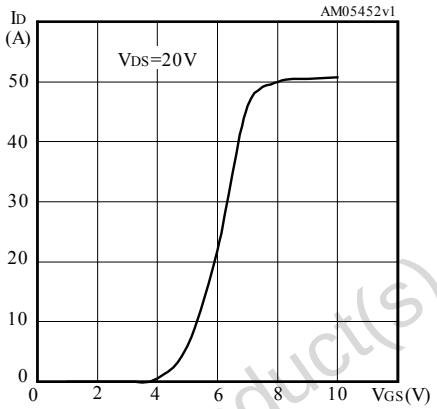


Figure 9. Gate charge vs gate-source voltage

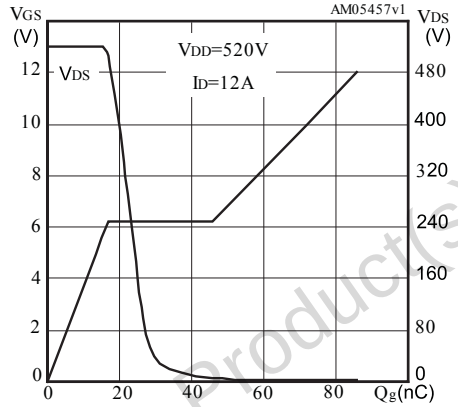


Figure 10. Static drain-source on resistance

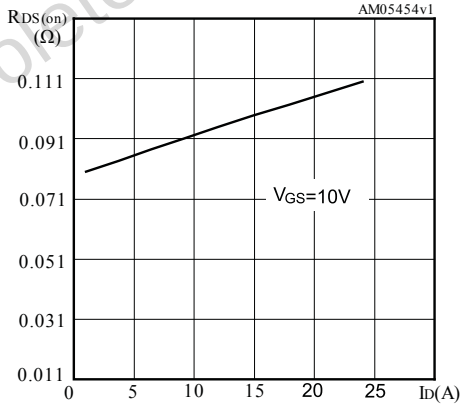


Figure 11. Capacitance variations

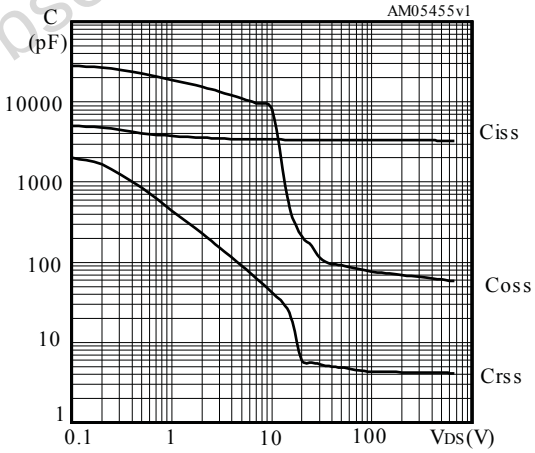


Figure 12. Output capacitance stored energy

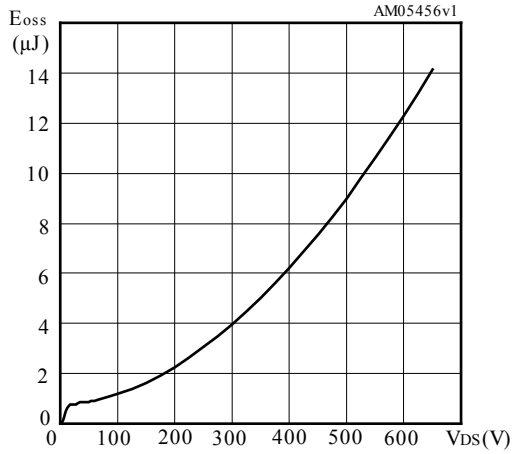


Figure 13. Normalized gate threshold voltage vs temperature

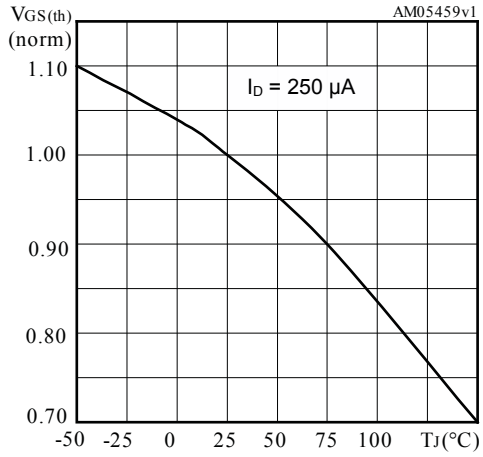


Figure 14. Normalized on resistance vs temperature

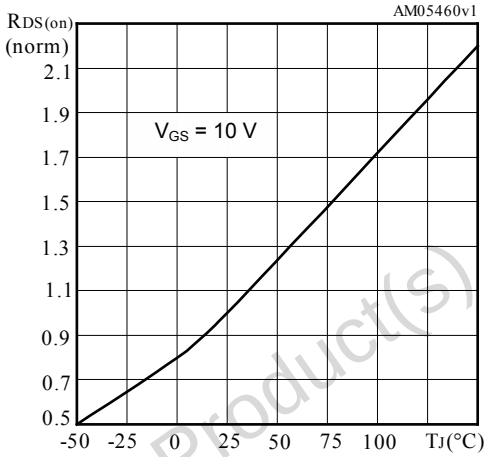


Figure 15. Source-drain diode forward characteristics

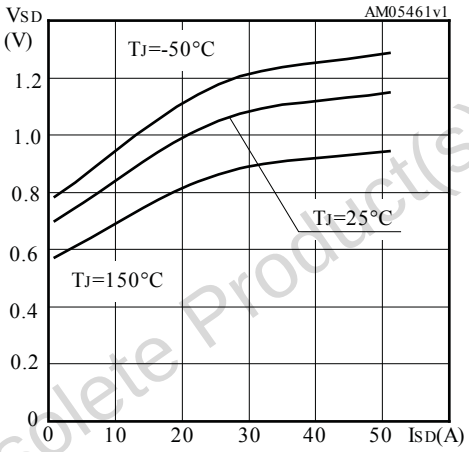


Figure 16. Normalized $V_{(BR)DSS}$ vs temperature

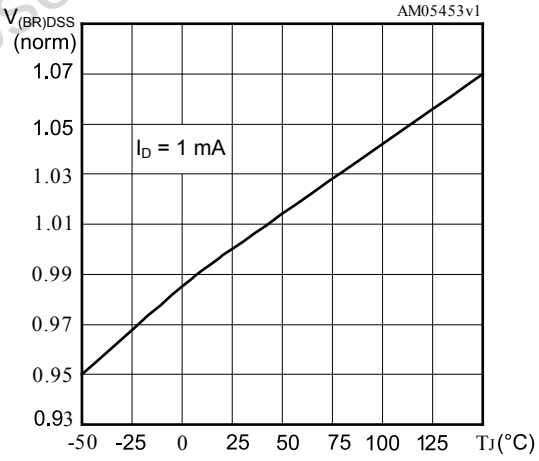
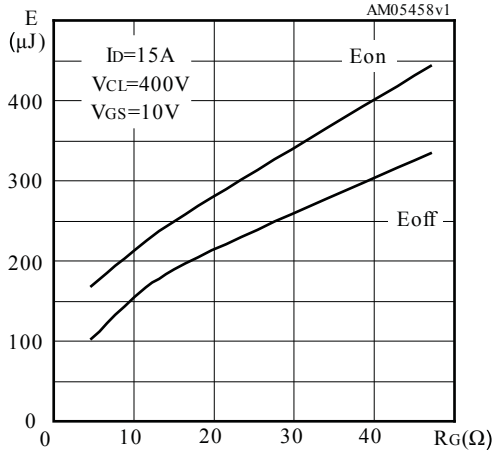


Figure 17. Switching energy vs gate resistance



* Eon including reverse recovery of a SiC diode.

3 Test circuits

Figure 18. Test circuit for resistive load switching times

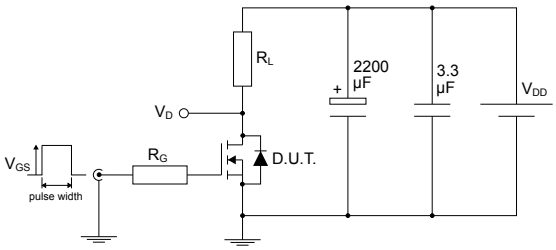


Figure 19. Test circuit for gate charge behavior

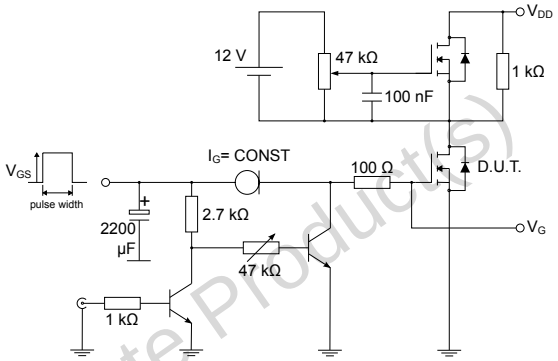


Figure 20. Test circuit for inductive load switching and diode recovery times

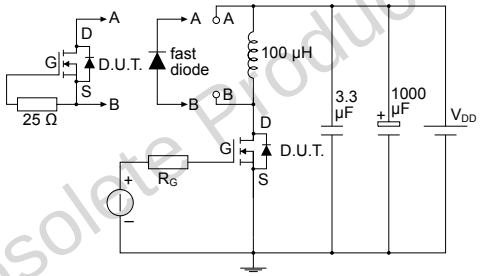


Figure 21. Unclamped inductive load test circuit

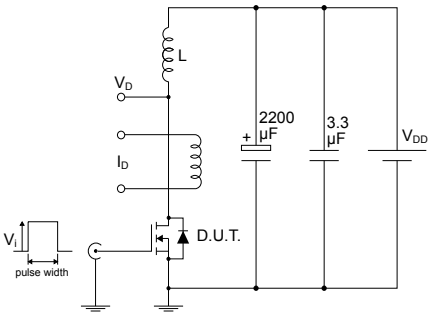


Figure 22. Unclamped inductive waveform

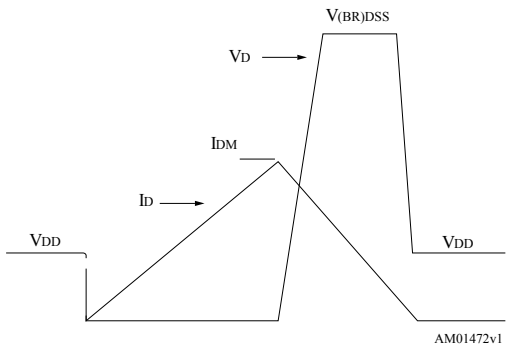
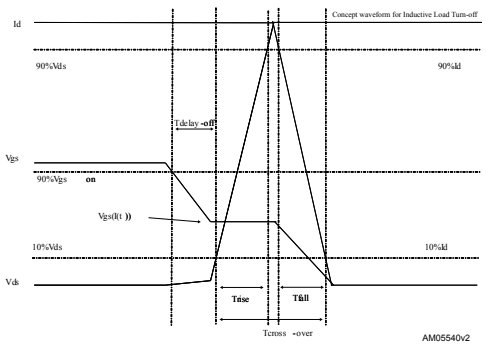


Figure 23. Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 TO-220FP package information

Figure 24. **TO-220FP package outline**

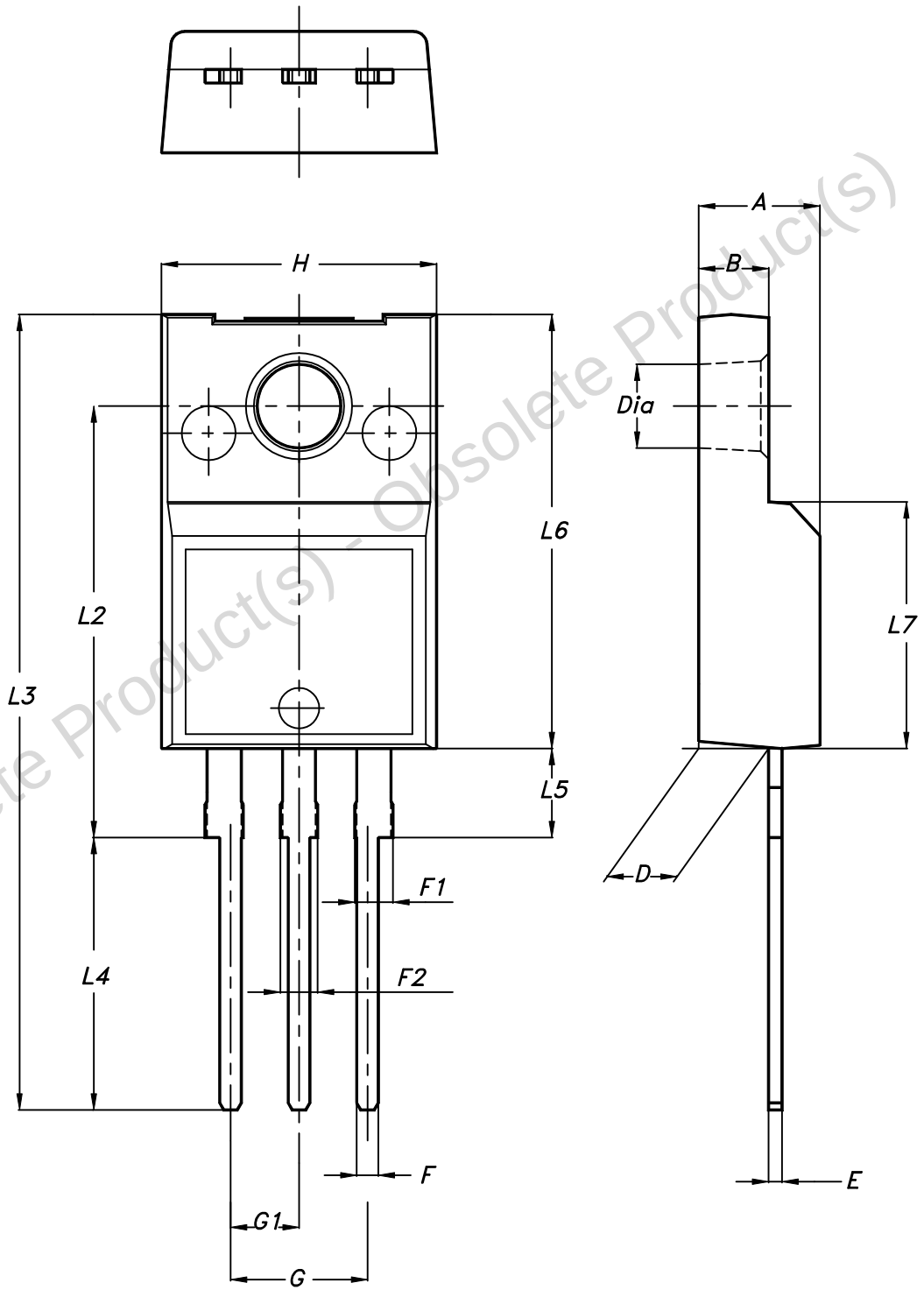


Table 8. **TO-220FP package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

4.2 I²PAK package information

Figure 25. I²PAK package outline

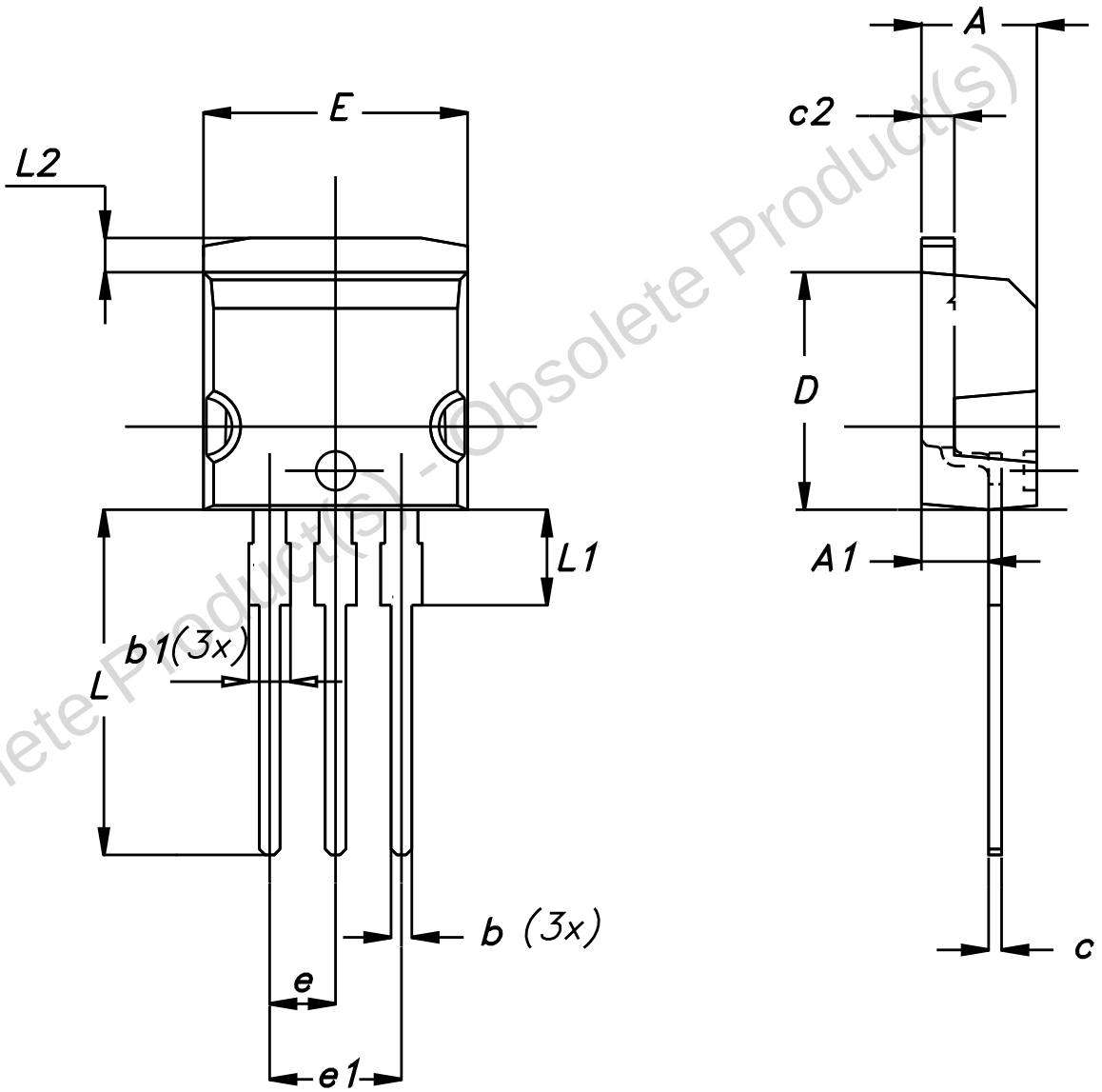


Table 9. I²PAK package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40	-	4.60
A1	2.40	-	2.72
b	0.61	-	0.88
b1	1.14	-	1.70
c	0.49	-	0.70
c2	1.23	-	1.32
D	8.95	-	9.35
e	2.40	-	2.70
e1	4.95	-	5.15
E	10	-	10.40
L	13	-	14
L1	3.50	-	3.93
L2	1.27	-	1.40

4.3 TO-220 type A package information

Figure 26. **TO-220 type A package outline**

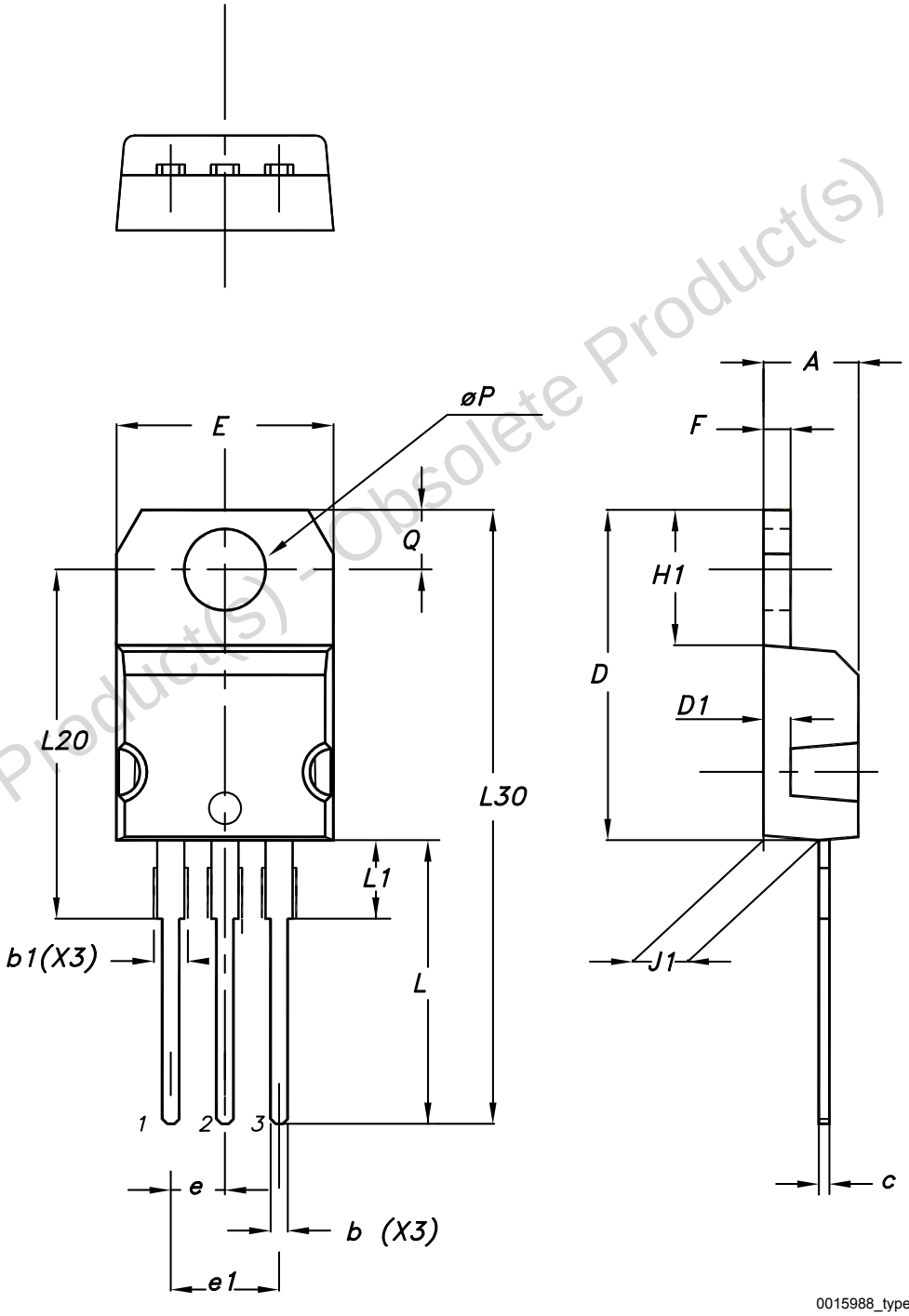


Table 10. **TO-220 type A package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.55
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10.00		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13.00		14.00
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95

4.4 TO-247 package information

Figure 27. **TO-247 package outline**

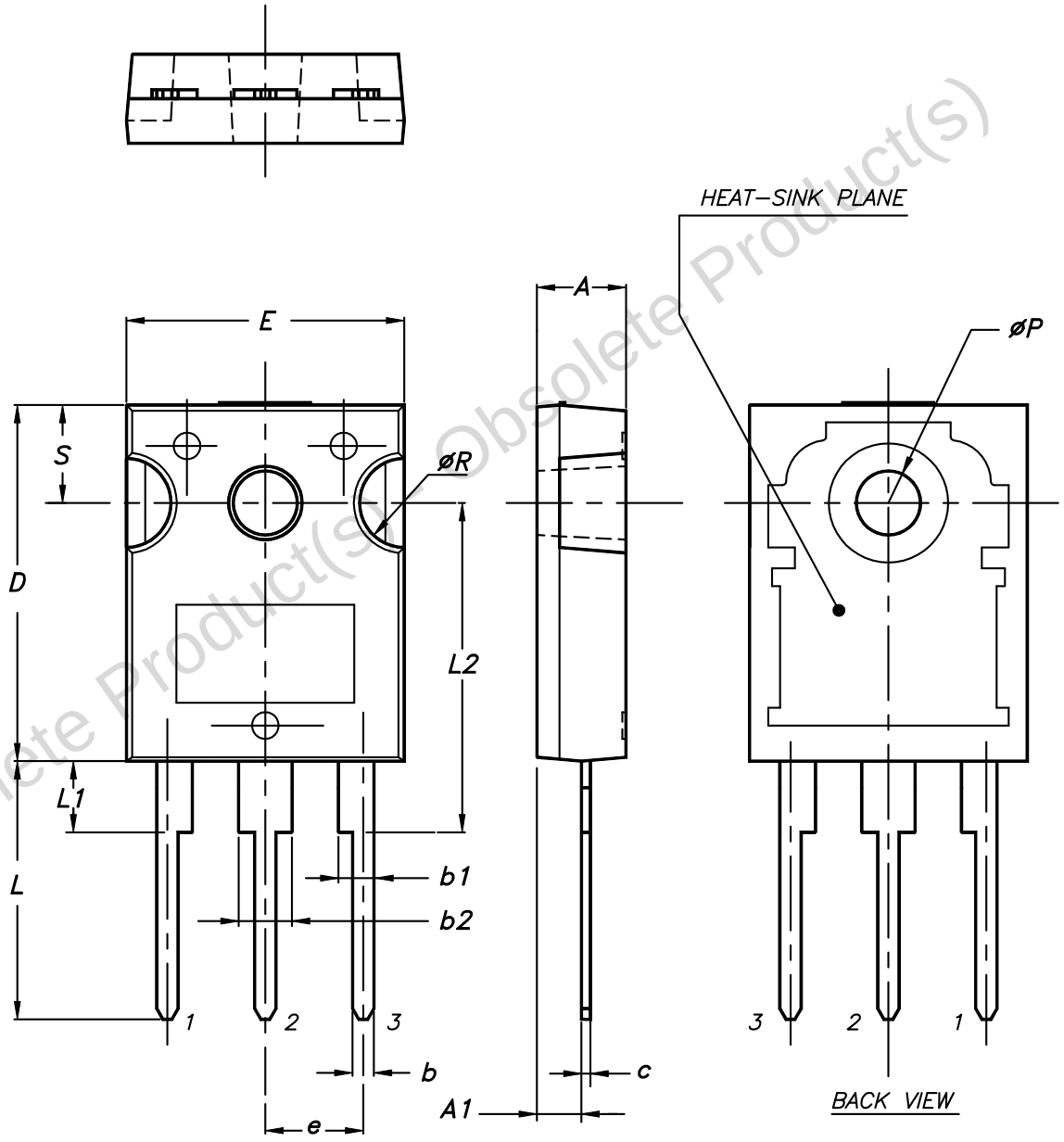


Table 11. **TO-247 package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e	5.30	5.45	5.60
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
ØP	3.55		3.65
ØR	4.50		5.50
S	5.30	5.50	5.70

5 Ordering information

Table 12. **Order codes**

Order code	Marking	Package	Packing
STF32N65M5	32N65M5	TO-220FP	Tube
STI32N65M5		I^2PAK	
STP32N65M5		TO-220	
STW32N65M5		TO-247	

Revision history

Table 13. **Document revision history**

Date	Version	Changes
05-Nov-2018	1	First release. Part numbers previously included in datasheet DocID15316.

Contents