STP4189D

P Channel Enhancement Mode MOSFET

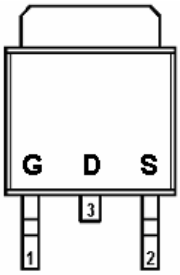
-12.0A

DESCRIPTION

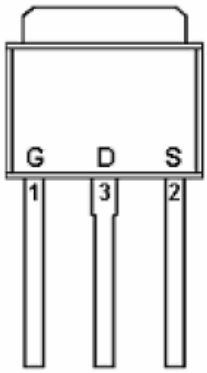
STP4189D is the P-Channel logic enhancement mode power field effect transistor which is produced using high cell density, DMOS trench technology. The STP413D has been designed specially to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low $R_{DS(ON)}$ and fast switching speed.

PIN CONFIGURATION (D-PAK)

TO-252



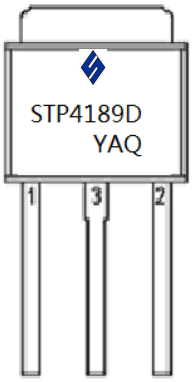
TO-251

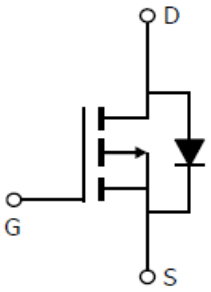


FEATURE

- -40V/-12.0A, $R_{DS(ON)}$ = 18mΩ (Typ.) @V_{GS} = -10V
- -40V/-8.0A, $R_{DS(ON)}$ = 24mΩ @V_{GS} =-4.5V
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- TO-252,TO-251 package design

PART MARKING





Y: Year Code
A: Week Date
Q: Process Code

STANSON TECHNOLOGY
120 Bentley Square, Mountain View, Ca 94040 USA
www.stansontech.com

STANSON

STP4189D

P Channel Enhancement Mode MOSFET

-12.0A

ABSOULTE MAXIMUM RATINGS (Ta = 25℃ Unless otherwise noted)

Parameter		Symbol	Typical	Unit
Drain-Source Voltage		VDSS	-40	V
Gate-Source Voltage		VGSS	±20	V
Pulsed Drain Current		IDM	-50	A
Continuous Source Current (Diode Conduction)		IS	-20	A
Power Dissipation	TA=25℃ TA=70℃	PD	52.5 31	W
Operation Junction Temperature		TJ	150	℃
Storgae Temperature Range		TSTG	-55/150	℃
Thermal Resistance-Junction to Ambient		RθJA	50	℃/W

STANSON TECHNOLOGY
120 Bentley Square, Mountain View, Ca 94040 USA
www.stansontech.com

STANSON

STP4189D

P Channel Enhancement Mode MOSFET

-12.0A

ELECTRICAL CHARACTERISTICS (Ta = 25℃ Unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V,ID=-250uA	-40			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},ID=-250uA	-1.0		-3.0	V
Gate Leakage Current	I_{GSS}	V_{DS}=0V,V_{GS}=±20V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-40V,V_{GS}=0V			-1	uA
		V_{DS}=-40V,V_{GS}=0V T_J=55℃			-5	
Drain-source On-Resistance	$R_{DS(on)}$	V_{GS}=-10V,I_D=-12A V_{GS}=-4.5V,I_D=-8A		18 23	22 29	mΩ
Forward Transconductance	gfs	V_{DS}=-5V,I_D=-12A		23		S
Diode Forward Voltage	V_{SD}	I_S=-1.0A,V_{GS}=0V			-1.2	V
Dynamic						
Total Gate Charge	Q_g	V_{DS}=-10V,V_{DS}=-20V I_D=-12A		31.5		nC
Gate-Source Charge	Q_{gs}			7.8		
Gate-Drain Charge	Q_{gd}			6.5		
Input Capacitance	C_{iss}	V_{DS} =-20V,VGS=0V F=1MHz		1870		pF
Output Capacitance	C_{oss}			185		
Reverse TransferCapacitance	C_{rss}			155		
Turn-On Time	$t_{d(on)}$	V_{GS}=-10V,V_{DS}=-20V R_L=1.6Ω,R_{GEN}=3Ω		10		nS
	tr			18		
Turn-Off Time	$t_{d(off)}$			38		
	tf			25		

STANSON TECHNOLOGY
120 Bentley Square, Mountain View, Ca 94040 USA
www.stansontech.com

TYPICAL CHARACTERICTICS

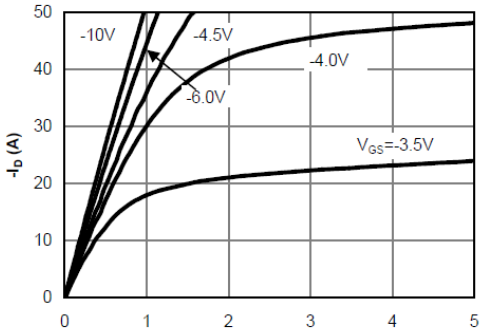


Figure 1: On-Region Characteristics

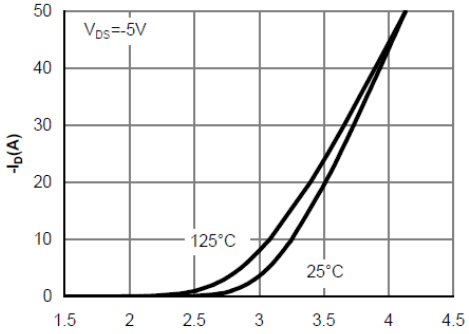


Figure 2: Transfer Characteristics

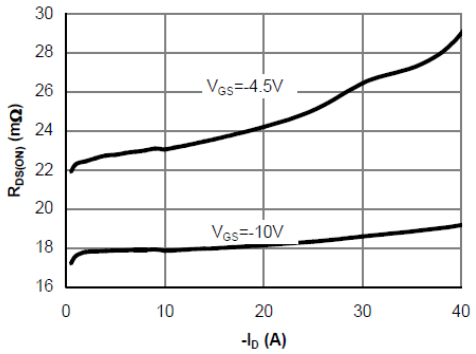


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

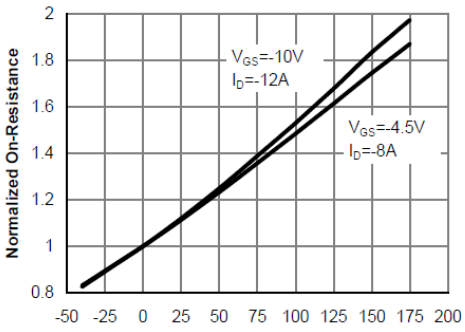


Figure 4: On-Resistance vs. Junction Temperature

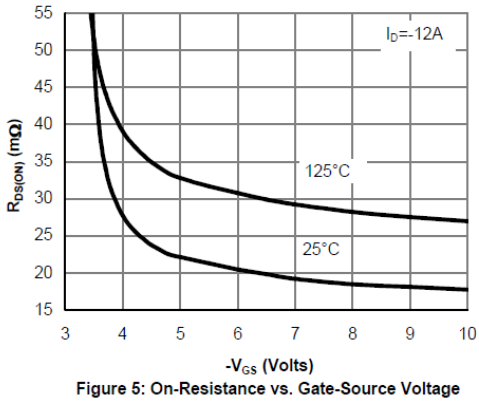


Figure 5: On-Resistance vs. Gate-Source Voltage

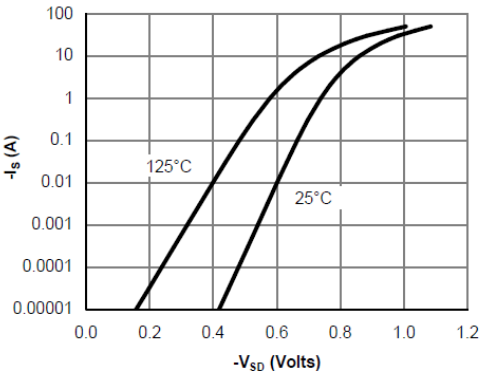


Figure 6: Body-Diode Characteristics

STANSON TECHNOLOGY
120 Bentley Square, Mountain View, Ca 94040 USA
www.stansontech.com

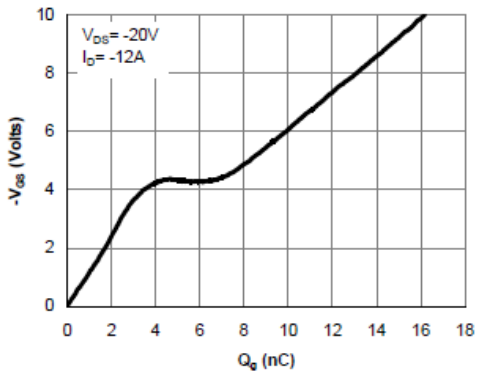


Figure 7: Gate-Charge Characteristics

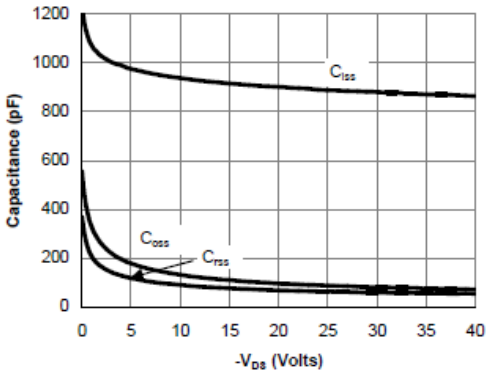


Figure 8: Capacitance Characteristics

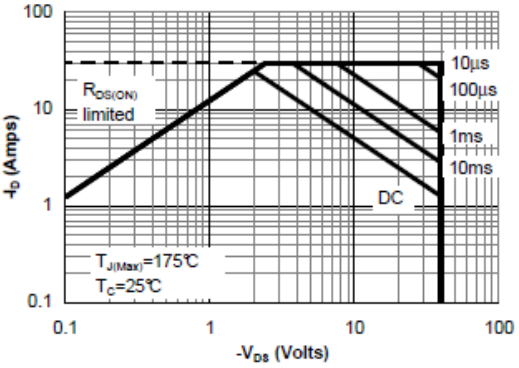


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

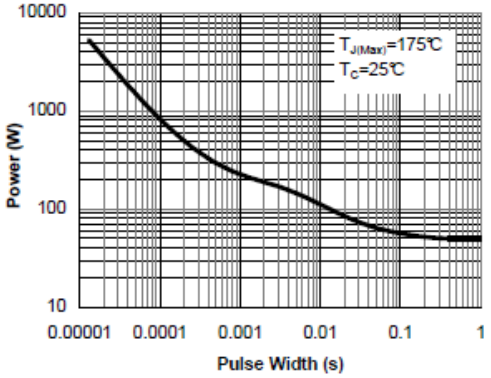


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

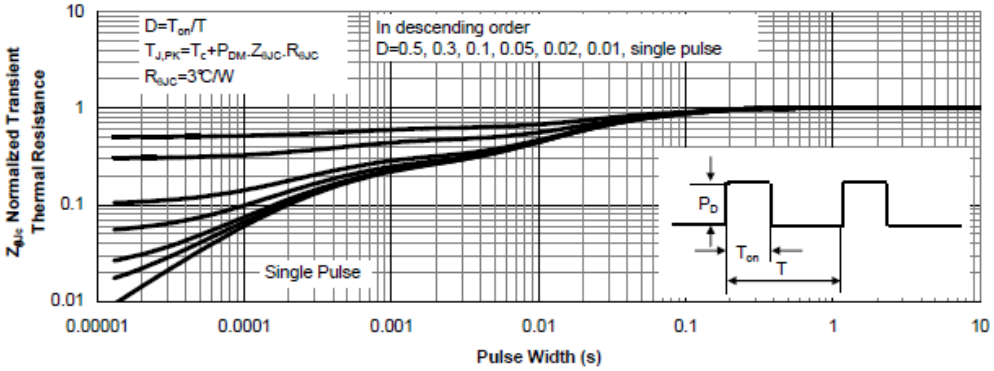


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

STANSON TECHNOLOGY
120 Bentley Square, Mountain View, Ca 94040 USA
www.stansontech.com

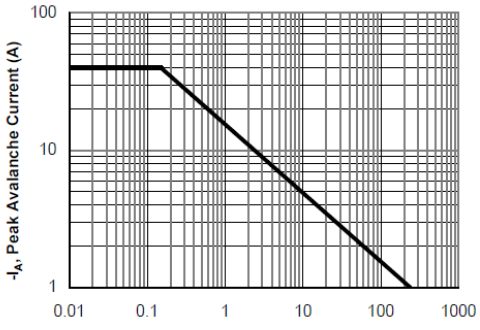


Figure 12: Single Pulse Avalanche Capability

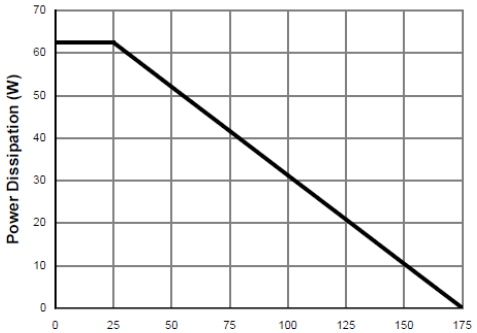


Figure 13: Power De-rating (Note B)

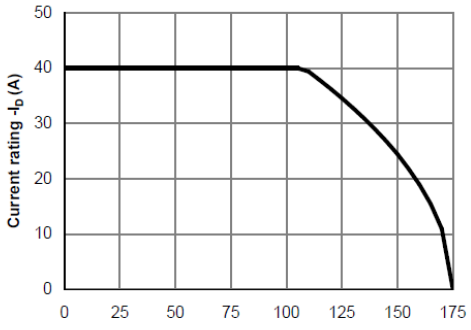


Figure 14: Current De-rating (Note B)

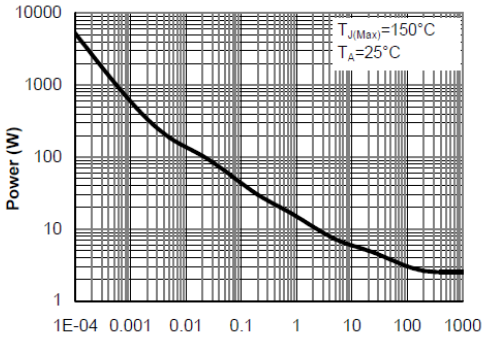


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note G)

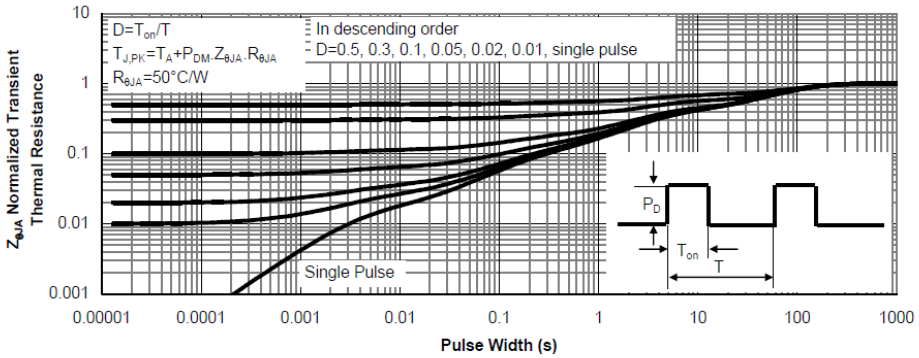
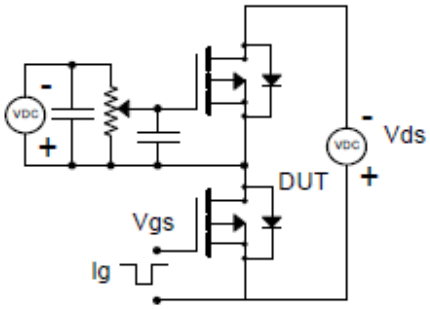
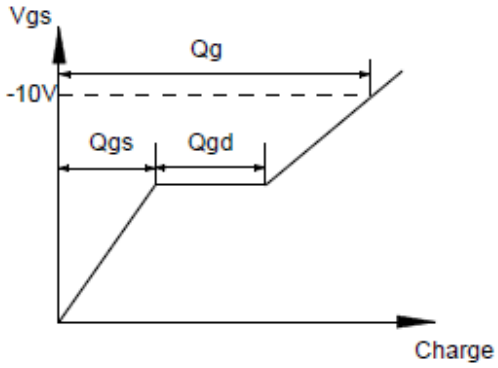


Figure 16: Normalized Maximum Transient Thermal Impedance (Note G)

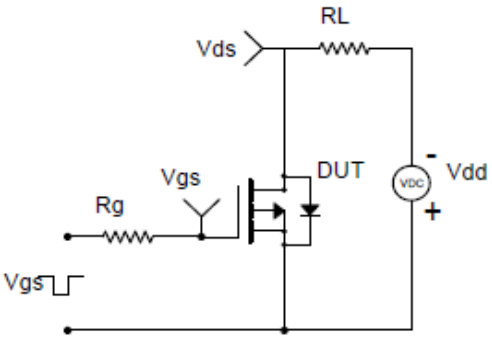
STANSON TECHNOLOGY
120 Bentley Square, Mountain View, Ca 94040 USA
www.stansontech.com

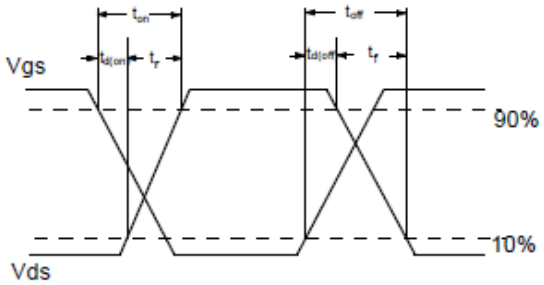
GATE CHARGE TEST CIRCUIT & WAVEFORM





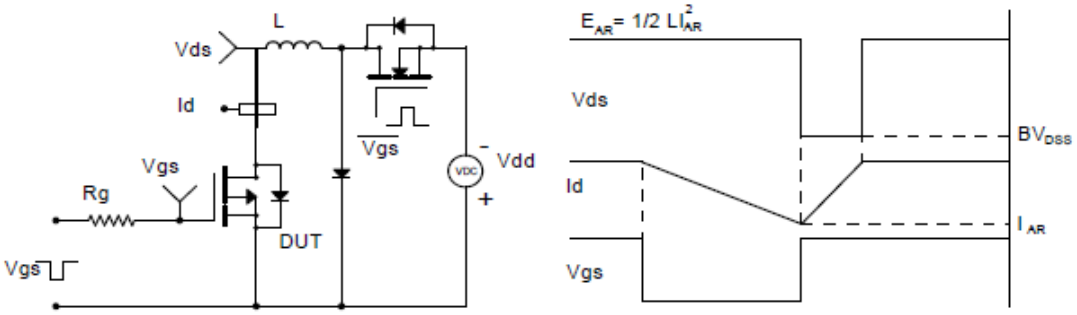
TESISTIVE SWITCHING TEST CIRCUIT & WAVEFORMS



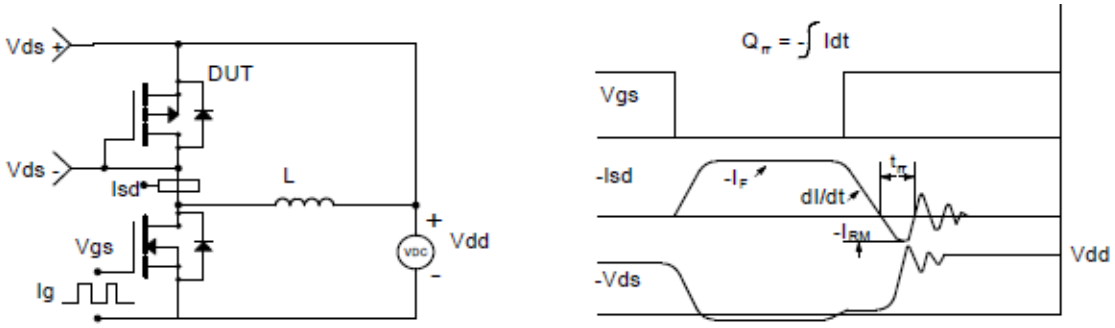


STANSON TECHNOLOGY
120 Bentley Square, Mountain View, Ca 94040 USA
www.stansontech.com

UNCLAMPED INDUCTIVE SWITCHING (UIS) TEST CIRCUIT & WAVEFORMS



DIODE TEC0VERY TEST CIRCUIT & WAVEFORMS



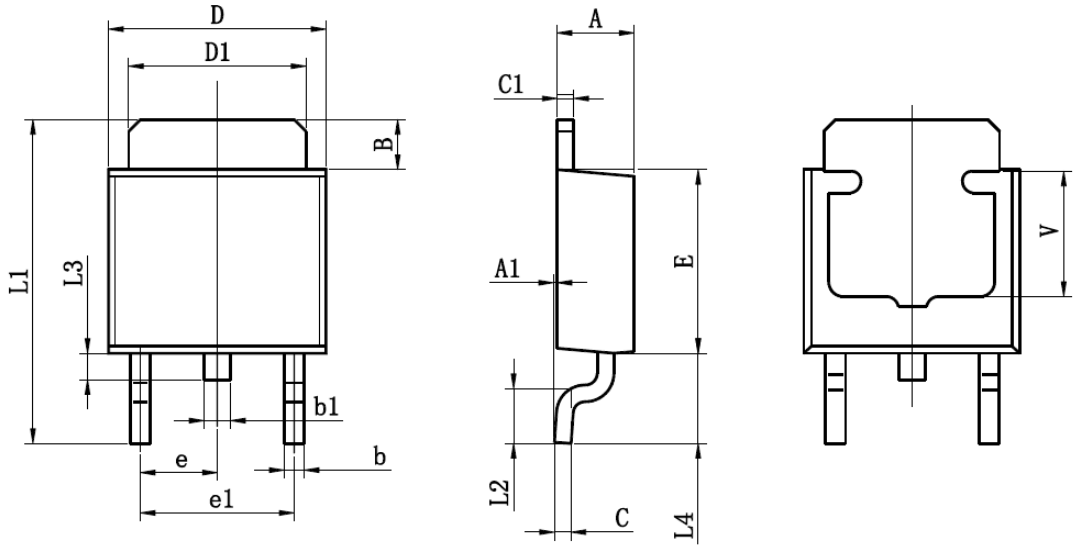
STANSON TECHNOLOGY
120 Bentley Square, Mountain View, Ca 94040 USA
www.stansontech.com

STP4189D

P Channel Enhancement Mode MOSFET

-12.0A

TO-252-2L PACKAGE OUTLINE SOP-8P



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	2.200	2.400	0.087	0.094
A1	0.000	0.127	0.000	0.005
B	1.350	1.650	0.053	0.065
b	0.500	0.700	0.020	0.028
b1	0.700	0.900	0.028	0.035
c	0.430	0.580	0.017	0.023
c1	0.430	0.580	0.017	0.023
D	6.350	6.650	0.250	0.262
D1	5.200	5.400	0.205	0.213
E	5.400	5.700	0.213	0.224
e	2.300TYP		0.091TYP	
e1	4.500	4.700	0.177	0.185
L1	9.500	9.900	0.374	0.390
L2	1.400	1.780	0.055	0.070
L3	0.650	0.950	0.026	0.037
L4	2.550	2.900	0.100	0.114
V	3.80REF		0.150REF	

STANSON TECHNOLOGY
120 Bentley Square, Mountain View, Ca 94040 USA
www.stansontech.com