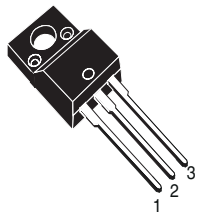
STP5NK80ZFP-H

N-channel 800 V, 1.9 Ω, 4.3 A, TO-220FP Zener-protected SuperMESH™ Power MOSFET

Features

Type	V_{DSS} (@Tjmax)	$R_{DS(on)}$ max	I_D
STP5NK80ZFP-H	800 V	< 2.4 Ω	4.3 A

- 100% avalanche tested
- Gate charge minimized
- Very low intrinsic capacitance
- Very good manufacturing repeatability



TO-220FP

Application

- Switching applications

Description

The SuperMESH™ series is obtained through an extreme optimization of ST's well established strip-based PowerMESH™ layout. In addition to pushing on-resistance significantly down, special care is taken to ensure a very good dv/dt capability for the most demanding applications. Such series complements ST full range of high voltage Power MOSFETs including revolutionary MDmesh™ products.

Figure 1. Internal schematic diagram

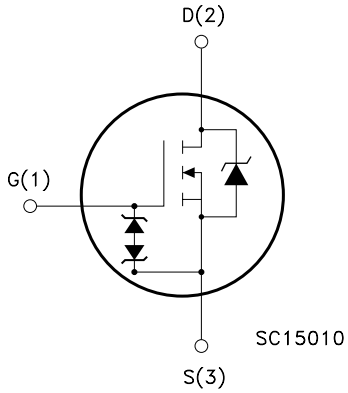


Table 1. Device summary

Order code	Marking	Package	Packaging
STP5NK80ZFP-H	P5NK80ZFP-H	TO-220FP	Tube

Note: Meets ECOPACK2® standards, an environmentally-friendly grade of products commonly referred to as "halogen-free".

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage (V_{GS} = 0)	800	V
V_{GS}	Gate-source voltage	± 30	V
I_D	Drain current (continuous) at T_C = 25 °C	4.3 (1)	A
I_D	Drain current (continuous) at T_C=100 °C	2.7 (1)	A
I_{DM}(2)	Drain current (pulsed)	17.2 (1)	A
P_{TOT}	Total dissipation at T_C = 25 °C	30	W
	Derating factor	0.24	W/°C
$V_{ESD(G-S)}$	Gate source ESD (HBM-C=100 pF, R=1.5 kΩ)	3500	V
dv/dt (3)	Peak diode recovery voltage slope	4.5	V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t=1 s; T_C = 25 °C)	2500	V
T_J T_{stg}	Operating junction temperature Storage temperature	-55 to 150	°C

1. Limited only by maximum temperature allowed.
2. Pulse width limited by safe operating area.
3. $I_{SD} \leq 4.3$ A, di/dt $\leq$ 200A/µs, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq T_{JMAX}$.

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case max	4.2	°C/W

Table 4. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_J max)	4.3	A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, $I_D = I_{AR}$, V_{DD}= 50 V)	190	mJ

2 Electrical characteristics

(T_{CASE}= 25 °C unless otherwise specified)

Table 5. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS}= 0	800			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max rating, V_{DS} = Max rating,Tc = 125 °C			1 50	µA µA
I_{GSS}	Gate body leakage current (V_{GS} = 0)	V_{GS} = ± 20 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 100 µA	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10 V, I_D = 2.15 A		1.9	2.4	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward transconductance	V_{DS} =15 V, I_D = 2.15 A	-	4.25		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V, f=1 MHz, V_{GS}=0	-	910 98 20		pF pF pF
C_{osseq} (2).	Equivalent output capacitance	V_{GS}=0, V_{DS} =0 to 400 V	-	40		pF
$t_{d(on)}$ t_r $t_{d(off)}$ t_r	Turn-on delay time Rise time Turn-on delay time fall time	V_{DD}= 400 V, I_D= 2 A, R_G=4.7 Ω, V_{GS}=10 V (see *Figure 17*)	-	18 25 45 30		ns ns ns ns
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD}=640 V, I_D = 4.3 A V_{GS} =10 V	-	32.4 5 18.5	45.5	nC nC nC
$t_{d(Voff)}$ t_r	Off-voltage rise time Fall time Cross-over time	V_{DD}=640 V, I_D= 4.3 A, R_G=4.7 Ω, V_{GS}=10 V (see *Figure 20*)	-	22 10 32		ns ns ns

1. Pulsed: pulse duration=300µs, duty cycle 1.5%
2. $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
I_{SD}	Source-drain current		-		4.3	A
I_{SDM}(1)	Source-drain current (pulsed)				17.2	A
V_{SD}(2)	Forward on voltage	I_{SD}= 4.3 A, V_{GS}=0	-		1.6	V
t_{rr}	Reverse recovery time	I_{SD}= 4.3 A, di/dt = 100 A/µs, V_{DD}=40 V, Tj = 150 °C (see *Figure 20*)	-	500		ns
Q_{rr}	Reverse recovery charge			3		µC
I_{RRM}	Reverse recovery current			12		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300µs, duty cycle 1.5%

Table 8. Gate-source zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
BV_{GSO}	Gate-source breakdown voltage	Igs=± 1mA (open drain)	30	-		V

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

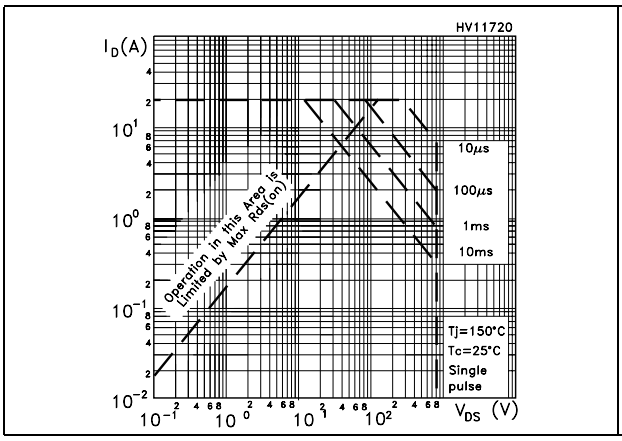


Figure 3. Thermal impedance

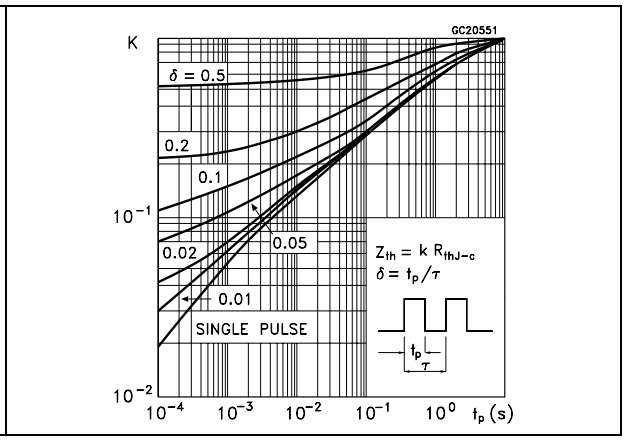


Figure 4. Output characteristics

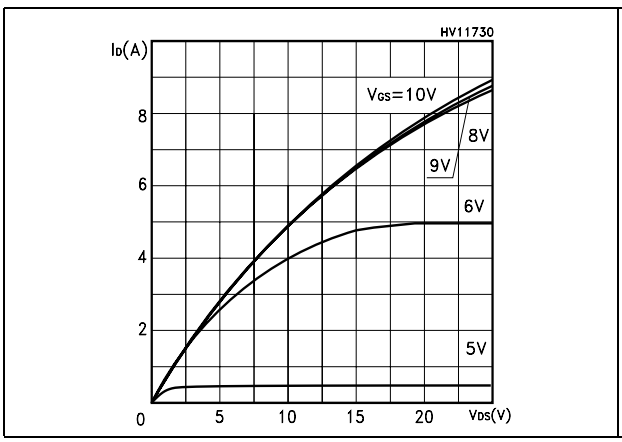


Figure 5. Transfer characteristics

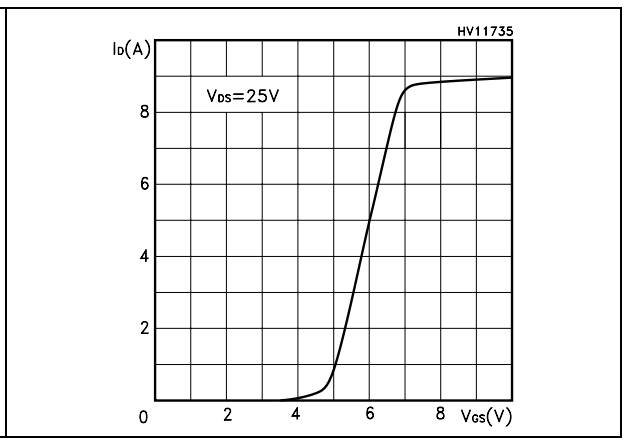


Figure 6. Transconductance

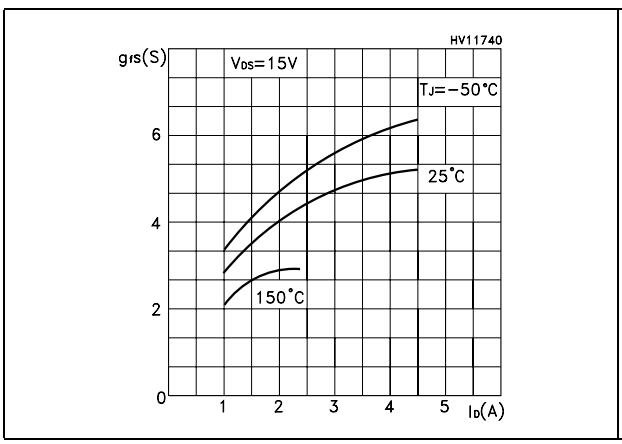


Figure 7. Static drain-source on resistance

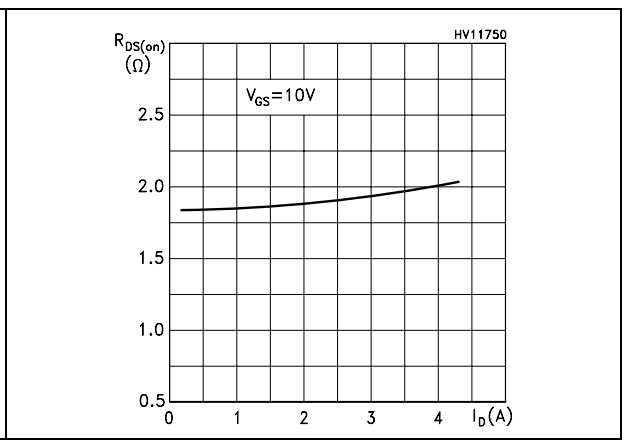


Figure 8. Gate charge vs gate-source voltage

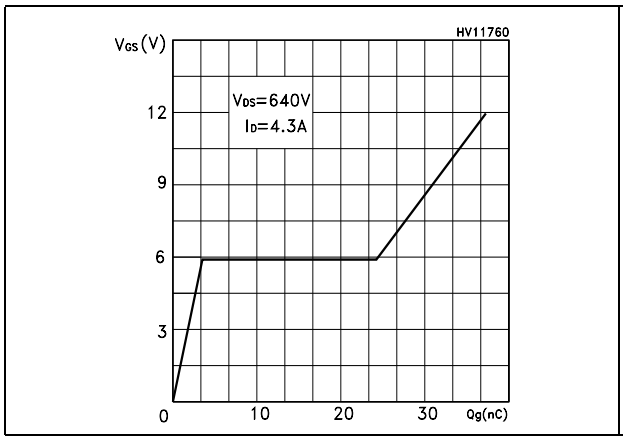


Figure 9. Capacitance variations

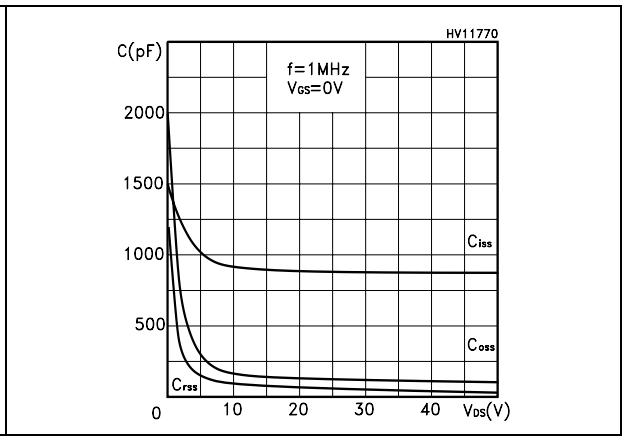


Figure 10. Normalized gate threshold voltage vs temperature

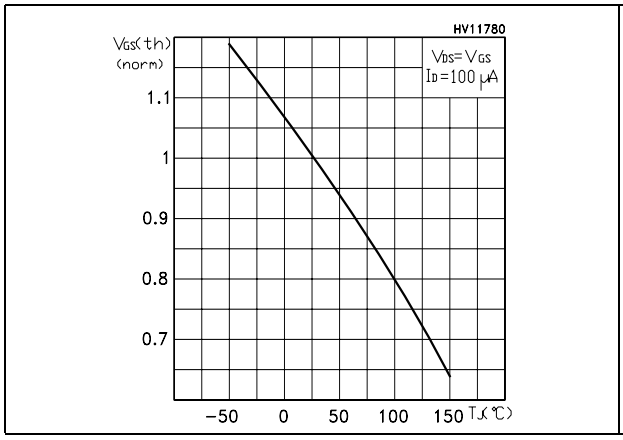


Figure 11. Normalized on resistance vs temperature

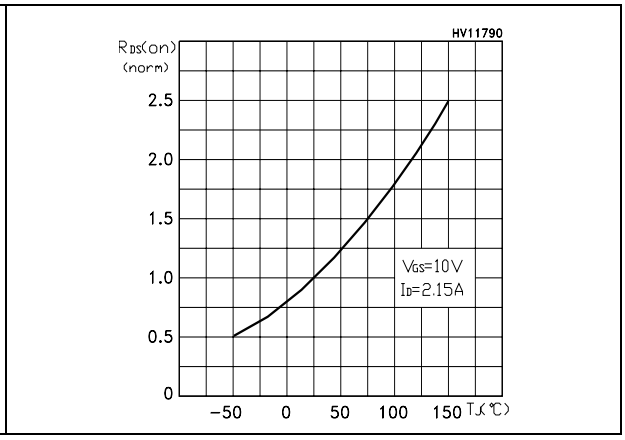


Figure 12. Source-drain diode forward characteristics

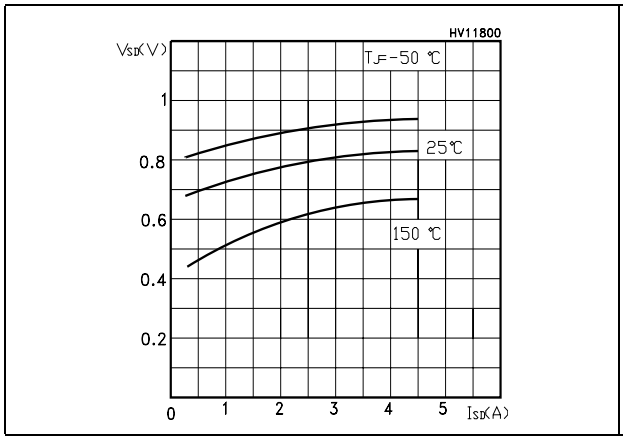


Figure 13. Normalized BVdss vs temperature

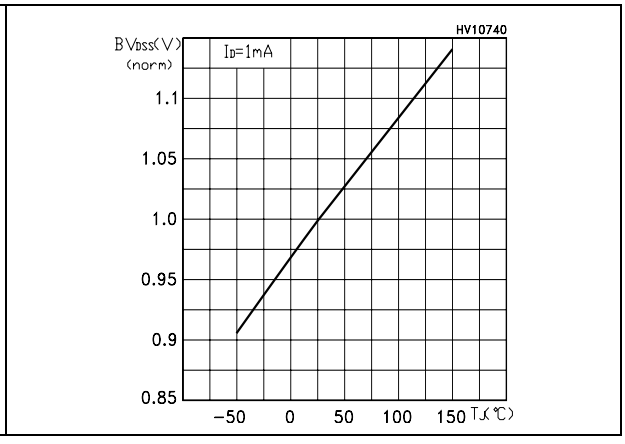
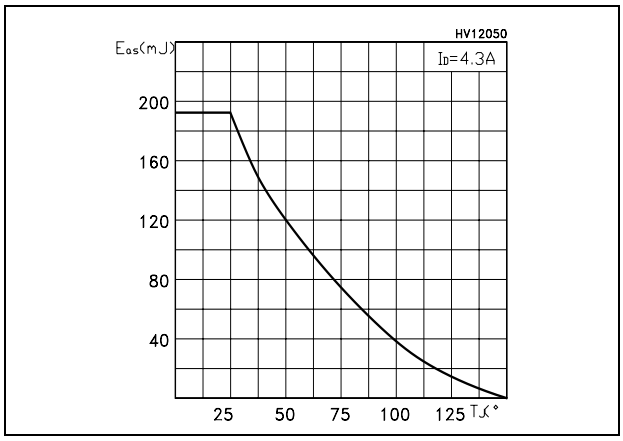


Figure 14. Source-drain diode forward characteristics



3 Test circuit

Figure 15. Unclamped inductive load test circuit

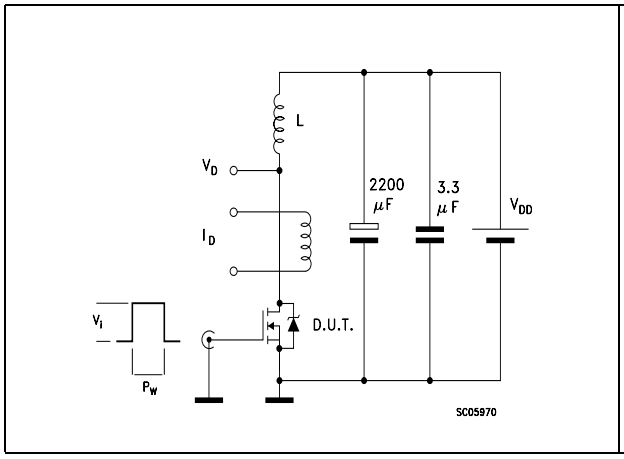


Figure 16. Unclamped inductive waveform

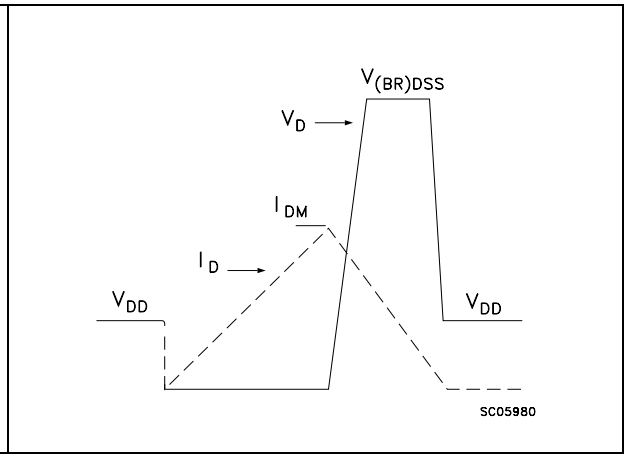


Figure 17. Switching times test circuit for resistive load

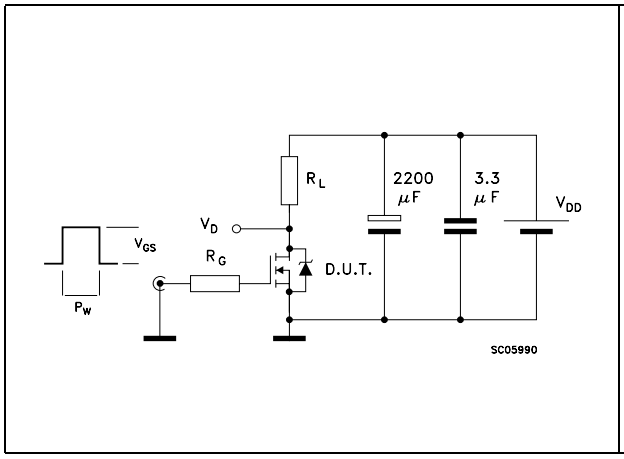


Figure 18. Gate charge test circuit

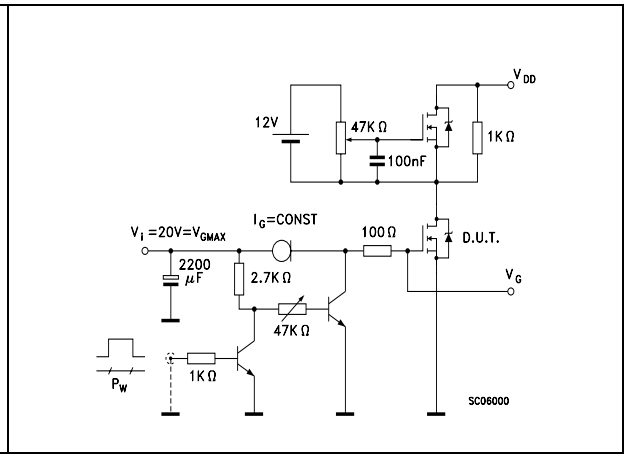
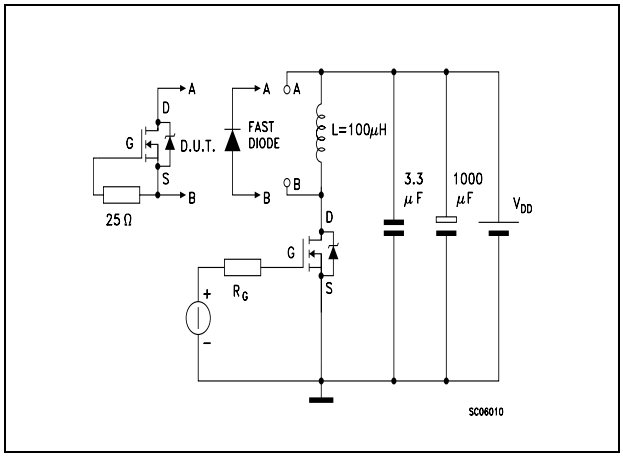


Figure 19. Test circuit for inductive load switching and diode recovery times



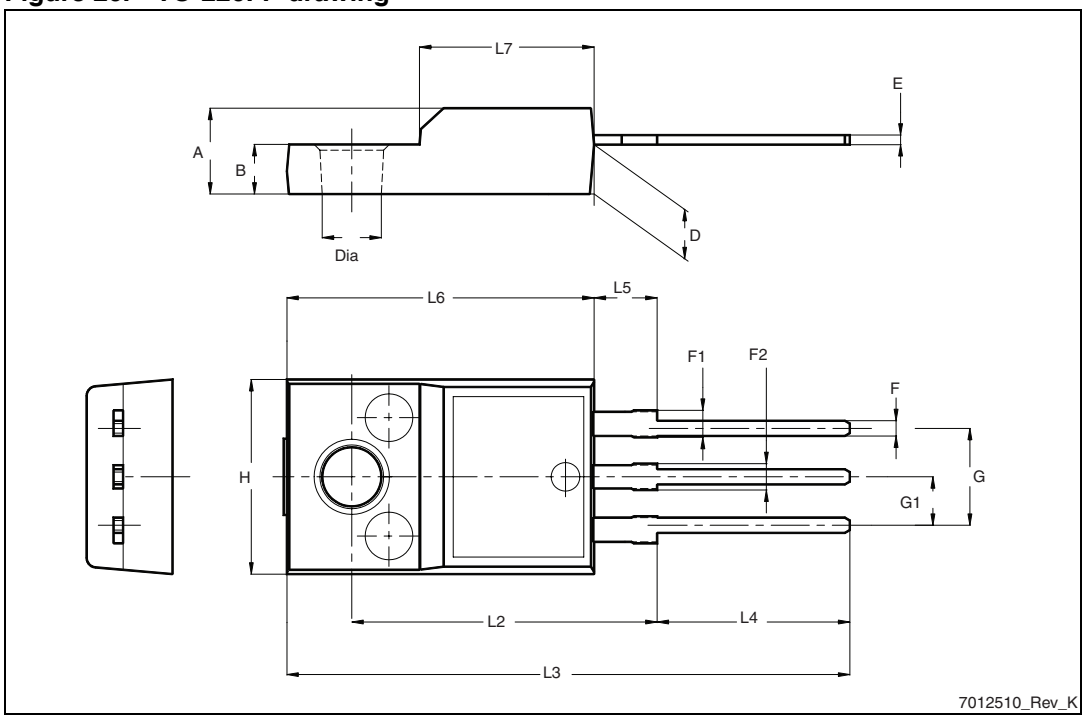
4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 9. TO-220FP mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

Figure 20. TO-220FP drawing



5 Revision history

Table 10. Revision history

Date	Revision	Changes
09-Apr-2010	1	First release.

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