



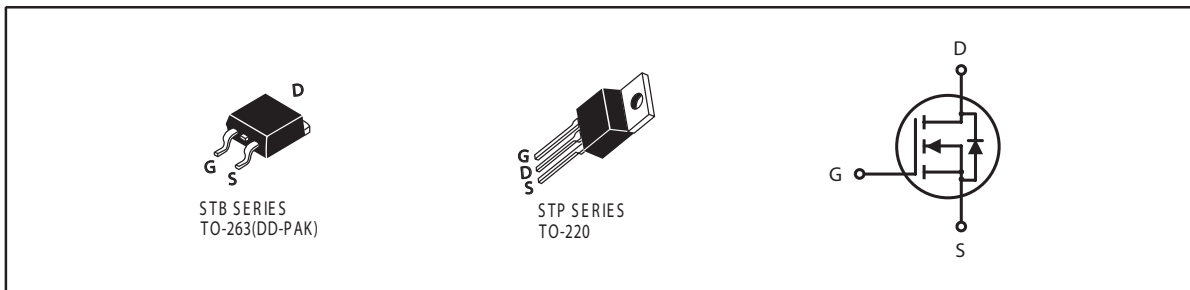
## N-Channel Logic Level Enhancement Mode Field Effect Transistor

### PRODUCT SUMMARY

V <sub>DSS</sub>	I <sub>D</sub>	R <sub>DS(ON)</sub> (mΩ) Max
60V	36A	27 @ V <sub>GS</sub> =10V
		42 @ V <sub>GS</sub> =4.5V

### FEATURES

- Super high dense cell design for extremely low R<sub>DS(ON)</sub>.
- High power and current handling capability.
- TO-220 & TO-263 package.



### ABSOLUTE MAXIMUM RATINGS (T<sub>C</sub>=25°C unless otherwise noted)

Symbol	Parameter	Limit	Units
V <sub>DS</sub>	Drain-Source Voltage	60	V
V <sub>GS</sub>	Gate-Source Voltage	±20	V
I <sub>D</sub>	Drain Current-Continuous <sup>a</sup>	T <sub>C</sub> =25°C	36
		T <sub>C</sub> =70°C	29
I <sub>DM</sub>	-Pulsed <sup>b</sup>	106	A
E <sub>AS</sub>	Avalanche Energy <sup>c</sup>	113	mJ
P <sub>D</sub>	Maximum Power Dissipation <sup>a</sup>	T <sub>C</sub> =25°C	70
		T <sub>C</sub> =70°C	45
T <sub>J</sub> , T <sub>STG</sub>	Operating Junction and Storage Temperature Range	-55 to 150	°C

### THERMAL CHARACTERISTICS

R <sub>θJC</sub>	Thermal Resistance, Junction-to-Case	1.75	°C/W
R <sub>θJA</sub>	Thermal Resistance, Junction-to-Ambient	62.5	°C/W

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## ELECTRICAL CHARACTERISTICS (T<sub>C</sub>=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>OFF CHARACTERISTICS</b>						
B <sub>V</sub> DSS	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =250uA	60			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =48V, V <sub>GS</sub> =0V			1	A
I <sub>GSS</sub>	Gate-Body leakage current	V <sub>GS</sub> = ±20V, V <sub>DS</sub> =0V			±100	nA
<b>ON CHARACTERISTICS</b>						
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250uA	1	2	3	V
R <sub>DS(ON)</sub>	Drain-Source On-State Resistance	V <sub>GS</sub> =10V, I <sub>D</sub> =25A		21	27	m ohm
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =20A		32	42	m ohm
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> =10V, I <sub>D</sub> =25A		26		S
<b>DYNAMIC CHARACTERISTICS <sup>b</sup></b>						
C <sub>ISS</sub>	Input Capacitance	V <sub>DS</sub> =15V, V <sub>GS</sub> =0V f=1.0MHz		1830		pF
C <sub>OSS</sub>	Output Capacitance			182		pF
C <sub>RSS</sub>	Reverse Transfer Capacitance			120		pF
<b>SWITCHING CHARACTERISTICS <sup>b</sup></b>						
t <sub>D(ON)</sub>	Turn-On DelayTime	V <sub>DD</sub> =15V I <sub>D</sub> =1A		45		ns
t <sub>r</sub>	Rise Time			70		ns
t <sub>D(OFF)</sub>	Turn-Off DelayTime	V <sub>GS</sub> =10V R <sub>GEN</sub> =60 ohm		125		ns
t <sub>f</sub>	Fall Time			38		ns
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> =15V, I <sub>D</sub> =25A, V <sub>GS</sub> =10V		28		nC
Q <sub>gs</sub>	Gate-Source Charge	V <sub>DS</sub> =15V, I <sub>D</sub> =25A, V <sub>GS</sub> =10V		4.5		nC
Q <sub>gd</sub>	Gate-Drain Charge			9		nC
<b>DRAIN-SOURCE DIODE CHARACTERISTICS</b>						
I <sub>S</sub>	Maximum Continuous Drain-Source Diode Forward Current				10	A
V <sub>SD</sub>	Diode Forward Voltage	V <sub>GS</sub> =0V, I <sub>S</sub> =10A		0.84	1.3	V
<b>Notes</b>						
a. Pulse Test: Pulse Width ≤ 300us, Duty Ctcle ≤ 2%.						
b. Guaranteed by design, not subject to production testing.						
c. Starting T <sub>J</sub> =25°C, L=1.25mH, V <sub>DD</sub> =30V, V <sub>GS</sub> =10V. (See Figure13)						

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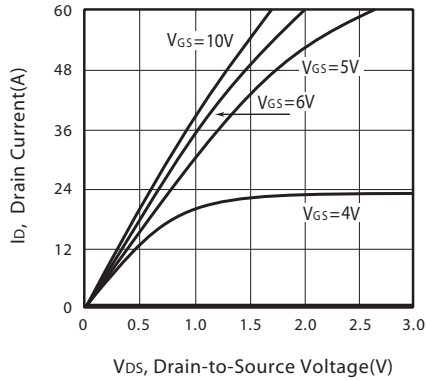


Figure 1. Output Characteristics

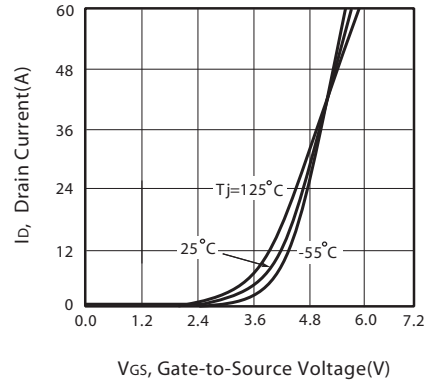


Figure 2. Transfer Characteristics

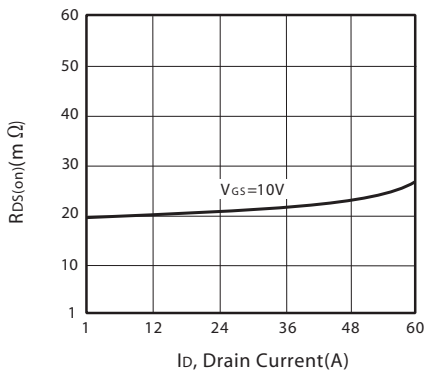


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

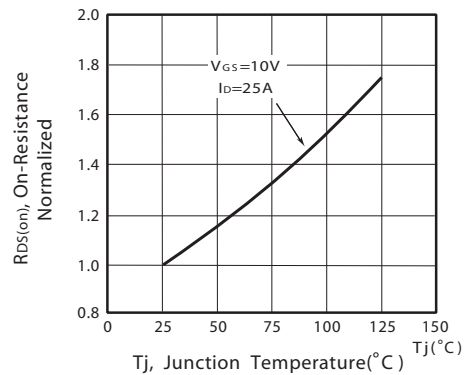


Figure 4. On-Resistance Variation with Drain Current and Temperature

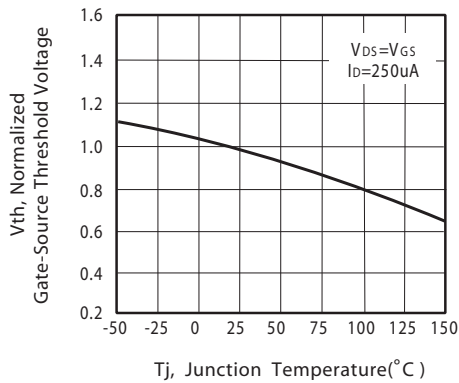


Figure 5. Gate Threshold Variation with Temperature

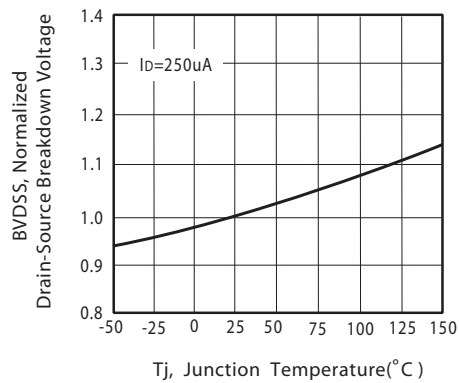


Figure 6. Breakdown Voltage Variation with Temperature

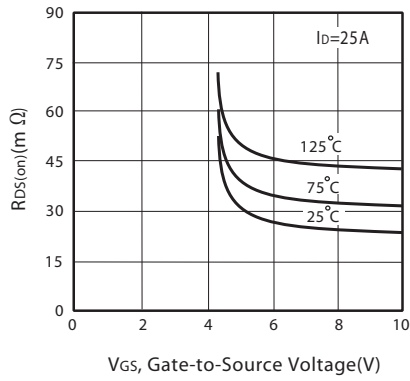


Figure 7. On-Resistance vs. Gate-Source Voltage

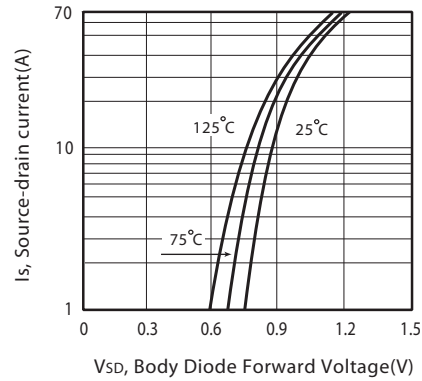


Figure 8. Body Diode Forward Voltage Variation with Source Current

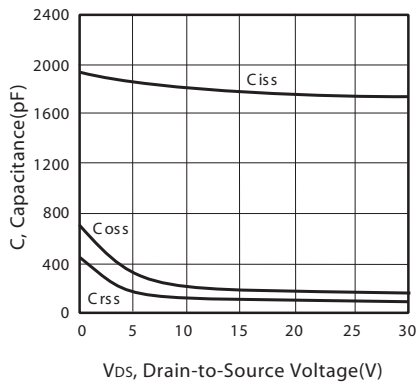


Figure 9. Capacitance

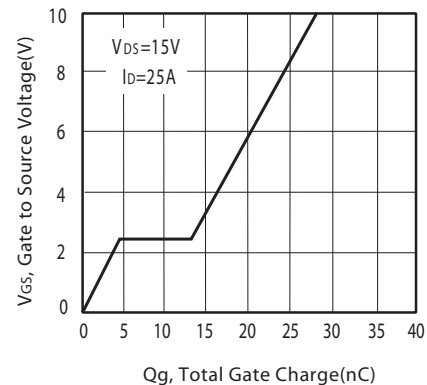


Figure 10. Gate Charge

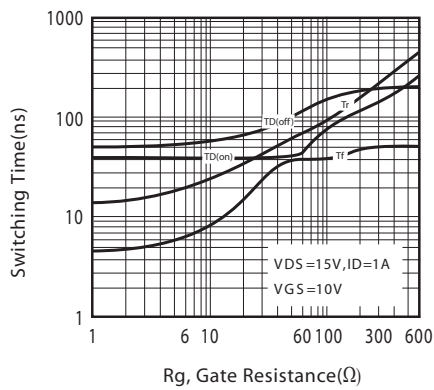


Figure 11. switching characteristics

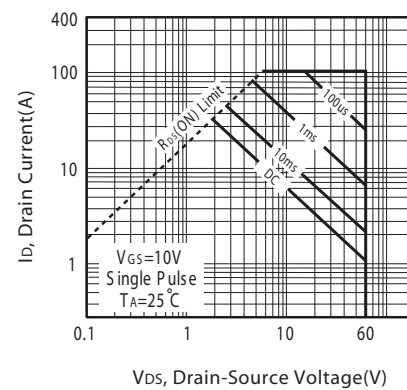
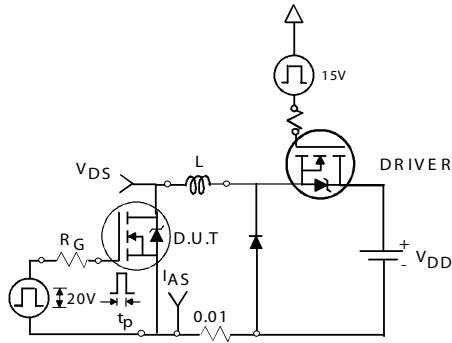
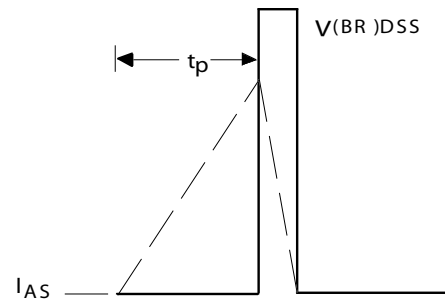


Figure 12. Maximum Safe Operating Area



Unclamped Inductive Test Circuit

Figure 13a.



Unclamped Inductive Waveforms

Figure 13b.

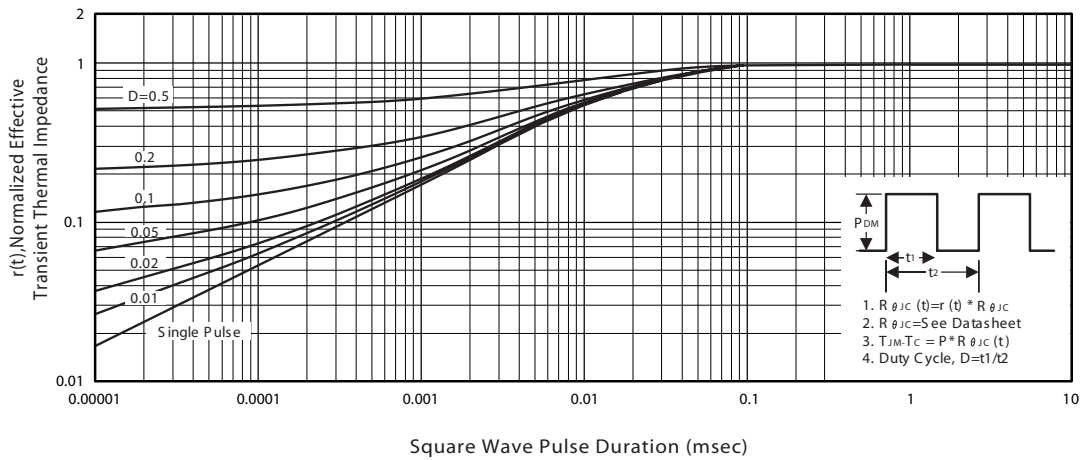


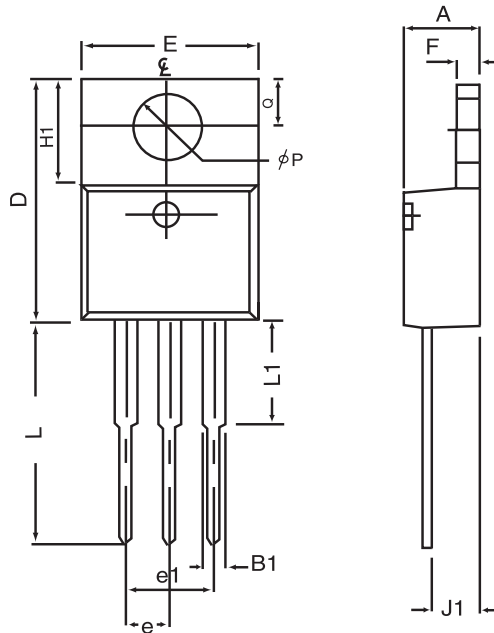
Figure 14. Normalized Thermal Transient Impedance Curve

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## PACKAGE OUTLINE DIMENSIONS

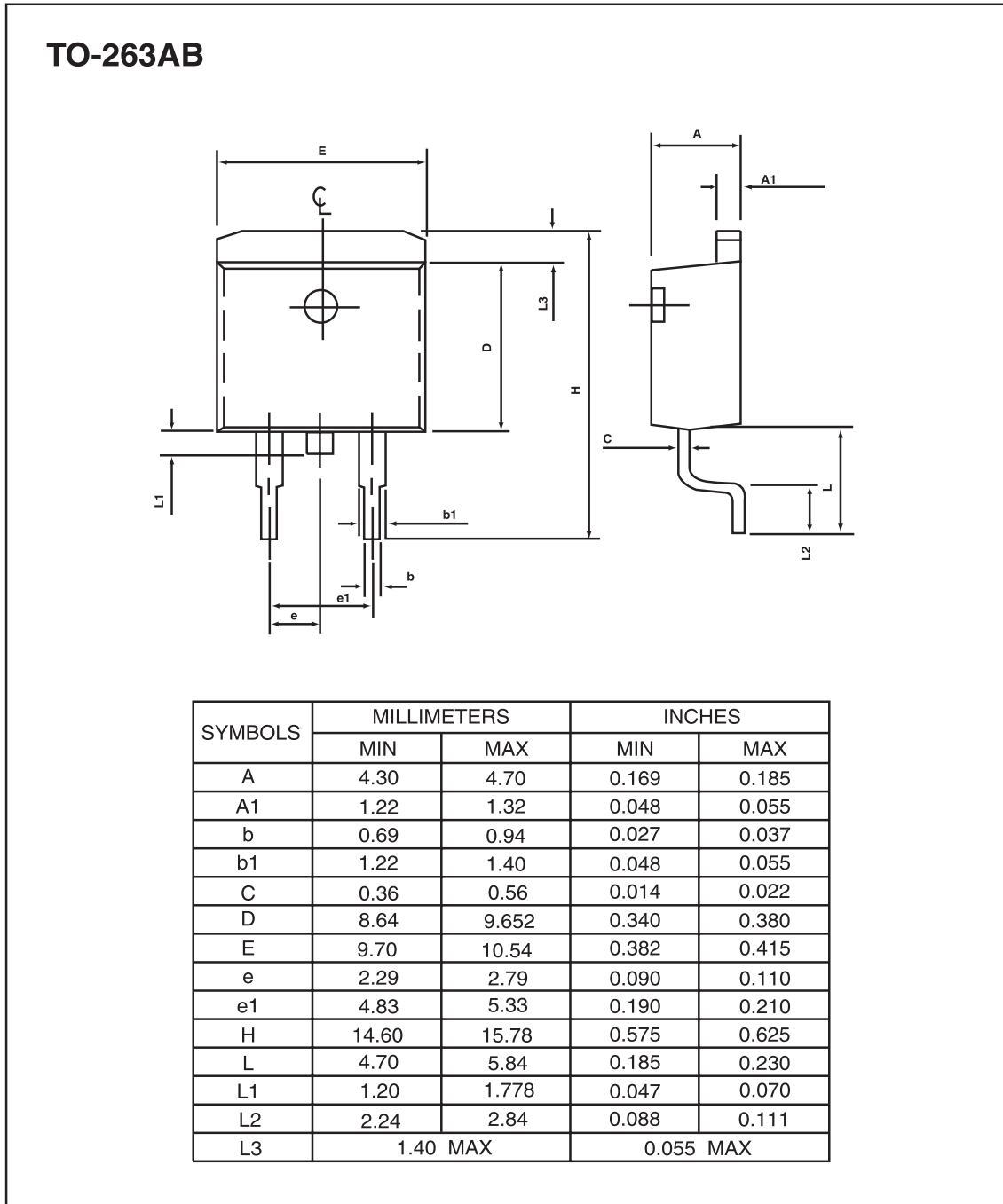
TO-220



SYMBOLS	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.32	4.80	0.170	0.189
B1	1.27	1.65	0.050	0.630
D	14.6	16.00	0.575	0.610
E	9.70	10.41	0.382	0.410
e	2.34	2.74	0.092	0.108
e1	4.68	5.48	0.184	0.216
F	1.14	1.40	0.045	0.055
H1	5.97	6.73	0.235	0.265
J1	2.20	2.79	0.087	0.110
L	12.88	14.22	0.507	0.560
L1	3.00	6.35	0.120	0.250
φP	3.50	3.94	0.138	0.155
Q	2.54	3.05	0.100	0.120

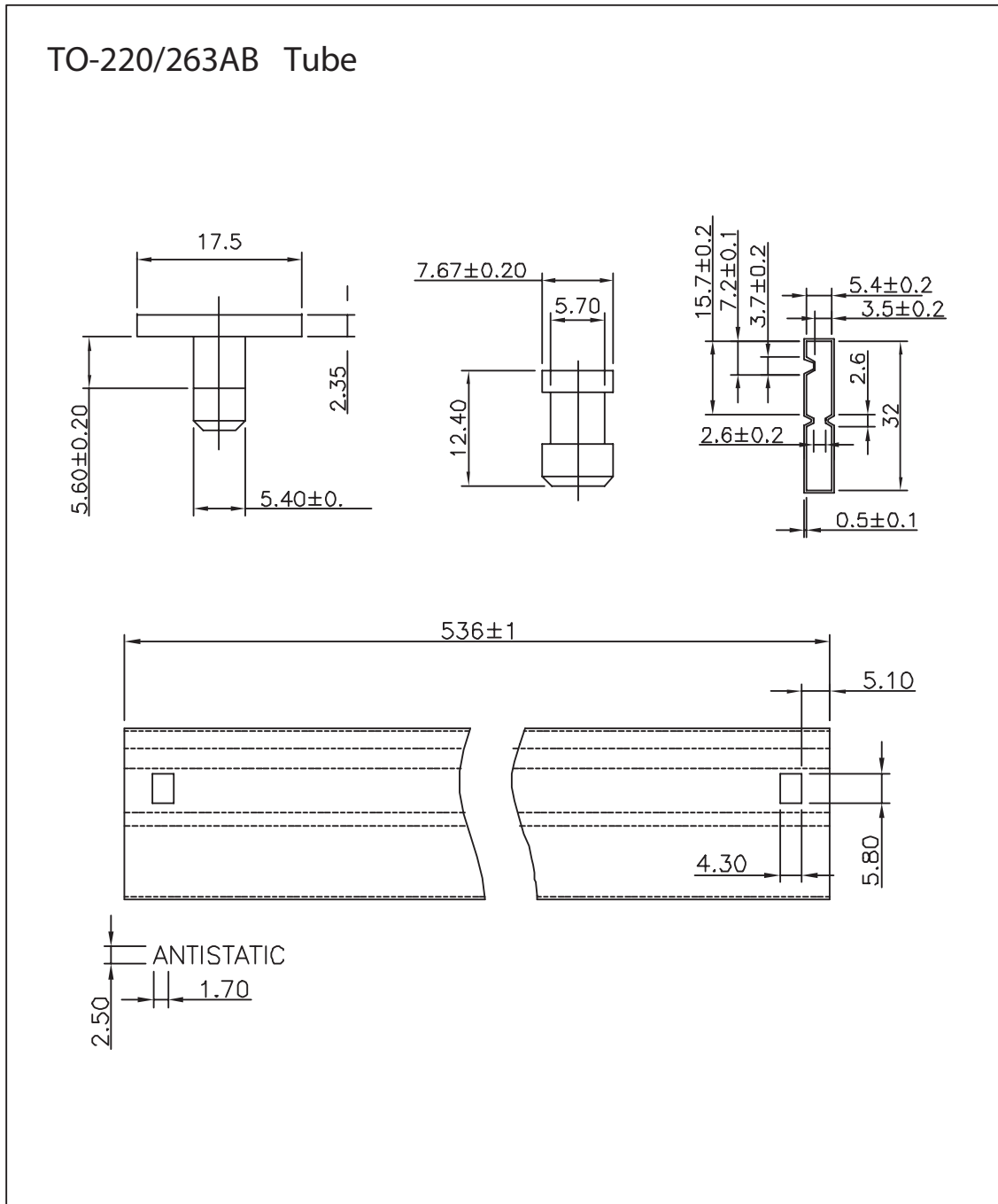
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