



STP60NF03L

N-channel 30V - 0.008 Ω - 60A TO-220
STripFET™ Power MOSFET

General features

Type	V _{DSS}	R _{DS(on)}	I _D
STP60NF03L	30V	<0.01 Ω	60A

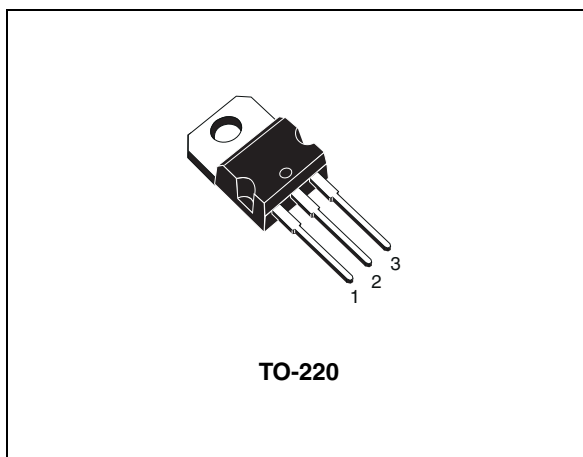
- Low threshold drive

Description

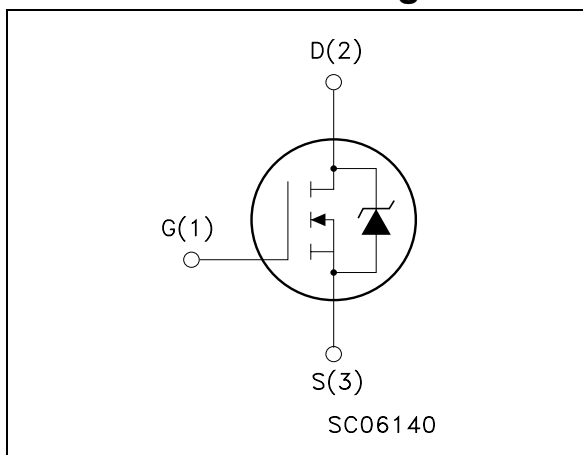
This Power MOSFET is the latest development of STMicroelectronics unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

Applications

- Switching application



Internal schematic diagram



Order codes

Part number	Marking	Package	Packaging
STP60NF03L	P60NF03L	TO-220	Tube

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1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	30	V
V_{DGR}	Drain-gate Voltage ($R_{GS} = 20 \text{ k}\Omega$)	30	V
V_{GS}	Gate- source Voltage	± 20	V
I_D	Drain current (continuous) at $T_C = 25^\circ\text{C}$	60	A
I_D	Drain current (continuous) at $T_C=100^\circ\text{C}$	42	A
$I_{DM}^{(1)}$	Drain current (pulsed)	240	A
P_{TOT}	Total dissipation at $T_C = 25^\circ\text{C}$	100	W
	Derating factor	0.67	W/ $^\circ\text{C}$
$E_{AS}^{(2)}$	Single pulse avalanche energy	650	mJ
T_J T_{stg}	Operating junction temperature Storage temperature	175 -65 to 175	$^\circ\text{C}$

1. Pulse width limited by safe operating area
2. Starting $T_j = 25^\circ\text{C}$, $I_D = 30\text{A}$, $V_{DD} = 20\text{V}$

Table 2. Thermal data

$R_{thj-case}$	Thermal resistance junction-case Max	1.5	$^\circ\text{C}/\text{W}$
R_{thj-a}	Thermal resistance junction-ambient Max	62.5	$^\circ\text{C}/\text{W}$
$R_{thc-sink}$	Thermal resistance case-sink typ	0.5	$^\circ\text{C}/\text{W}$
T_l	Maximum lead temperature for soldering purpose	300	$^\circ\text{C}$

2 Electrical characteristics

($T_{CASE}=25^{\circ}C$ unless otherwise specified)

Table 3. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250 \mu A, V_{GS} = 0$	30			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{Max rating},$ $V_{DS} = \text{Max rating} @ 125^{\circ}C$			1 10	μA μA
I_{GSS}	Gate body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20V$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	1	1.5	2.5	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10V, I_D = 30A$ $V_{GS} = 4.5V, I_D = 30A$		0.008 0.0095	0.010 0.015	Ω Ω

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} > I_{D(on)} \times R_{DS(on)max},$ $I_D = 30A$		60		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 25V, f = 1 \text{ MHz},$ $V_{GS} = 0$		2550 630 215		pF pF pF
$t_{d(on)}$ t_r	Turn-on Delay Time Rise Time	$V_{DD} = 15V, I_D = 30A,$ $R_G = 4.7\Omega, V_{GS} = 4.5V$ (see Figure 12)		40 250		ns ns
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	$V_{DD} = 24V, I_D = 60A$ $V_{GS} = 5V$		43 12 21	58	nC nC nC

1. Pulsed: pulse duration=300 μs , duty cycle 1.5%

Table 5. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
I_{SD}	Source-drain current				60	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				240	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD}=60A, V_{GS}=0$			1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD}=60A,$ $di/dt = 100A/\mu s,$ $V_{DD}=15V, T_j=150^\circ C$ (see Figure 14)		75 100 2.6		ns μC A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

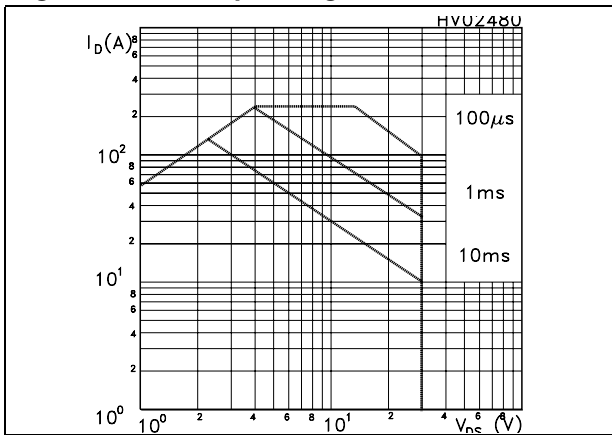


Figure 2. Thermal impedance

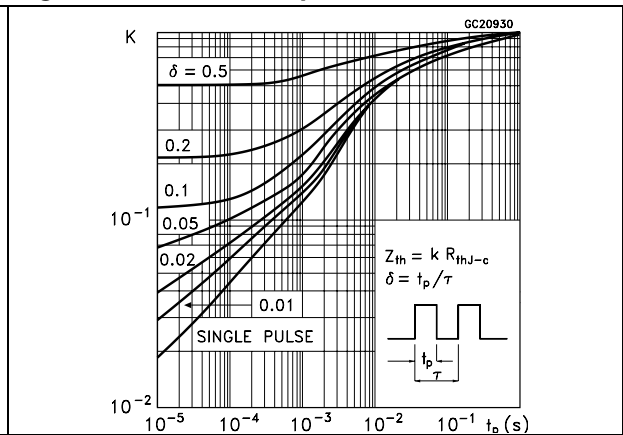


Figure 3. Output characteristics

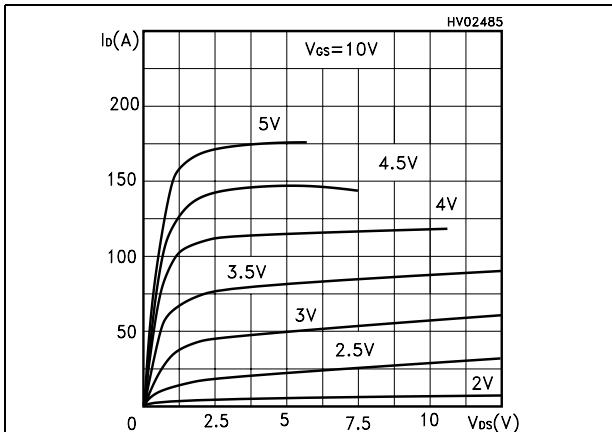


Figure 4. Transfer characteristics

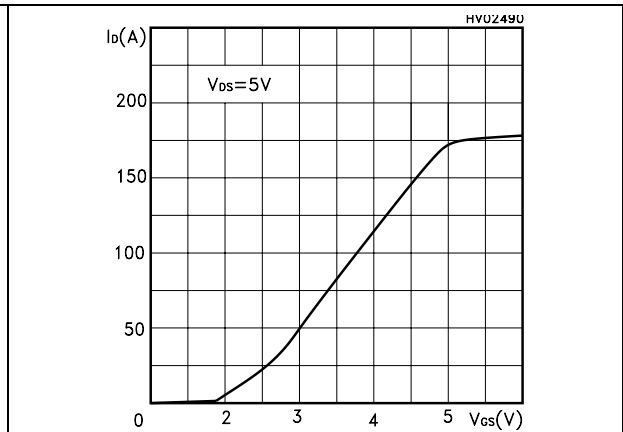


Figure 5. Transconductance

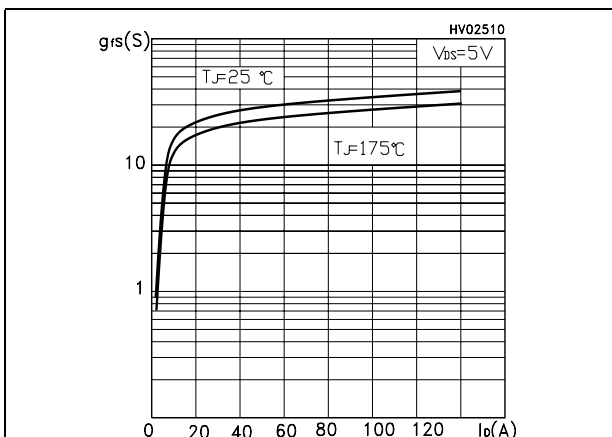


Figure 6. Static drain-source on resistance

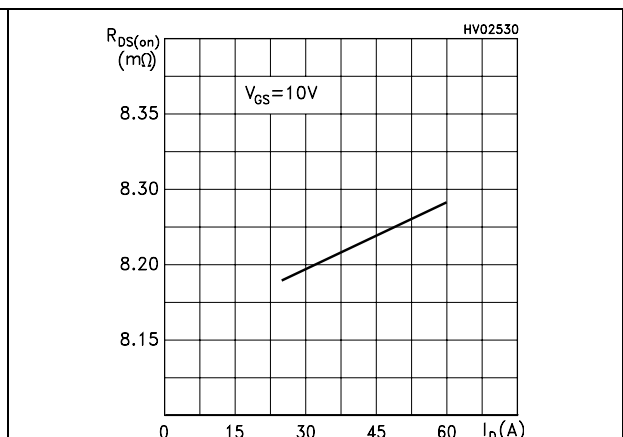


Figure 7. Gate charge vs gate-source voltage Figure 8. Capacitance variations

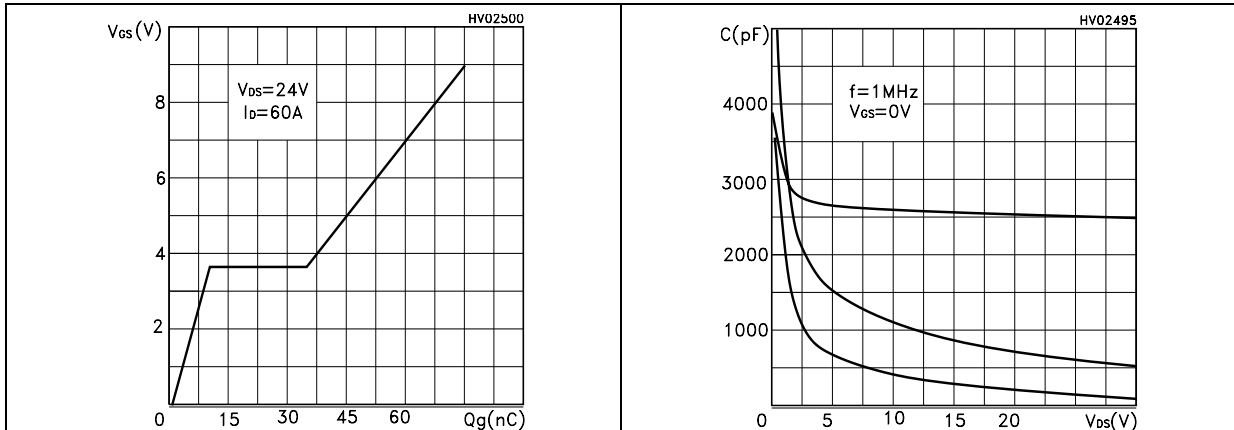


Figure 9. Normalized gate threshold voltage vs temperature Figure 10. Normalized on resistance vs temperature

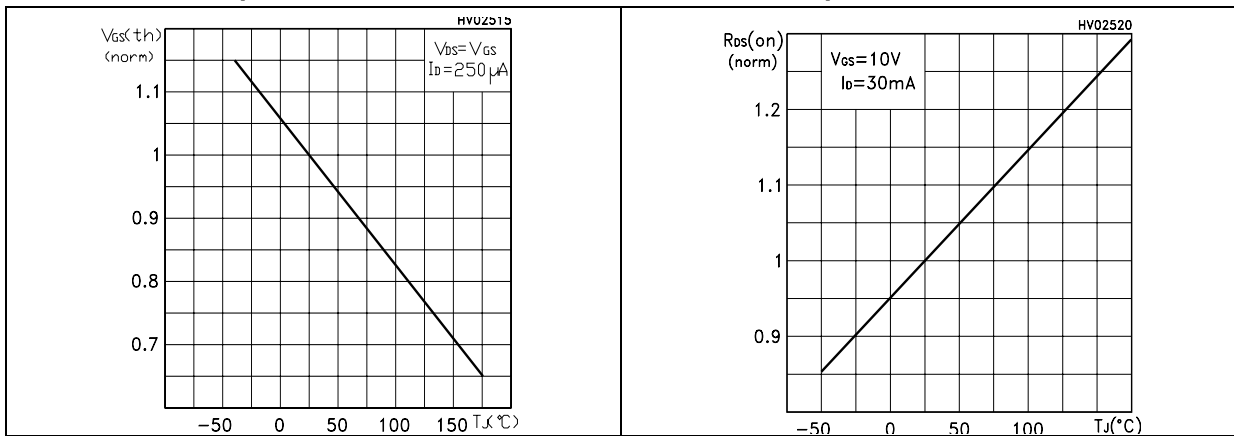
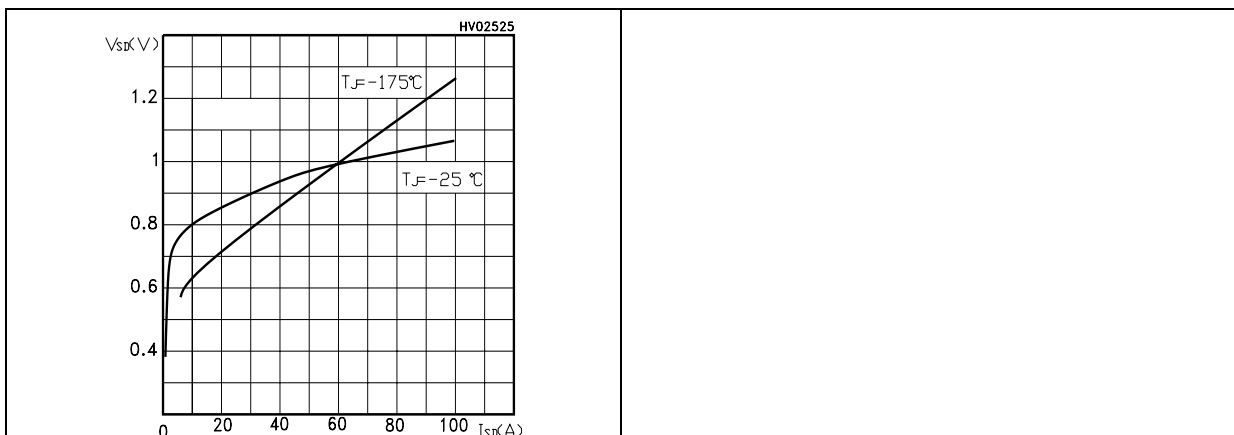


Figure 11. Source-drain diode forward characteristics



3 Test circuit

Figure 12. Switching times test circuit for resistive load

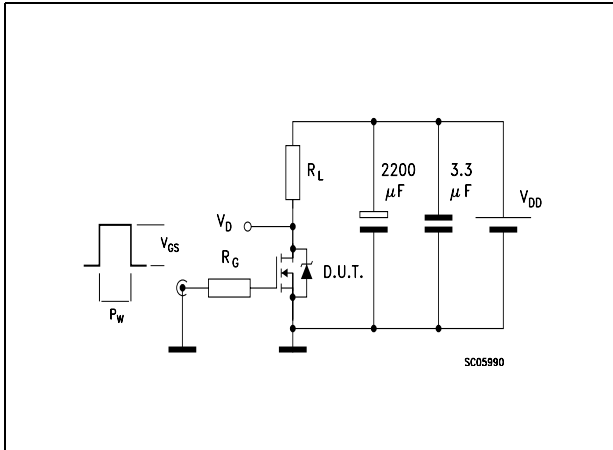


Figure 13. Gate charge test circuit

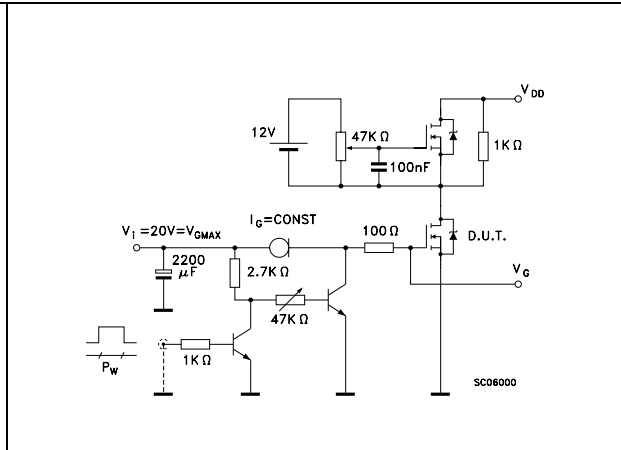


Figure 14. Test circuit for inductive load switching and diode recovery times

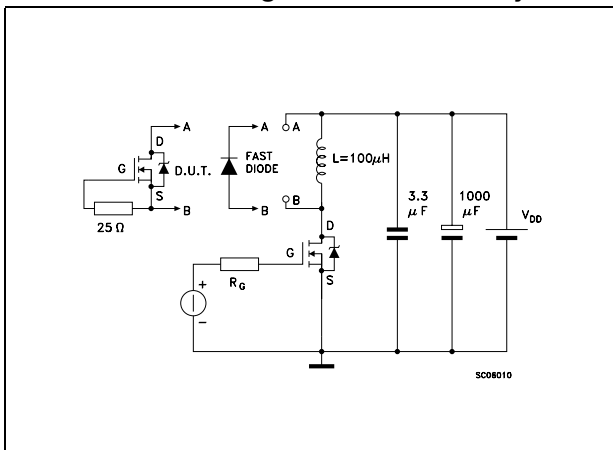


Figure 15. Unclamped Inductive load test circuit

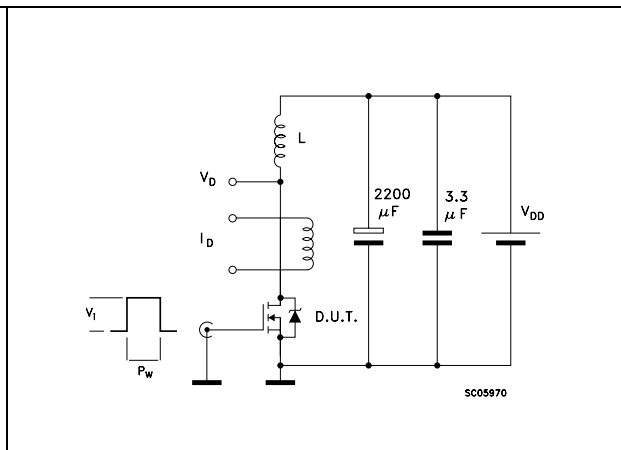


Figure 16. Unclamped inductive waveform

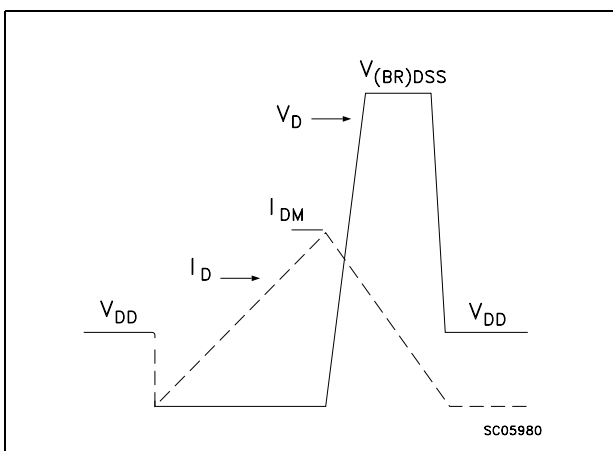
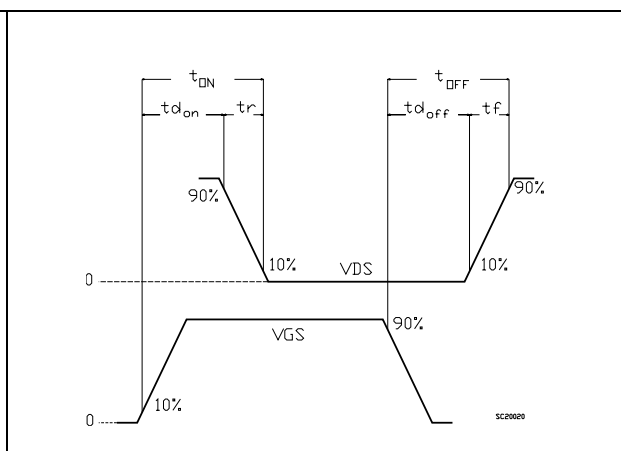


Figure 17. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

5 Revision history

Table 6. Revision history

Date	Revision	Changes
09-Sep-2004	3	Complete document
09-Aug-2006	4	New template, no content change

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