

STP60NH2LL

N-channel 24V - 0.010Ω - 40A TO-220 STripFET™ Power MOSFET

General features

Туре	V _{DSS} (@Tjmax)		
STP60NH2LL	24V	<0.011Ω	40A ⁽¹⁾

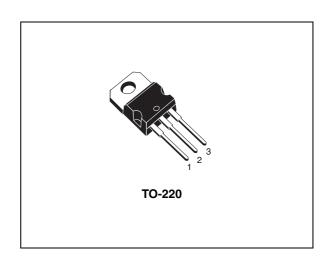
- 1. Value limited by wire bonding
- R_{DS(ON)} * Qg industry's benchmark
- Conduction losses reduced
- Switching losses reduced
- Low threshold device

Description

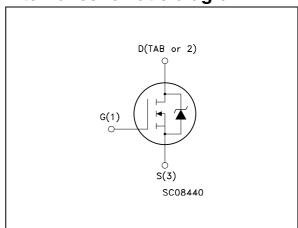
The STP60NH2LL utilizes the latest advanced design rules of ST's proprietary STripFET™ technology. This is suitable for the most demanding DC-DC converter application where high efficiency is to be achieved.

Applications

■ Switching application



Internal schematic diagram



Order codes

Part number	Marking	Package	Packaging	
STP60NH2LL	P60NH2LL	TO-220	Tube	

Contents STP60NH2LL

Contents

1	Electrical ratings	3
2	Electrical characteristics	
3	Test circuit	
4	Appendix A	9
5	Package mechanical data	11
6	Revision history	13

STP60NH2LL Electrical ratings

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit	
V _{spike} ⁽¹⁾	Drain-source Voltage Rating	30	V	
V _{DS}	Drain-source voltage (V _{GS} = 0)	24	V	
V _{GS}	Gate-source voltage	±18	V	
I _D	Drain current (continuous) at T _C = 25°C	40	Α	
I _D	Drain current (continuous) at T _C =100°C	28	Α	
I _{DM} ⁽²⁾	Drain current (pulsed)	160	Α	
P _{TOT}	Total dissipation at T _C = 25°C	60 V		
	Derating factor	0.4	W/°C	
E _{AS} ⁽³⁾	Single pulse avalanche energy	600	mJ	
T _{stg}	Storage temperature	55 to 175	°C	
T _j	Max. operating junction temperature	-55 to 175		

^{1.} Guaranteed when external Rg=4.7 Ω and t_{f} < t_{fmax}

Table 2. Thermal data

R _{thj-case}	Thermal resistance junction-case Max	2.5	°C/W
R _{thj-a}	Thermal resistance junction-ambient Max	100	°C/W
T _I	Maximum lead temperature for soldering purpose	275	°C

^{2.} Pulse width limited by safe operating area

^{3.} Starting $T_j = 25$ °C, $I_D = 20A$, $V_{DD} = 15V$

Electrical characteristics STP60NH2LL

2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Table 3. On/off states

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	$I_D = 25 \text{ mA}, V_{GS} = 0$	24			V
I _{DSS}	Zero gate voltage drain current ($V_{GS} = 0$) $V_{DS} = \text{Max rating}, V_{DS} = \text{Max rating}, V_{CS} = \text{Max rating}, V_{CS$				1 10	μ Α μ Α
I _{GSS}	Gate body leakage current $V_{GS} = \pm 16V$				± 100	nA
V _{GS(th)}	Gate threshold voltage $V_{DS} = V_{GS}$, $I_D = 250\mu A$		1			٧
R _{DS(on)}	Static drain-source on resistance	V_{GS} = 10V, I_{D} = 20A V_{GS} = 4.5V, I_{D} = 20A		0.010 0.012	0.011 0.0135	Ω

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
g _{fs} ⁽¹⁾	Forward transconductance	V _{DS} = 10V, I _D = 10A		18		S
C _{iss} C _{oss} C _{rss}	nput capacitance Dutput capacitance Reverse transfer capacitance V _{DS} =25V, f=1 MHz, V _{GS} =0			990 385 40		pF pF pF
t _{d(on)} t _r t _{d(off)} t _f	Turn-on delay time rise time Turn-off delay time fall time	$V_{DD} = 10 \text{ V}, I_{D} = 20 \text{ A}$ $R_{G} = 4.7 \Omega, V_{GS} = 4.5 \text{ V}$ (see Figure 13)		5 56 13 10		ns ns ns
Q _g Q _{gs} Q _{gd}	Total gate charge Gate-source charge Gate-drain charge	$0.44 \le V_{DD} = 10V, I_D = 40A$ $V_{GS} = 4.5V$		8.7 4.2 2.4	27	nC nC nC
Q _{oss} ⁽²⁾	Output charge	V _{DS} = 16 V, V _{GS} = 0 V		7.6		nC
R_g	Gate input resistance	f=1MHz Gate DC Bias=0 test signal level=20mV open drain		1.3		Ω

^{1.} Pulsed: pulse duration=300µs, duty cycle 1.5%

^{2.} Qoss = $Coss^*\Delta Vin$, Coss = Cgd + Cds. See *Chapter 4: Appendix A*

Table 5. Source drain diode

Symbol	Parameter	Test conditions	Min.	Тур.	Max	Unit
I _{SD}	Source-drain current				40	Α
I _{SDM}	Source-drain current (pulsed)				160	Α
V _{SD} ⁽¹⁾	Forward on voltage	I _{SD} =20A, V _{GS} =0			1.3	٧
t _{rr} Q _{rr} I _{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I _{SD} =40A, di/dt = 100A/μs, V _{DD} =15V, Tj=150°C (see Figure 15)		32.5 28 1.7		ns μC Α

^{1.} Pulsed: pulse duration=300µs, duty cycle 1.5%

Electrical characteristics STP60NH2LL

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

Figure 2. Thermal impedance

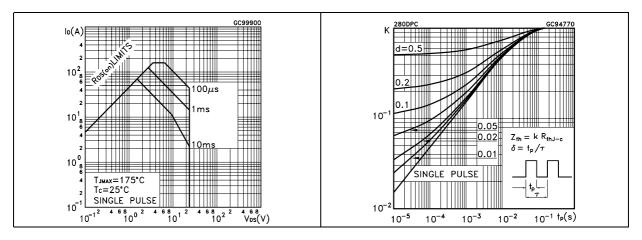


Figure 3. Output characteristics

Figure 4. Transfer characteristics

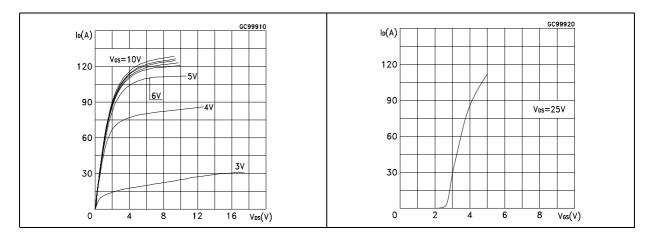


Figure 5. Transconductance

Figure 6. Static drain-source on resistance

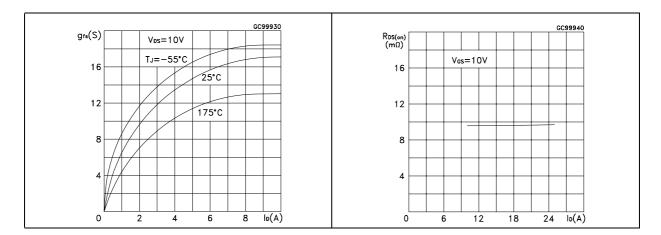


Figure 7. Gate charge vs. gate-source voltage Figure 8. Capacitance variations

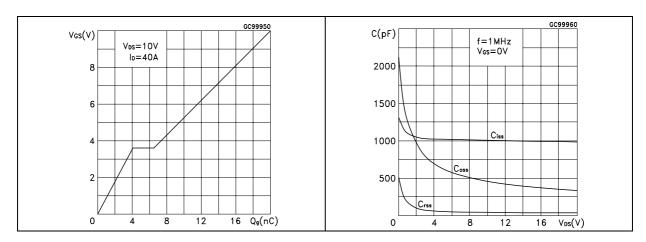


Figure 9. Normalized gate threshold voltage Figure 10. Normalized on resistance vs. vs. temperature temperature

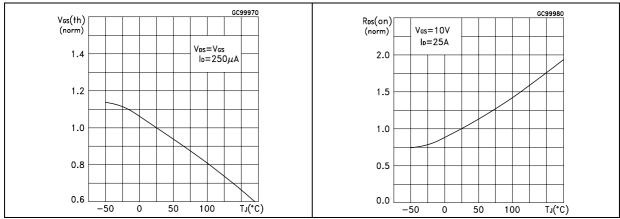
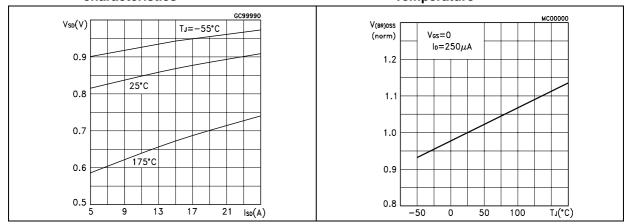


Figure 11. Source-drain diode forward characteristics

Figure 12. Normalized Breakdown Voltage vs. Temperature



Test circuit STP60NH2LL

3 Test circuit

Figure 13. Switching times test circuit for resistive load

Figure 14. Gate charge test circuit

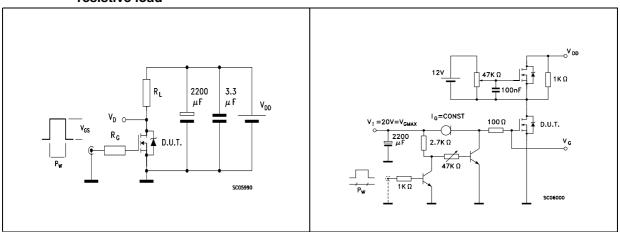


Figure 15. Test circuit for inductive load switching and diode recovery times

Figure 16. Unclamped Inductive load test circuit

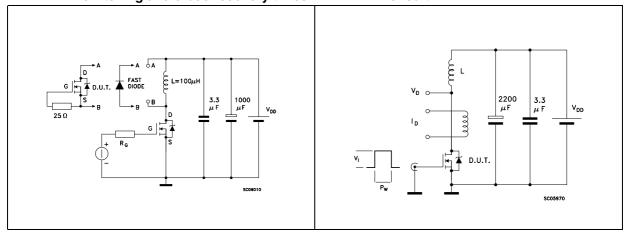
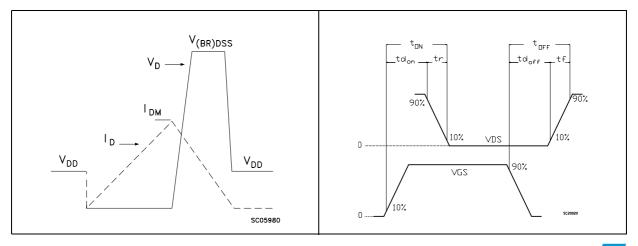


Figure 17. Unclamped inductive waveform

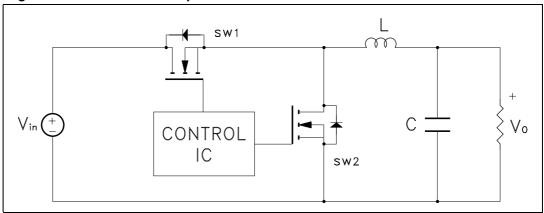
Figure 18. Switching time waveform



STP60NH2LL Appendix A

4 Appendix A

Figure 19. Buck converter: power losses estimation



The power losses associated with the FETs in a synchronous buck converter can be estimated using the equations shown in the table below. The formulas give a good approximation, for the sake of performance comparison, of how different pairs of devices affect the converter efficiency. However a very important parameter, the working temperature, is not considered. The real device behavior is really dependent on how the heat generated inside the devices is removed to allow for a safer working junction temperature.

- The low side (SW2) device requires:
- Very low R_{DS(on)} to reduce conduction losses
- Small Qgls to reduce the gate charge losses
- Small Coss to reduce losses due to output capacitance
- Small Qrr to reduce losses on SW1 during its turn-on
- The Cgd/Cgs ratio lower than Vth/Vgg ratio especially with low drain to source
- voltage to avoid the cross conduction phenomenon;
- The high side (SW1) device requires:
- Small Rg and Ls to allow higher gate current peak and to limit the voltage feedback on the gate
- Small Qg to have a faster commutation and to reduce gate charge losses
- Low R_{DS(on)} to reduce the conduction losses.

Appendix A STP60NH2LL

Table 6. Power losses calculation

		High side switching (SW1)	Low side switch (SW2)
Pconduction		$R_{_{ m DS(on)SW1}}*I_{ m L}^2*\delta$	$R_{DS(on)SW2} * I_L^2 * (1 - \delta)$
Pswitching		$V_{\text{in}} * (Q_{\text{gsth(SW1)}} + Q_{\text{gd(SW1)}}) * f * \frac{I_L}{I_g}$	Zero Voltage Switching
Pdiode	Recovery (1)	Not applicable	$V_{in} * Q_{rr(SW2)} * f$
ruiode	Conductio n	Not applicable	$V_{f(SW2)} * I_L * t_{deadtime} * f$
Pgate(Q _G)		$Q_{g(SW1)}*V_{gg}*f$	$Q_{gls(SW2)}*V_{gg}*f$
P _{Qoss}		$\frac{V_{in} *Q_{oss(SW1)} *f}{2}$	$\frac{V_{in} *Q_{oss(SW2)} *f}{2}$

^{1.} Dissipated by SW1 during turn-on

Table 7. Parameters meaning

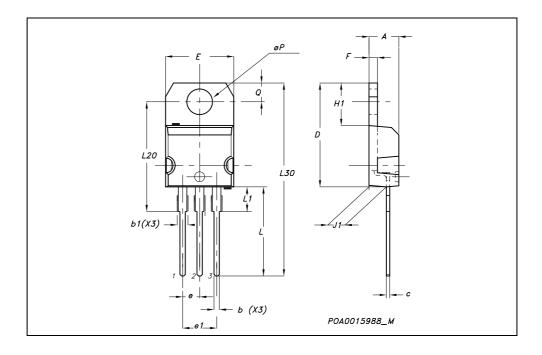
Parameter	Meaning		
d	Duty-cycle		
Q _{gsth}	Post threshold gate charge		
Q_{gls}	Third quadrant gate charge		
Pconduction	On state losses		
Pswitching	On-off transition losses		
Pdiode	Conduction and reverse recovery diode losses		
Pgate	Gate drive losses		
P _{Qoss}	Output capacitance losses		

5 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

TO-220 MECHANICAL DATA

DIM.		mm.			inch	
DINI.	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
Α	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.15		1.70	0.045		0.066
С	0.49		0.70	0.019		0.027
D	15.25		15.75	0.60		0.620
E	10		10.40	0.393		0.409
е	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.052
H1	6.20		6.60	0.244	0.2	
J1	2.40		2.72	0.094	0.10	
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
øΡ	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116



STP60NH2LL Revision history

6 Revision history

Table 8. Revision history

Date	Revision	Changes
31-May-2005	1	First release.
06-Sep-2006	2	The document has been reformatted.
31-Jan-2007	3	Typo mistake on <i>Table 1</i> .

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