

**N-Channel Logic Level Enhancement Mode Field Effect Transistor****PRODUCT SUMMARY**

V <sub>DSS</sub>	I <sub>D</sub>	R <sub>DS(ON)</sub> (mΩ) Typ
60V	29A	22 @ V <sub>GS</sub> =10V

**FEATURES**

- Super high dense cell design for extremely low R<sub>DS(ON)</sub>.
- High power and current handling capability.
- TO-220F package.

**ABSOLUTE MAXIMUM RATINGS (T<sub>C</sub>=25°C unless otherwise noted)**

Symbol	Parameter	Limit	Units
V <sub>DS</sub>	Drain-Source Voltage	60	V
V <sub>GS</sub>	Gate-Source Voltage	±20	V
I <sub>D</sub>	Drain Current-Continuous <sup>a</sup>	T <sub>C</sub> =25°C	29
		T <sub>C</sub> =70°C	24
I <sub>DM</sub>	-Pulsed <sup>b</sup>	90	A
E <sub>AS</sub>	Avalanche Energy <sup>d</sup>	110	mJ
P <sub>D</sub>	Maximum Power Dissipation <sup>a</sup>	T <sub>C</sub> =25°C	46
		T <sub>C</sub> =70°C	32
T <sub>J</sub> , T <sub>STG</sub>	Operating Junction and Storage Temperature Range	-55 to 175	°C

**THERMAL CHARACTERISTICS**

R <sub>θJC</sub>	Thermal Resistance, Junction-to-Case	3.25	°C/W
R <sub>θJA</sub>	Thermal Resistance, Junction-to-Ambient	62.5	°C/W

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## ELECTRICAL CHARACTERISTICS (T<sub>C</sub>=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>OFF CHARACTERISTICS</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V , I <sub>D</sub> =250uA	60			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =48V , V <sub>GS</sub> =0V			1	uA
I <sub>GSS</sub>	Gate-Body leakage current	V <sub>GS</sub> = ±20V , V <sub>DS</sub> =0V			±100	nA
<b>ON CHARACTERISTICS</b>						
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250uA	1.7	2.2	3	V
R <sub>DS(ON)</sub>	Drain-Source On-State Resistance	V <sub>GS</sub> =10V , I <sub>D</sub> =14.5A		22	28	m ohm
		V <sub>GS</sub> =4.5V , I <sub>D</sub> =11A		29	39	m ohm
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> =10V , I <sub>D</sub> =14.5A		33		S
<b>DYNAMIC CHARACTERISTICS <sup>c</sup></b>						
C <sub>ISS</sub>	Input Capacitance	V <sub>DS</sub> =30V, V <sub>GS</sub> =0V f=1.0MHz		1800		pF
C <sub>OSS</sub>	Output Capacitance			133		pF
C <sub>RSS</sub>	Reverse Transfer Capacitance			102		pF
<b>SWITCHING CHARACTERISTICS <sup>c</sup></b>						
t <sub>D(ON)</sub>	Turn-On DelayTime	V <sub>DD</sub> =30V I <sub>D</sub> =1A V <sub>GS</sub> =10V R <sub>GEN</sub> =6 ohm		35.5		ns
t <sub>r</sub>	Rise Time			30		ns
t <sub>D(OFF)</sub>	Turn-Off DelayTime			61		ns
t <sub>f</sub>	Fall Time			12.5		ns
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> =30V, I <sub>D</sub> =14.5A, V <sub>GS</sub> =10V		28		nC
		V <sub>DS</sub> =30V, I <sub>D</sub> =14.5A, V <sub>GS</sub> =4.5V		14		nC
Q <sub>gs</sub>	Gate-Source Charge	V <sub>DS</sub> =30V, I <sub>D</sub> =14.5A, V <sub>GS</sub> =10V		3.5		nC
Q <sub>gd</sub>	Gate-Drain Charge			7		nC
<b>DRAIN-SOURCE DIODE CHARACTERISTICS</b>						
V <sub>SD</sub>	Diode Forward Voltage	V <sub>GS</sub> =0V, I <sub>S</sub> =5A		0.79	1.3	V
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> =0V, I <sub>S</sub> =50A, dI <sub>F</sub> / dt = 100A/us		49		ns
Q <sub>rr</sub>	Reverse Recovery Charge			54		nC
<b>Notes</b> a.Surface Mounted on FR4 Board, t ≤ 10sec. b.Pulse Test:Pulse Width ≤ 300us, Duty Cycle ≤ 2%. c.Guaranteed by design, not subject to production testing. d.Starting T <sub>J</sub> =25°C, L=0.5mH, V <sub>DD</sub> = 30V.(See Figure13)						

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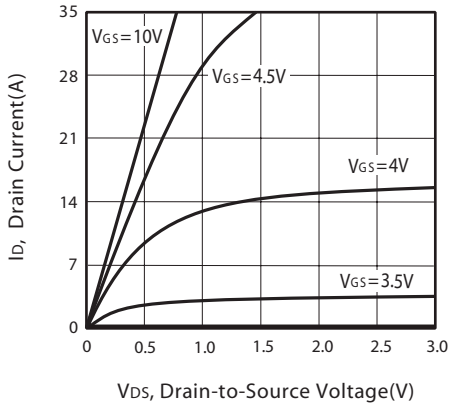


Figure 1. Output Characteristics

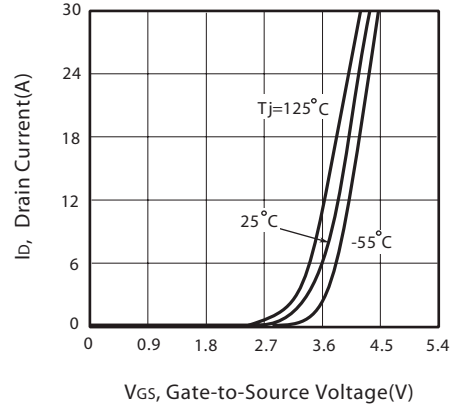


Figure 2. Transfer Characteristics

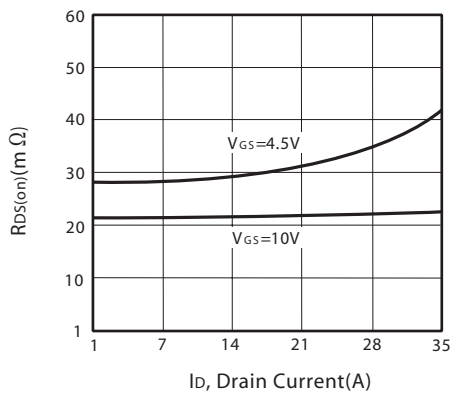


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

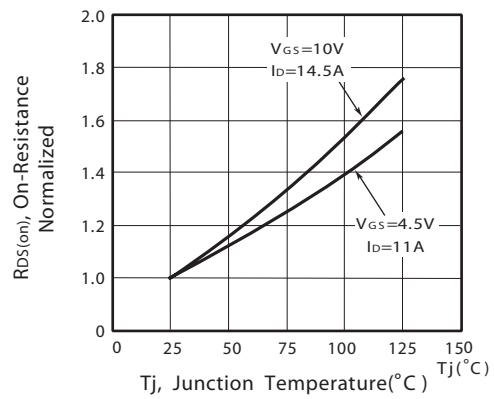


Figure 4. On-Resistance Variation with Drain Current and Temperature

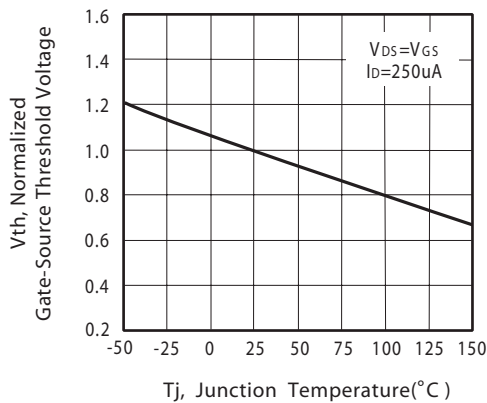


Figure 5. Gate Threshold Variation with Temperature

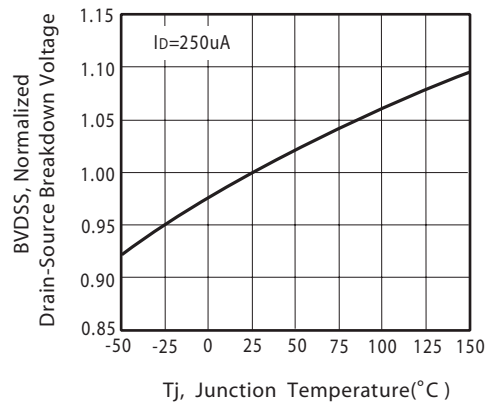


Figure 6. Breakdown Voltage Variation with Temperature

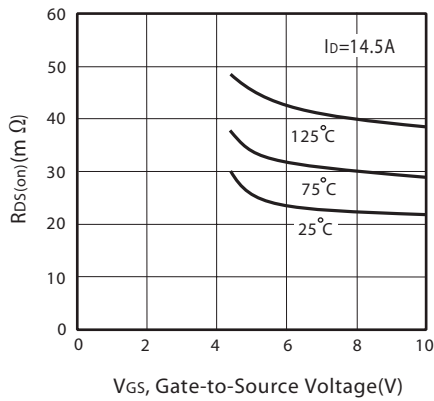


Figure 7. On-Resistance vs. Gate-Source Voltage

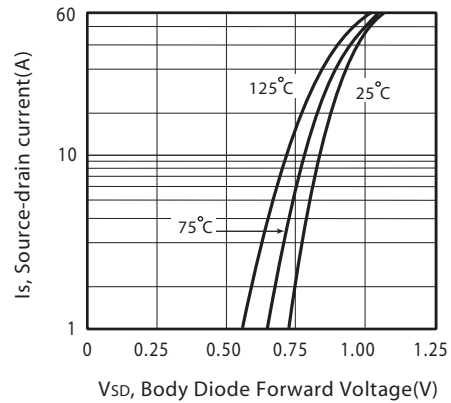


Figure 8. Body Diode Forward Voltage Variation with Source Current

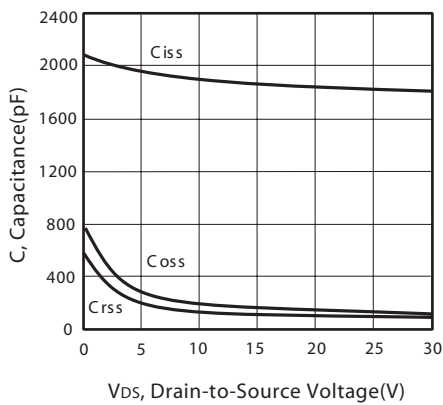


Figure 9. Capacitance

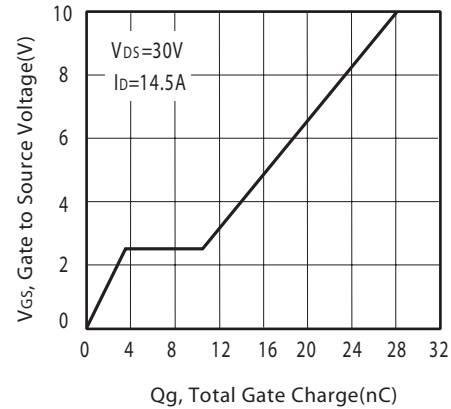


Figure 10. Gate Charge

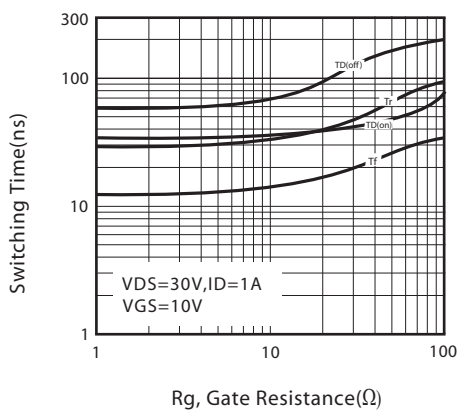


Figure 11. switching characteristics

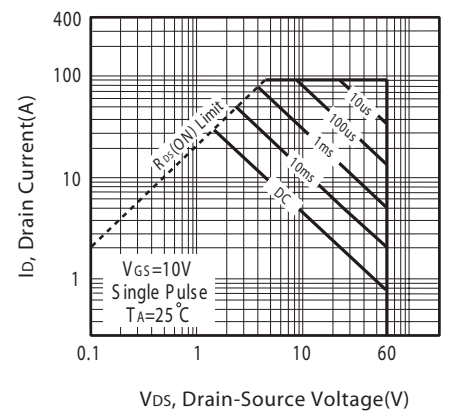
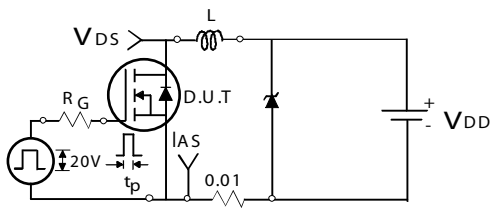
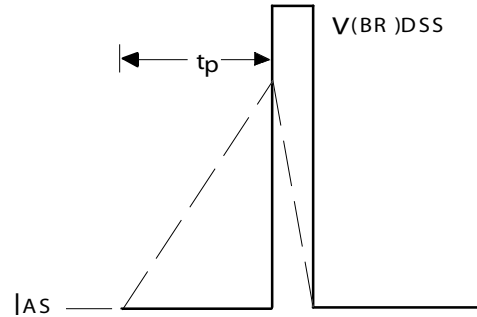


Figure 12. Maximum Safe Operating Area



Unclamped Inductive Test Circuit

Figure 13a.



Unclamped Inductive Waveforms

Figure 13b.

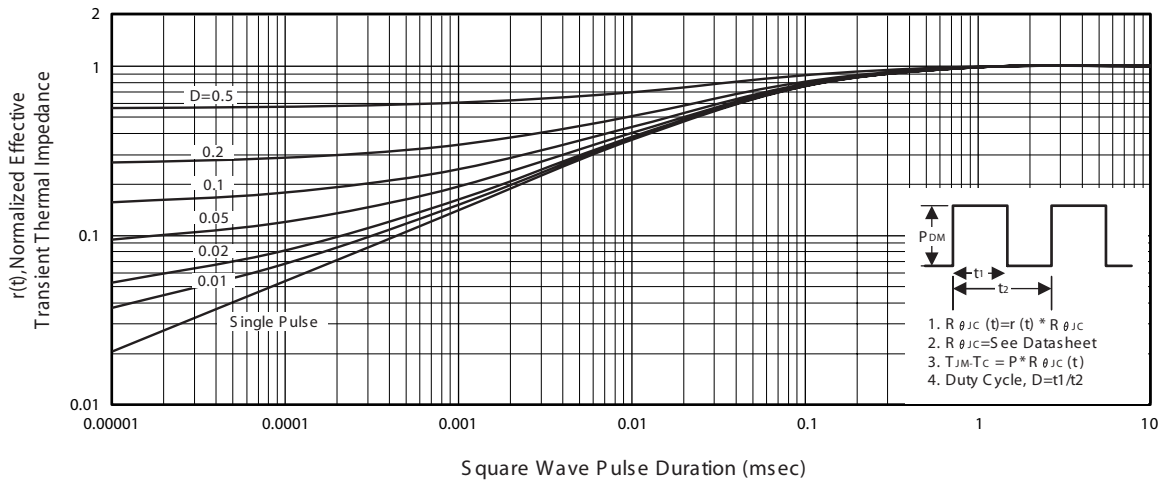
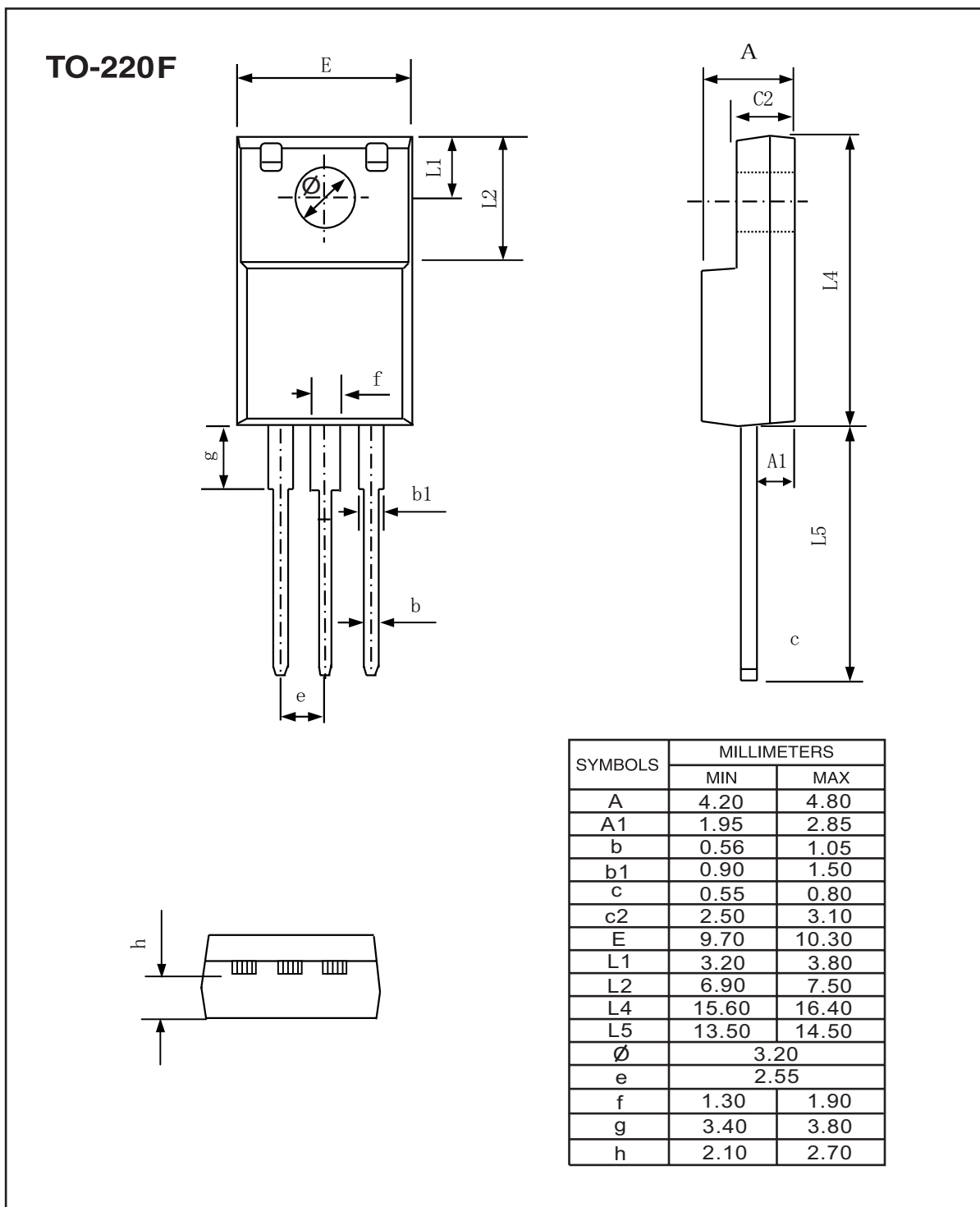


Figure 14. Normalized Thermal Transient Impedance Curve

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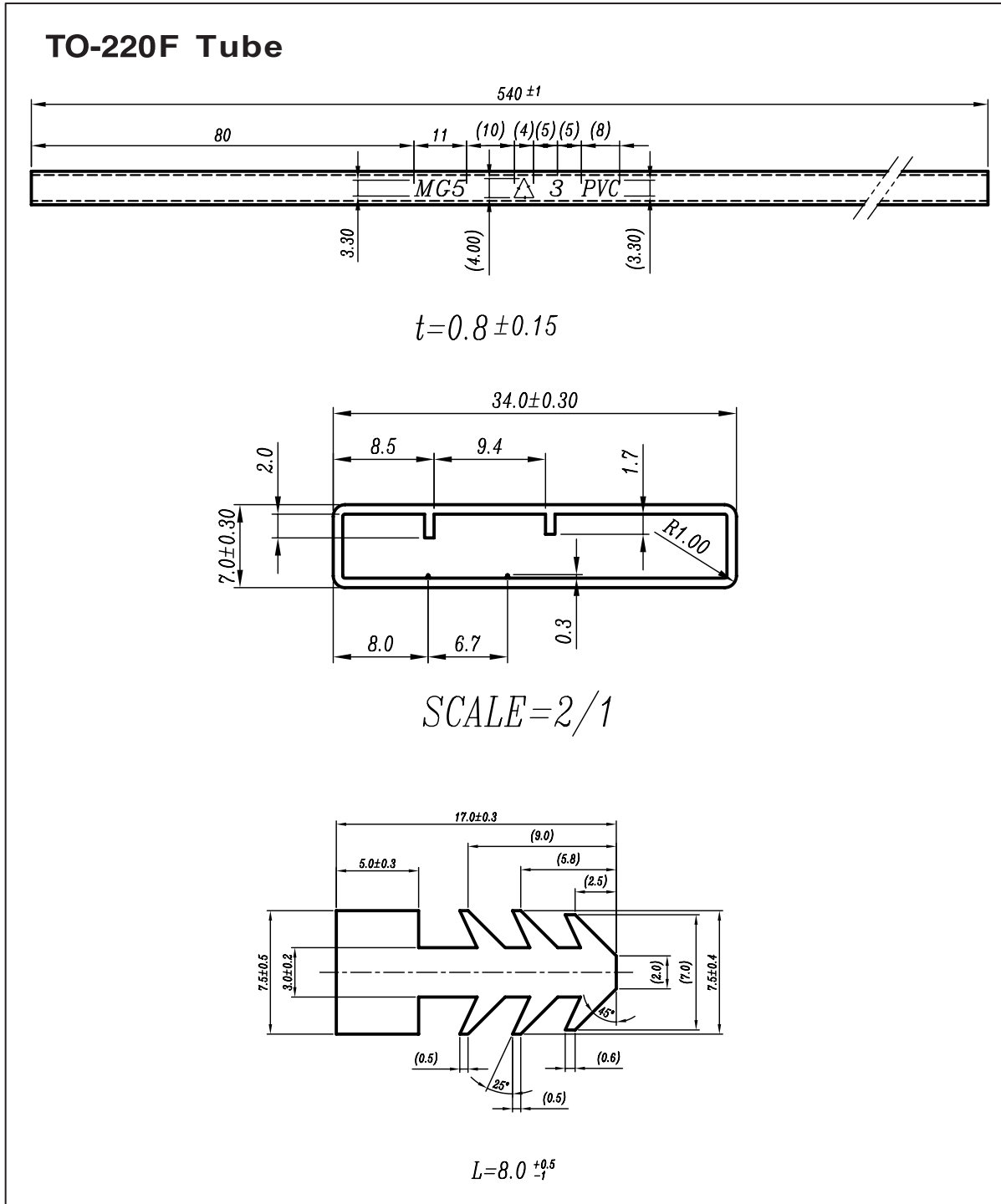
## PACKAGE OUTLINE DIMENSIONS



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