



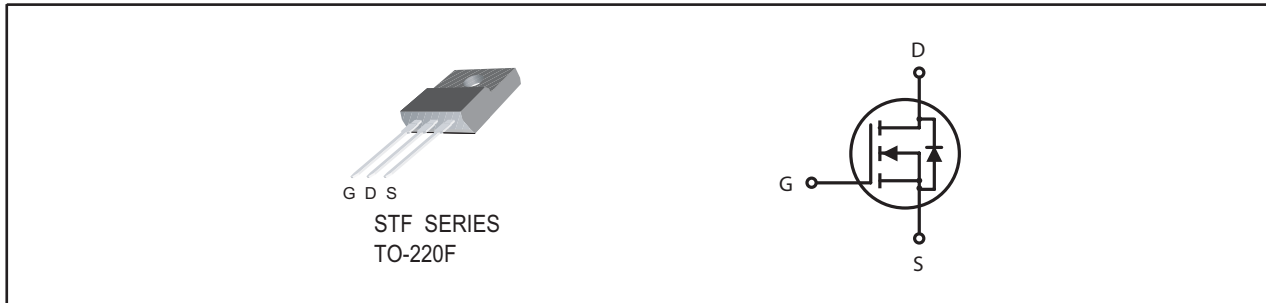
N-Channel Enhancement Mode Field Effect Transistor

PRODUCT SUMMARY

| V _{DSS} | I _D | R _{DS(ON)} (mΩ) Max |
|------------------|----------------|------------------------------|
| 60V | 22A | 19 @ V _{GS} =10V |
| | | 29 @ V _{GS} =4.5V |

FEATURES

- Super high dense cell design for low R_{DS(ON)}.
- Rugged and reliable.
- TO-220F Package.



ABSOLUTE MAXIMUM RATINGS (T_C=25°C unless otherwise noted)

| Symbol | Parameter | Limit | Units |
|-----------------------------------|--|----------------------|-------|
| V _{DS} | Drain-Source Voltage | 60 | V |
| V _{GS} | Gate-Source Voltage | ±20 | V |
| I _D | Drain Current-Continuous ^a | T _C =25°C | 22 |
| | | T _C =70°C | 17.7 |
| I _{DM} | -Pulsed ^b | 66 | A |
| E _{AS} | Avalanche Energy ^d | 182 | mJ |
| P _D | Maximum Power Dissipation ^a | T _C =25°C | 21 |
| | | T _C =70°C | 13.3 |
| T _J , T _{STG} | Operating Junction and Storage Temperature Range | -55 to 150 | °C |

THERMAL CHARACTERISTICS

| | | | |
|------------------|--|----|------|
| R _{θJC} | Thermal Resistance, Junction-to-Case ^a | 6 | °C/W |
| R _{θJA} | Thermal Resistance, Junction-to-Ambient ^a | 65 | °C/W |

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ELECTRICAL CHARACTERISTICS (T_A=25°C unless otherwise noted)

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|----------------------------------|--|-----|------|------|-------|
| OFF CHARACTERISTICS | | | | | | |
| BV _{DSS} | Drain-Source Breakdown Voltage | V _{GS} =0V , I _D =250uA | 60 | | | V |
| I _{DSS} | Zero Gate Voltage Drain Current | V _{DS} =48V , V _{GS} =0V | | | 1 | uA |
| I _{GSS} | Gate-Body Leakage Current | V _{GS} = ±20V , V _{DS} =0V | | | ±100 | nA |
| ON CHARACTERISTICS | | | | | | |
| V _{GS(th)} | Gate Threshold Voltage | V _{DS} =V _{GS} , I _D =250uA | 1 | 1.8 | 3 | V |
| R _{DS(ON)} | Drain-Source On-State Resistance | V _{GS} =10V , I _D =11A | | 15 | 19 | m ohm |
| | | V _{GS} =4.5V , I _D =9A | | 21 | 29 | m ohm |
| g _{FS} | Forward Transconductance | V _{DS} =20V , I _D =11A | | 31 | | S |
| DYNAMIC CHARACTERISTICS [°] | | | | | | |
| C _{ISS} | Input Capacitance | V _{DS} =25V, V _{GS} =0V f=1.0MHz | | 2180 | | pF |
| C _{OSS} | Output Capacitance | | | 196 | | pF |
| C _{RSS} | Reverse Transfer Capacitance | | | 132 | | pF |
| SWITCHING CHARACTERISTICS [°] | | | | | | |
| t _{D(ON)} | Turn-On Delay Time | V _{DD} =30V I _D =1A V _{GS} =10V R _{GEN} = 6 ohm | | 40 | | ns |
| t _r | Rise Time | | | 47 | | ns |
| t _{D(OFF)} | Turn-Off Delay Time | | | 65 | | ns |
| t _f | Fall Time | | | 37 | | ns |
| Q _g | Total Gate Charge | V _{DS} =30V, I _D =11A, V _{GS} =10V | | 34 | | nC |
| | | V _{DS} =30V, I _D =11A, V _{GS} =4.5V | | 17 | | nC |
| Q _{gs} | Gate-Source Charge | V _{DS} =30V, I _D =11A, V _{GS} =10V | | 4 | | nC |
| Q _{gd} | Gate-Drain Charge | | | 9 | | nC |
| DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS | | | | | | |
| V _{SD} | Diode Forward Voltage | V _{GS} =0V, I _S =2A | | 0.76 | 1.3 | V |

Notes

- Surface Mounted on FR4 Board, t ≤ 10sec.
- Pulse Test: Pulse Width ≤ 300us, Duty Cycle ≤ 2%.
- Guaranteed by design, not subject to production testing.
- Starting T_J=25°C, L=0.5mH, V_{DD} = 30V. (See Figure13)

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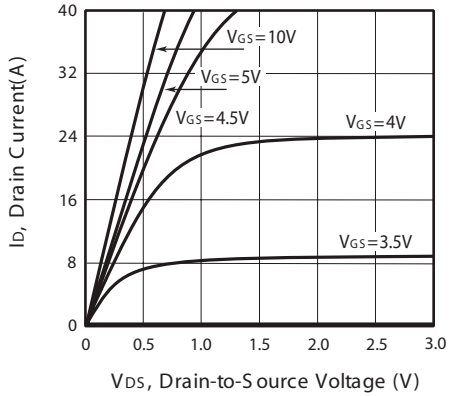


Figure 1. Output Characteristics

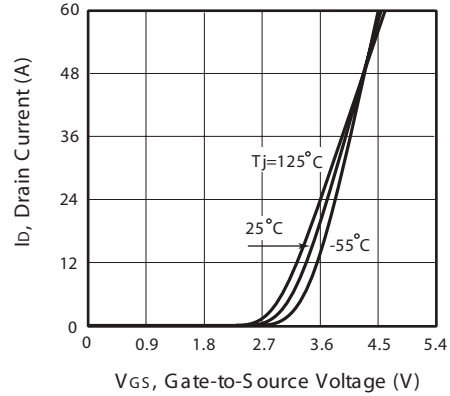


Figure 2. Transfer Characteristics

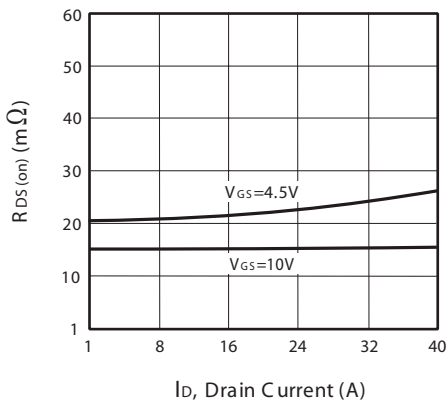


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

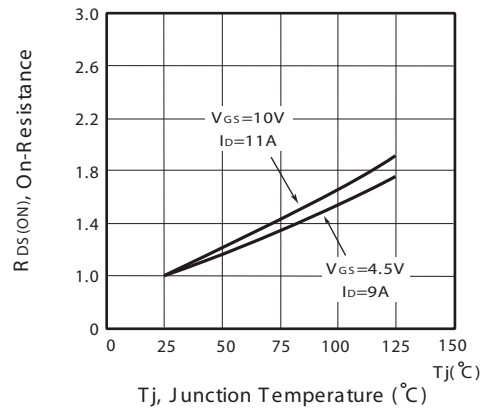


Figure 4. On-Resistance Variation with Drain Current and Temperature

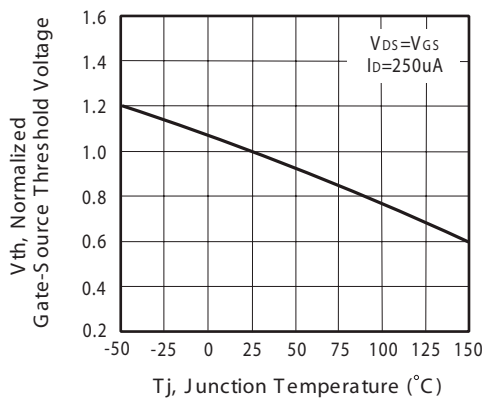


Figure 5. Gate Threshold Variation with Temperature

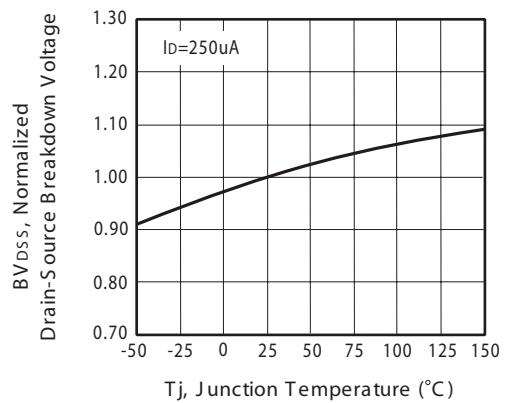


Figure 6. Breakdown Voltage Variation with Temperature

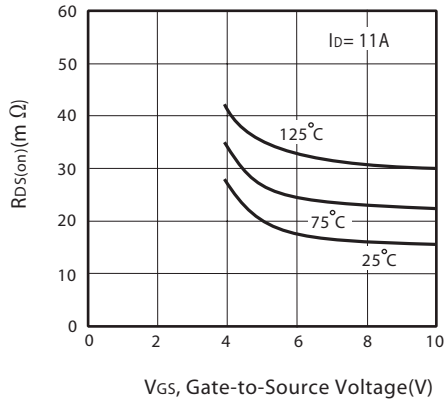


Figure 7. On-Resistance vs. Gate-Source Voltage

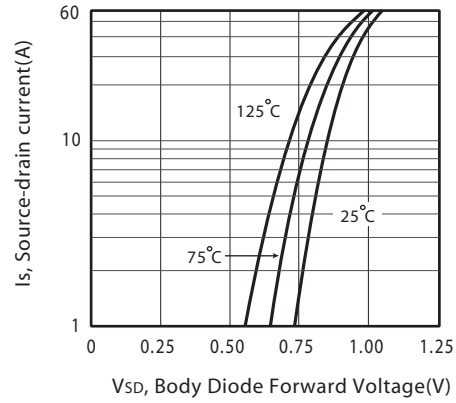


Figure 8. Body Diode Forward Voltage Variation with Source Current

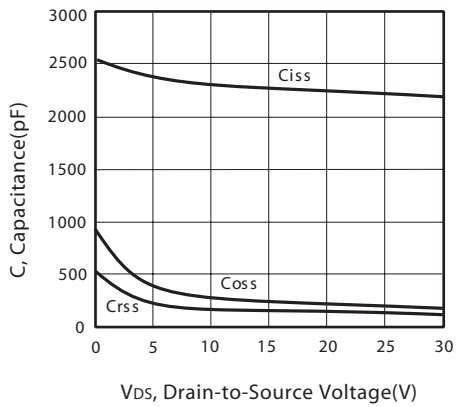


Figure 9. Capacitance

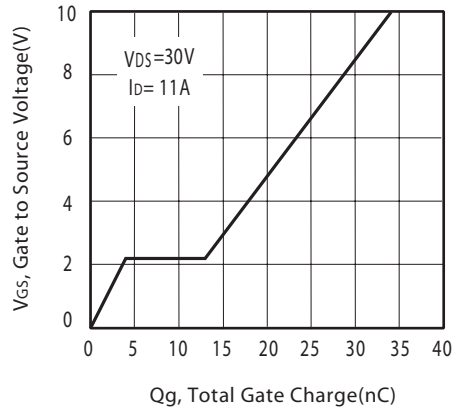


Figure 10. Gate Charge

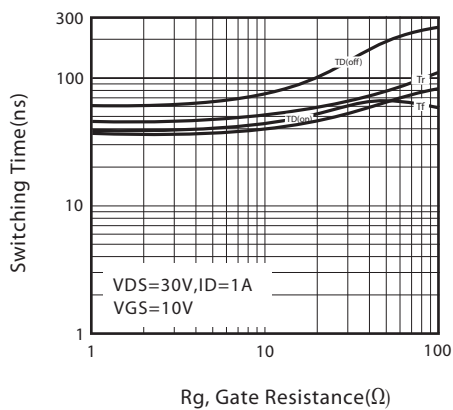


Figure 11. switching characteristics

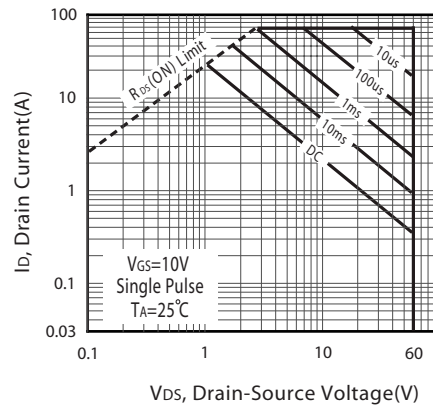
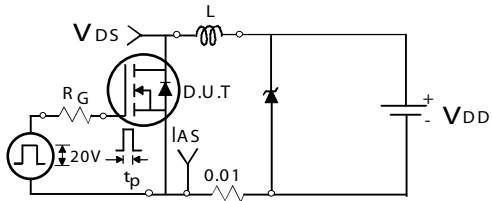
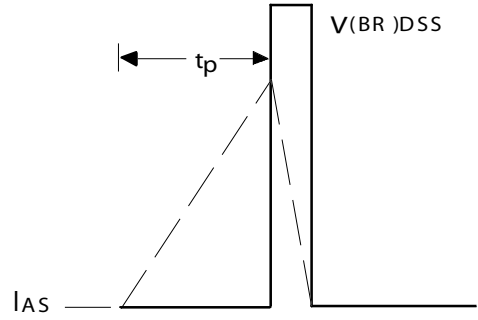


Figure 12. Maximum Safe Operating Area



Unclamped Inductive Test Circuit

Figure 13a.



Unclamped Inductive Waveforms

Figure 13b.

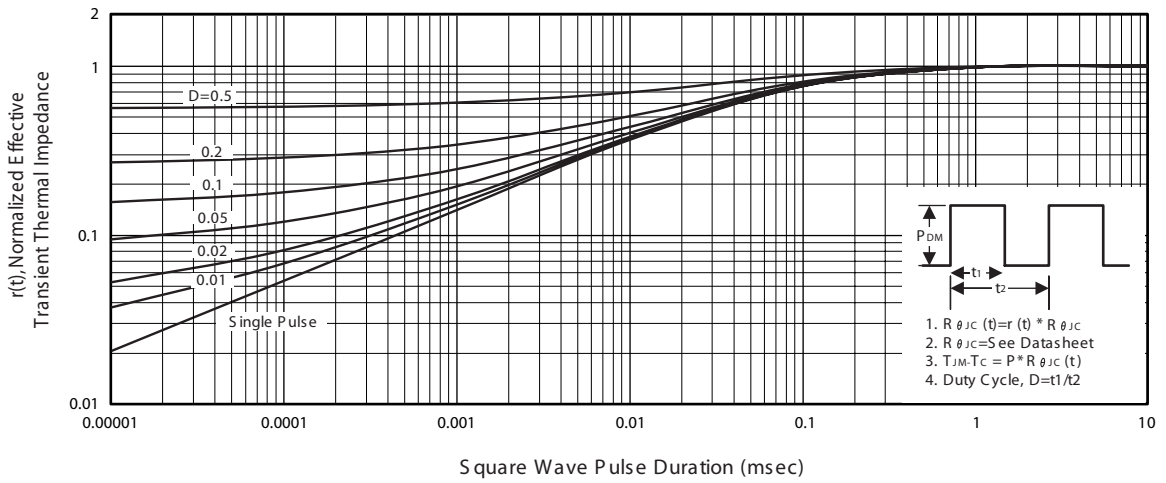
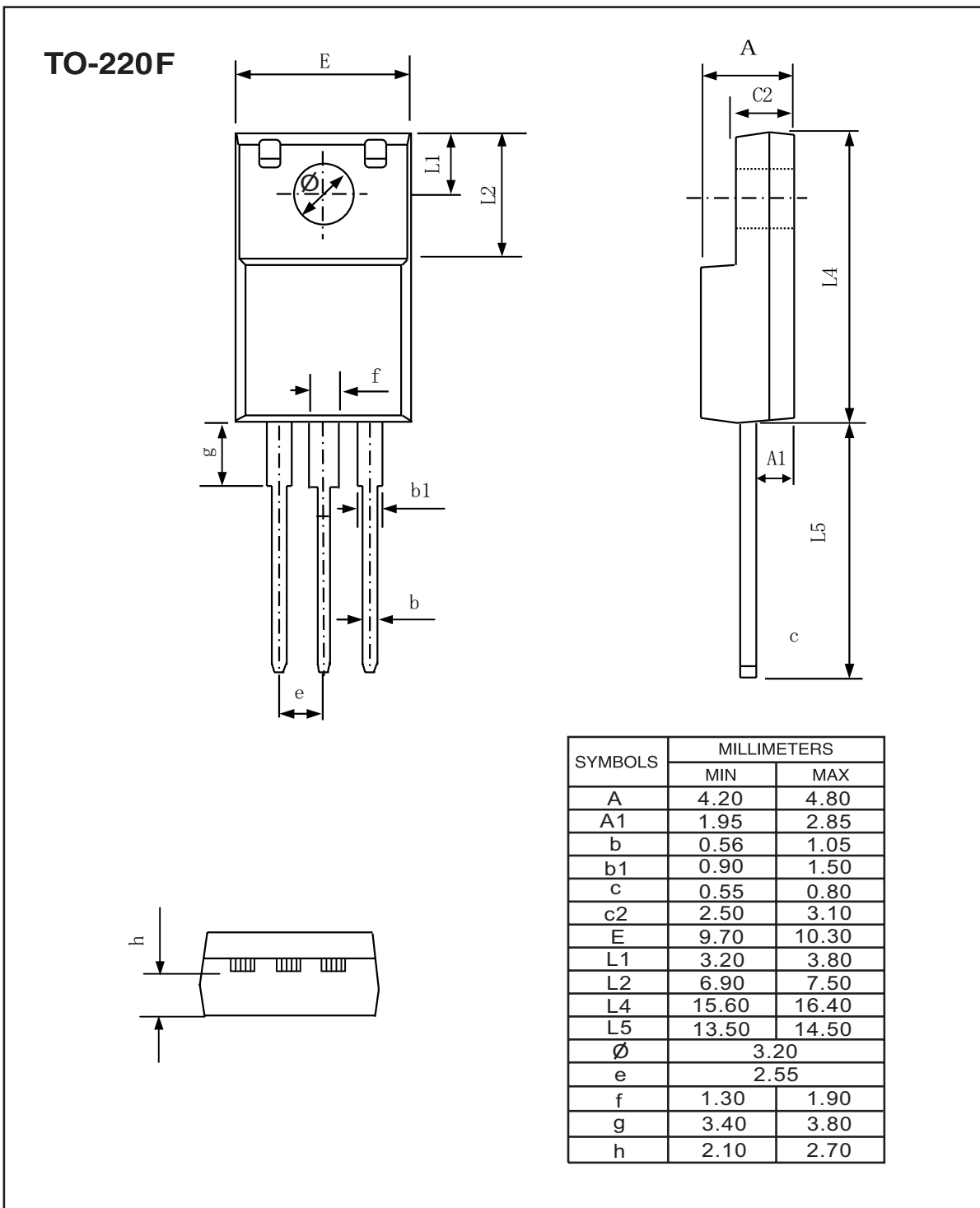


Figure 14. Normalized Thermal Transient Impedance Curve

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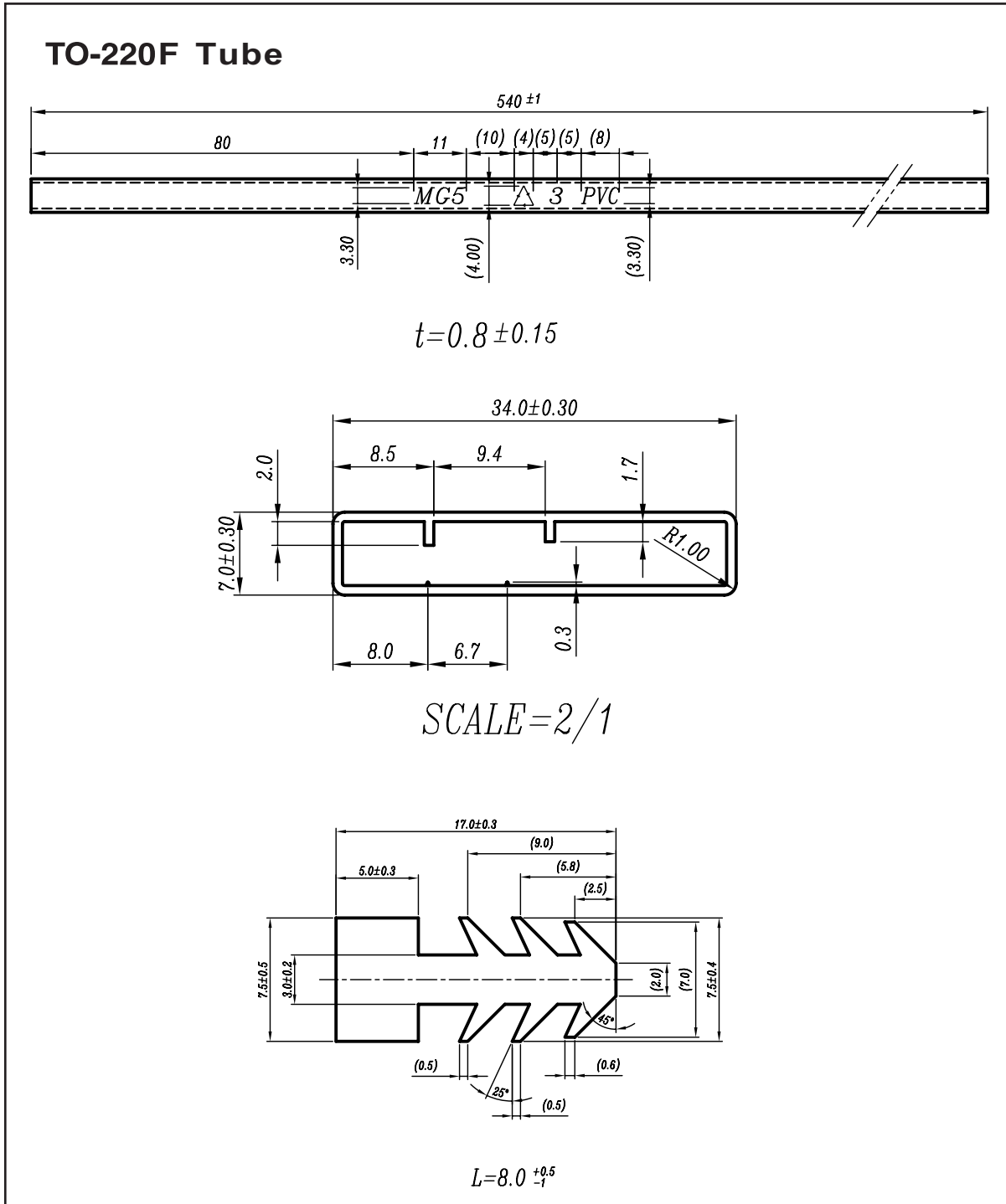
PACKAGE OUTLINE DIMENSIONS



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