



STP6NK70Z STF6NK70Z

N-CHANNEL 700V - 1.5Ω - 5A TO-220/TO-220FP Zener-Protected SuperMESH™ MOSFET

Table 1: General Features

TYPE	V _{DSS}	R _{DS(on)}	I _D	P _w
STP6NK70Z	700 V	< 1.8 Ω	5 A	110 W
STF6NK70Z	700 V	< 1.8 Ω	5 A (*)	30 W

- TYPICAL R_{DS(on)} = 1.5 Ω
- EXTREMELY HIGH dv/dt CAPABILITY
- IMPROVED ESD CAPABILITY
- 100% AVALANCHE RATED
- GATE CHARGE MINIMIZED
- VERY LOW INTRINSIC CAPACITANCES
- VERY GOOD MANUFACTURING REPEATABILITY

DESCRIPTION

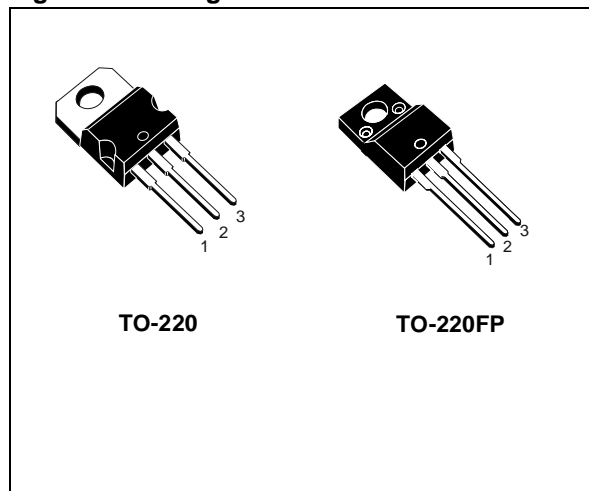
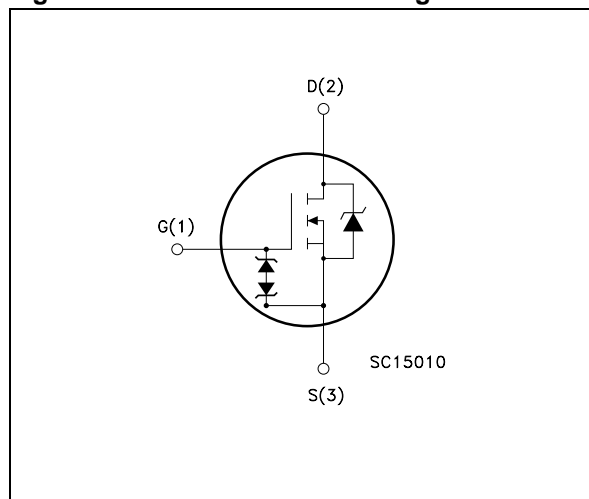
The SuperMESH™ series is obtained through an extreme optimization of ST's well established stripbased PowerMESH™ layout. In addition to pushing on-resistance significantly down, special care is taken to ensure a very good dv/dt capability for the most demanding applications. Such series complements ST full range of high voltage MOSFETs including revolutionary MDmesh™ products.

APPLICATIONS

- HIGH CURRENT, HIGH SPEED SWITCHING
- IDEAL FOR OFF-LINE POWER SUPPLIES, ADAPTORS AND PFC

Table 2: Order Codes

SALES TYPE	MARKING	PACKAGE	PACKAGING
STP6NK70Z	P6NK70Z	TO-220	TUBE
STF6NK70Z	F6NK70Z	TO-220FP	TUBE

Figure 1: Package

Figure 2: Internal Schematic Diagram


STP6NK70Z - STF6NK70Z**Table 3: Absolute Maximum ratings**

Symbol	Parameter	Value		Unit
		STP6NK70Z	STF6NK70Z	
V _{DS}	Drain-source Voltage (V _{GS} = 0)	700		V
V _{DGR}	Drain-gate Voltage (R _{GS} = 20 kΩ)	700		V
V _{GS}	Gate- source Voltage	± 30		V
I _D	Drain Current (continuous) at T _C = 25°C	5	5 (*)	A
I _D	Drain Current (continuous) at T _C = 100°C	3.15	3.15 (*)	A
I _{DM} (●)	Drain Current (pulsed)	20	20 (*)	A
P _{TOT}	Total Dissipation at T _C = 25°C	110	30	W
	Derating Factor	0.87	0.24	W/°C
V _{ESD(G-S)}	Gate source ESD(HBM-C=100pF, R=1.5KΩ)	4000		V
dv/dt (1)	Peak Diode Recovery voltage slope	4.5		V/ns
V _{ISO}	Insulation Withstand Voltage (DC)	-	2500	V
T _j	Operating Junction Temperature	-55 to 150		°C
T _{stg}	Storage Temperature	-55 to 150		°C

(●) Pulse width limited by safe operating area

(1) I_{SD} ≤ 5A, di/dt ≤ 100A/μs, V_{DD} ≤ V_{(BR)DSS}, T_j ≤ T_{JMAX}.

(*) Limited only by maximum temperature allowed

Table 4: Thermal Data

		TO-220	TO-220FP	
R _{thj-case}	Thermal Resistance Junction-case Max	1.14	4.2	°C/W
R _{thj-amb}	Thermal Resistance Junction-ambient Max	62.5		°C/W
T _I	Maximum Lead Temperature For Soldering Purpose	300		°C

Table 5: Avalanche Characteristics

Symbol	Parameter	Max Value	Unit
I _{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T _j max)	5	A
E _{AS}	Single Pulse Avalanche Energy (starting T _j = 25 °C, I _D = I _{AR} , V _{DD} = 50 V)	200	mJ

Table 6: Gate-Source Zener Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
BV _{GSO}	Gate-Source Breakdown Voltage	I _{gs} =± 1mA (Open Drain)	30			V

PROTECTION FEATURES OF GATE-TO-SOURCE ZENER DIODES

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

ELECTRICAL CHARACTERISTICS ($T_{CASE} = 25^{\circ}C$ UNLESS OTHERWISE SPECIFIED)**Table 7: On /Off**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	$I_D = 1 \text{ mA}, V_{GS} = 0$	700			V
I_{DSS}	Zero Gate Voltage Drain Current ($V_{GS} = 0$)	$V_{DS} = \text{Max Rating}$ $V_{DS} = \text{Max Rating}, T_C = 125^{\circ}C$			1 50	μA μA
I_{GSS}	Gate-body Leakage Current ($V_{DS} = 0$)	$V_{GS} = \pm 20 \text{ V}$			± 10	μA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 100 \mu A$	3	3.75	4.5	V
$R_{DS(on)}$	Static Drain-source On Resistance	$V_{GS} = 10 \text{ V}, I_D = 2.5 \text{ A}$		1.5	1.8	Ω

Table 8: Dynamic

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$g_{fs} (1)$	Forward Transconductance	$V_{DS} = 15 \text{ V}, I_D = 2.5 \text{ A}$		4.4		S
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	$V_{DS} = 25 \text{ V}, f = 1 \text{ MHz}, V_{GS} = 0$		930 105 22		pF pF pF
$C_{OSS \text{ eq}} (3)$	Equivalent Output Capacitance	$V_{GS} = 0 \text{ V}, V_{DS} = 0 \text{ to } 560 \text{ V}$		70		pF
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on Delay Time Rise Time Turn-off-Delay Time Fall Time	$V_{DD} = 350 \text{ V}, I_D = 2.5 \text{ A},$ $R_G = 4.7 \Omega, V_{GS} = 10 \text{ V}$ (see Figure 17)		17 18 45 30		ns ns ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	$V_{DD} = 560 \text{ V}, I_D = 5 \text{ A},$ $V_{GS} = 10 \text{ V}$ (see Figure 20)		34 6.5 17	47	nC nC nC

Table 9: Source Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} $I_{SDM} (2)$	Source-drain Current Source-drain Current (pulsed)				5 20	A A
$V_{SD} (1)$	Forward On Voltage	$I_{SD} = 5 \text{ A}, V_{GS} = 0$			1.6	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 5 \text{ A}, di/dt = 100 \text{ A}/\mu s$ $V_{DD} = 35 \text{ V}$ (see Figure 18)		432 2.37 11		ns μC A
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 5 \text{ A}, di/dt = 100 \text{ A}/\mu s$ $V_{DD} = 35 \text{ V}, T_j = 150^{\circ}C$ (see Figure 18)		588 3.38 11.5		ns μC A

(1) Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %.

(2) Pulse width limited by safe operating area.

(3) $C_{OSS \text{ eq}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{OSS} when V_{DS} increases from 0 to 80% V_{DSS} .

Figure 3: Safe Operating Area

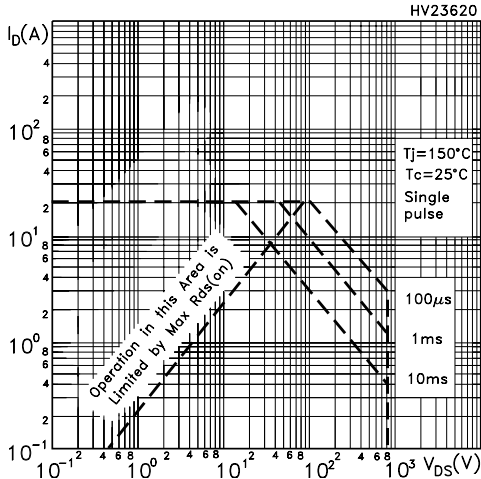


Figure 4: Safe Operating Area for TO-220FP

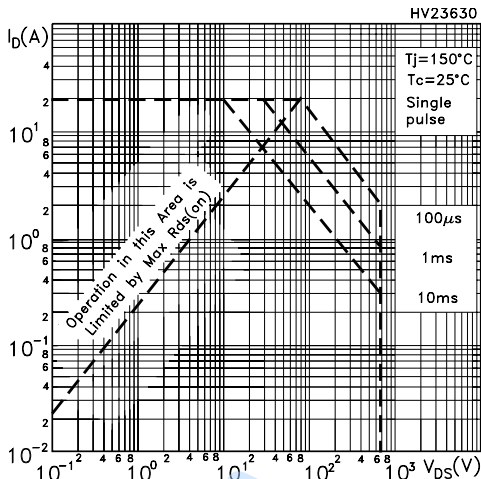


Figure 5: Output Characteristics

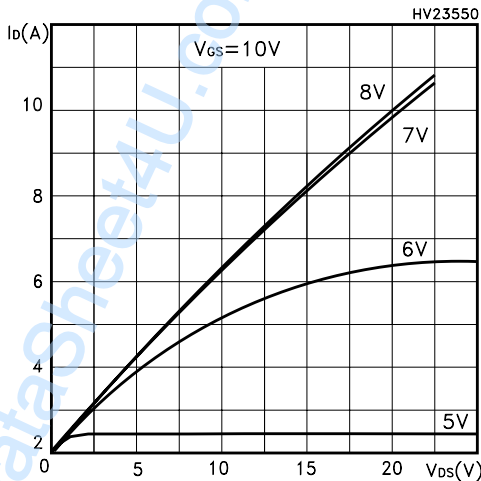


Figure 6: Thermal Impedance

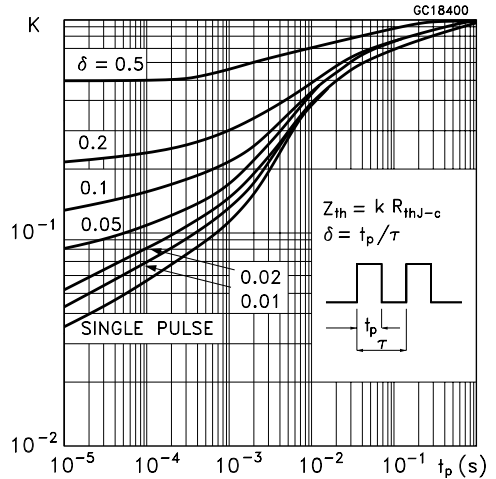


Figure 7: Thermal Impedance for TO-220FP

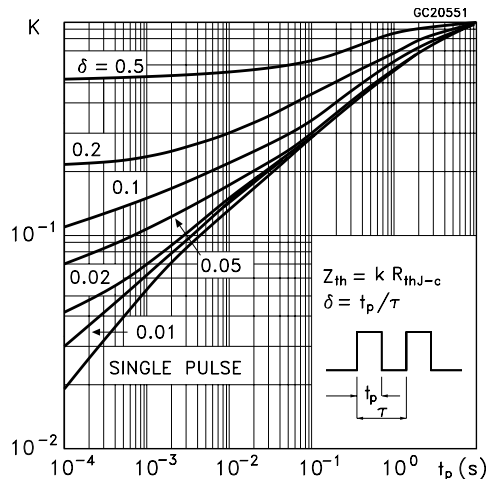


Figure 8: Transfer Characteristics

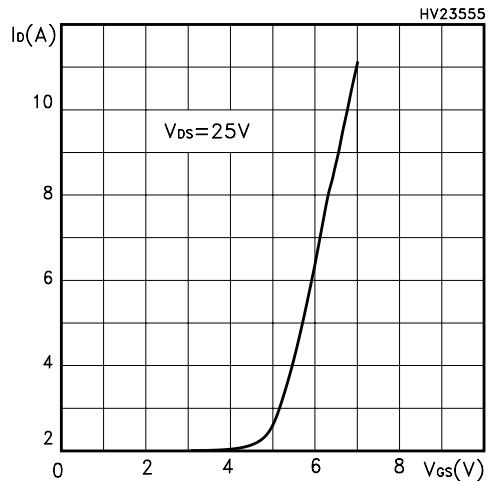


Figure 9: Transconductance

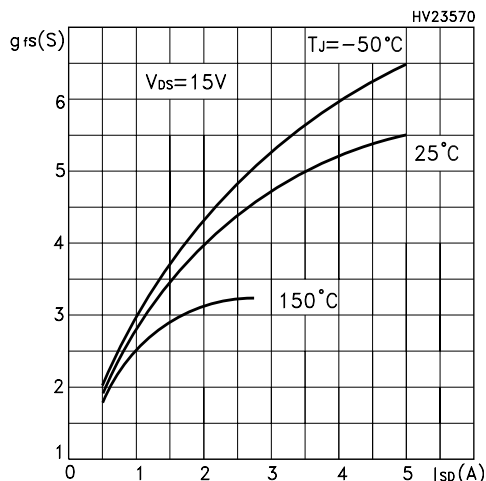


Figure 10: Gate Charge vs Gate-source Voltage

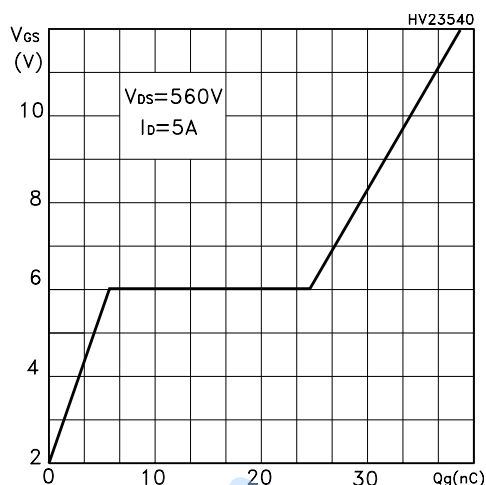


Figure 11: Source-Drain Diode Forward Characteristics

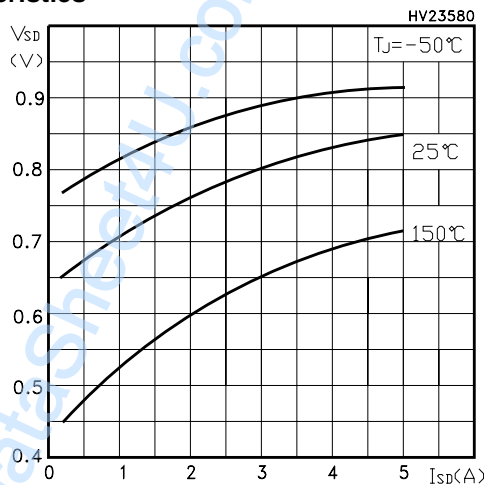


Figure 12: Static Drain-source On Resistance

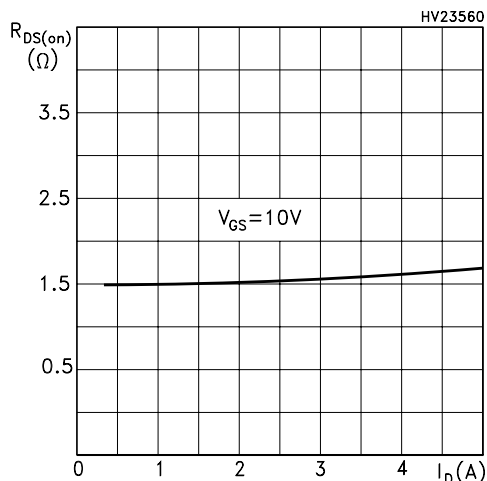


Figure 13: Capacitance Variations

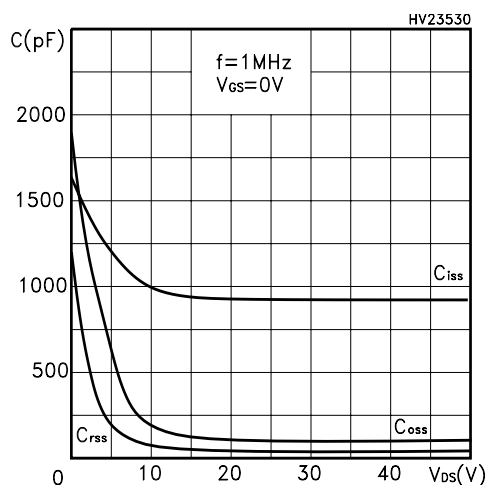


Figure 14: Normalized BV_DS vs Temperature

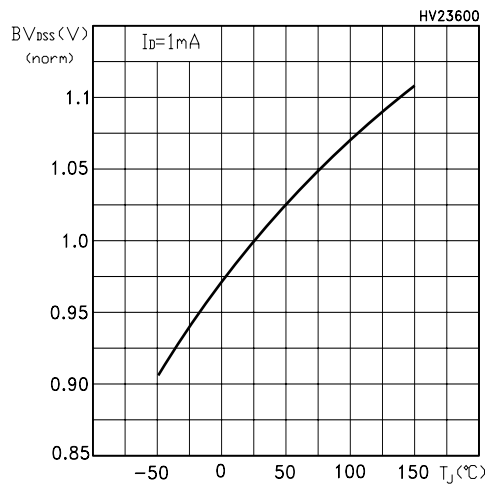


Figure 15: Avalanche Energy vs Starting Tj

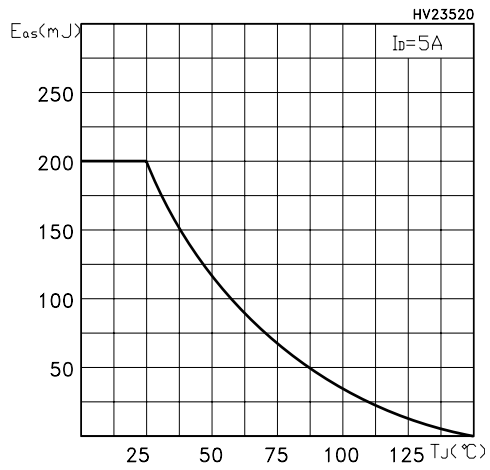


Figure 16: Unclamped Inductive Load Test Circuit

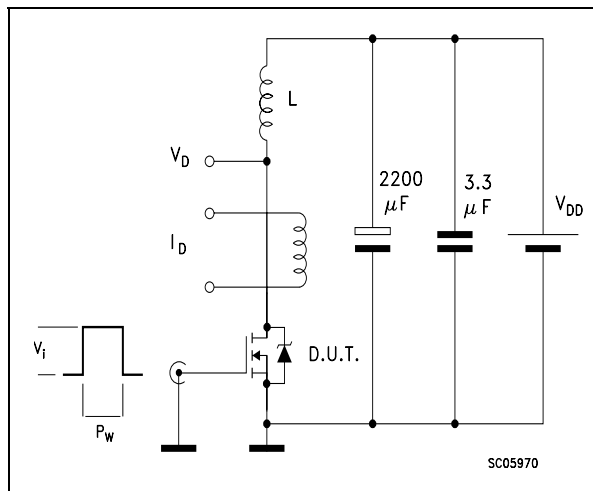


Figure 17: Switching Times Test Circuit For Resistive Load

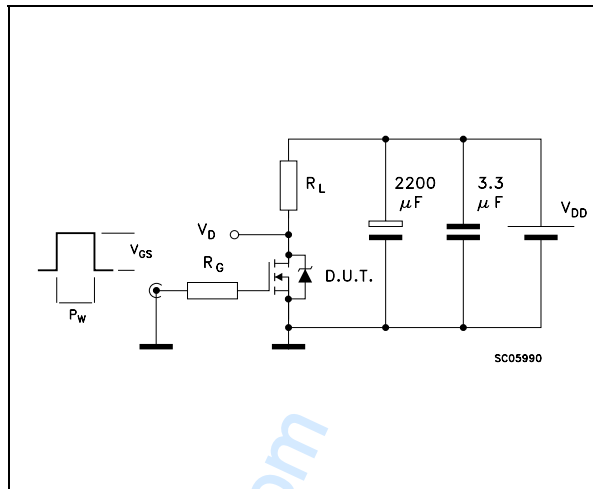


Figure 18: Test Circuit For Inductive Load Switching and Diode Recovery Times

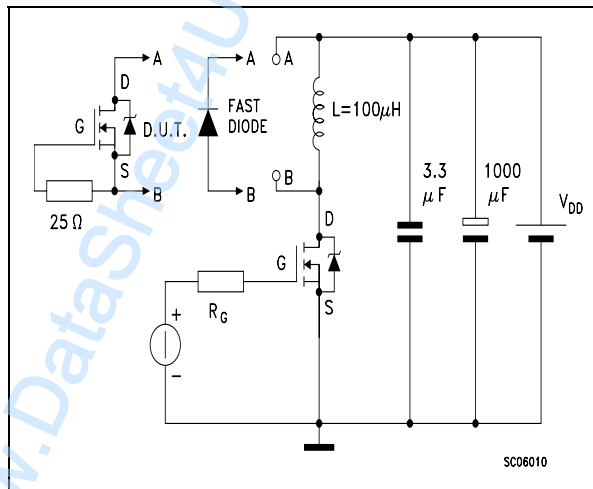


Figure 19: Unclamped Inductive Waferform

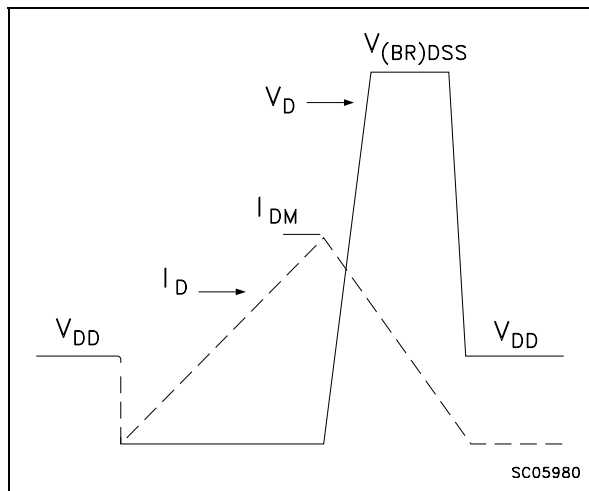
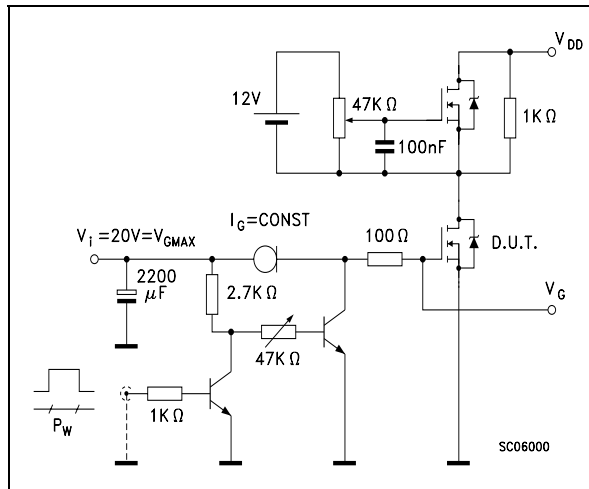


Figure 20: Gate Charge Test Circuit

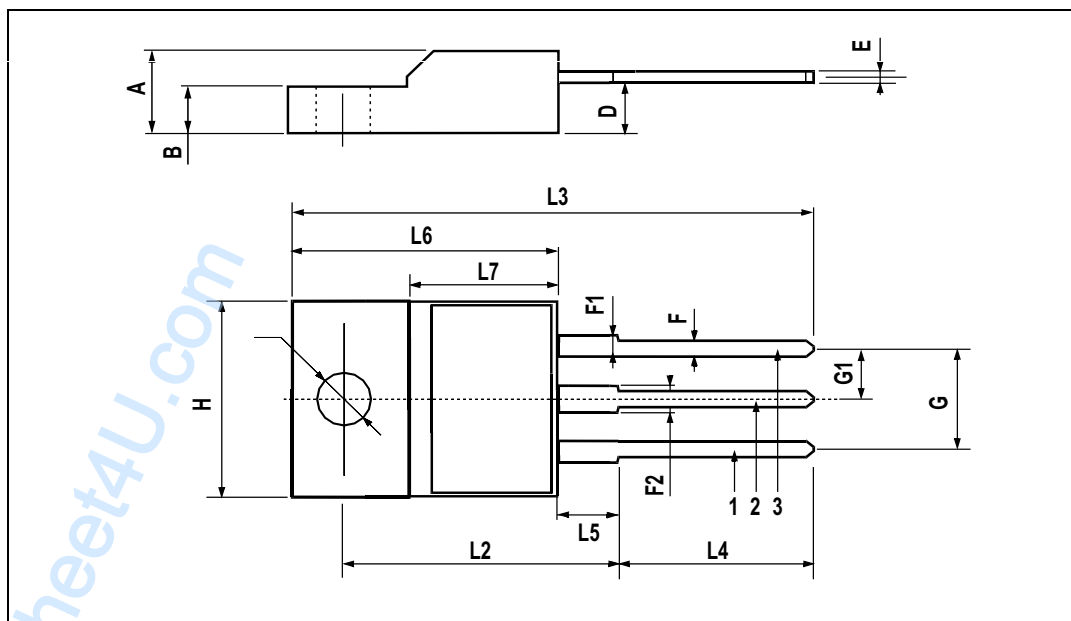


STP6NK70Z - STF6NK70Z

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

TO-220FP MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
B	2.5		2.7	0.098		0.106
D	2.5		2.75	0.098		0.108
E	0.45		0.7	0.017		0.027
F	0.75		1	0.030		0.039
F1	1.15		1.7	0.045		0.067
F2	1.15		1.7	0.045		0.067
G	4.95		5.2	0.195		0.204
G1	2.4		2.7	0.094		0.106
H	10		10.4	0.393		0.409
L2		16			0.630	
L3	28.6		30.6	1.126		1.204
L4	9.8		10.6	.0385		0.417
L5	2.9		3.6	0.114		0.141
L6	15.9		16.4	0.626		0.645
L7	9		9.3	0.354		0.366
∅	3		3.2	0.118		0.126



TO-220 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.15		1.70	0.045		0.066
c	0.49		0.70	0.019		0.027
D	15.25		15.75	0.60		0.620
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.052
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
øP	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116

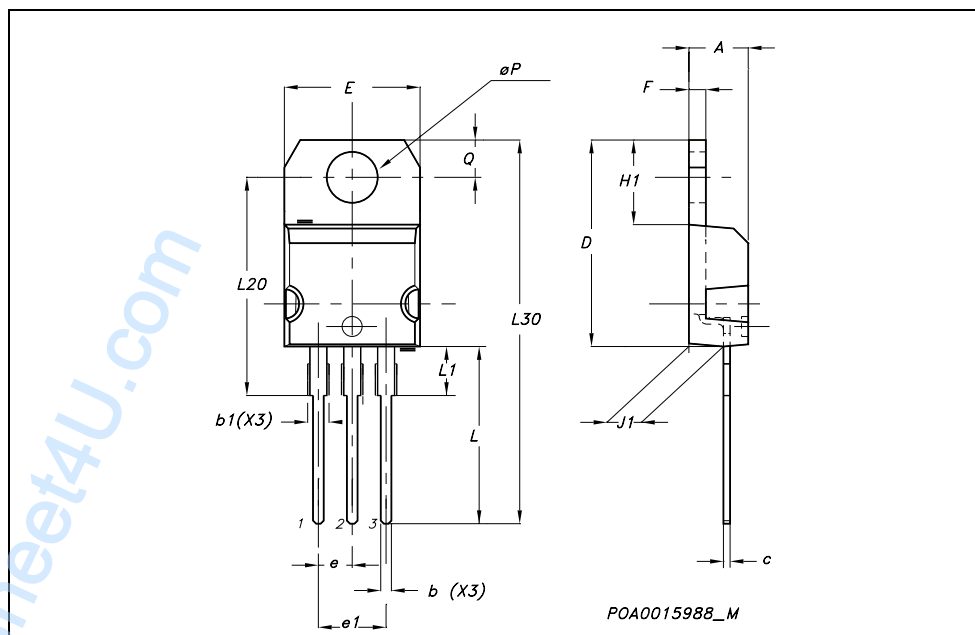


Table 10: Revision History

Date	Revision	Description of Changes
24-Sep-2004	1	First release.
04-Nov-2004	2	Complete version
06-Sep-2005	3	Inserted Ecopack indication

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