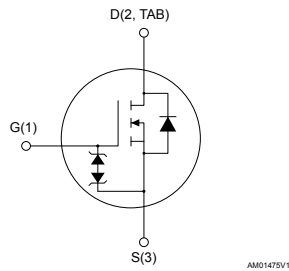
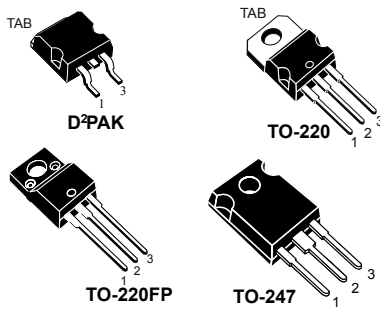


## N-channel 900 V, 1.56 $\Omega$ typ., 5.8 A SuperMESH™ Power MOSFET in D<sup>2</sup>PAK, TO-220, TO-220FP and TO-247 packages



### Features

Order codes	V <sub>DS</sub>	R <sub>DS(on)</sub> max.	I <sub>D</sub>
STB6NK90ZT4	900 V	2 $\Omega$	5.8 A
STP6NK90Z			
STP6NK90ZFP			
STW7NK90Z			

- Extremely high dv/dt capability
- 100% avalanche tested
- Gate charge minimized
- Zener-protected

### Applications

- Switching applications

### Description

These high-voltage devices are Zener-protected N-channel Power MOSFETs developed using the SuperMESH™ technology by STMicroelectronics, an optimization of the well-established PowerMESH™. In addition to a significant reduction in on-resistance, these devices are designed to ensure a high level of dv/dt capability for the most demanding applications.

Product status
STB6NK90ZT4
STP6NK90Z
STP6NK90ZFP
STW7NK90Z

# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value		Unit
		D <sup>2</sup> PAK, TO-220, TO-247	TO-220FP	
V <sub>DS</sub>	Drain-source voltage	900		V
V <sub>GS</sub>	Gate-source voltage	± 30		V
I <sub>D</sub>	Drain current (continuous) at T <sub>C</sub> = 25 °C	5.8	5.8 <sup>(1)</sup>	A
I <sub>D</sub>	Drain current (continuous) at T <sub>C</sub> = 100 °C	3.65	3.65 <sup>(1)</sup>	A
I <sub>DM</sub> <sup>(2)</sup>	Drain current (pulsed)	23.2	23.2	A
P <sub>TOT</sub>	Total dissipation at T <sub>C</sub> = 25 °C	140	30	W
dv/dt <sup>(3)</sup>	Peak diode recovery voltage slope	4.5		V/ns
V <sub>ISO</sub>	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1 s; T <sub>C</sub> = 25 °C)	-	2500	V
T <sub>J</sub>	Operating junction temperature range	-55 to 150		°C
T <sub>stg</sub>	Storage temperature range			°C

1. Limited by maximum junction temperature.
2. Pulse width limited by safe operating area.
3.  $I_{SD} \leq 5.8 \text{ A}$ ,  $di/dt \leq 200 \text{ A}/\mu\text{s}$ ,  $V_{DD} \leq V_{(BR)DSS}$ .

**Table 2. Thermal data**

Symbol	Parameter	Value				Unit
		D <sup>2</sup> PAK	TO-220	TO-220FP	TO-247	
R <sub>thj-case</sub>	Thermal resistance junction-case	0.89		4.2	0.89	°C/W
R <sub>thj-pcb</sub>	Thermal resistance junction-pcb	60				°C/W
R <sub>thj-amb</sub>	Thermal resistance junction-ambient	62.5			50	°C/W

**Table 3. Avalanche characteristics**

Symbol	Parameter	Value	Unit
I <sub>AR</sub>	Avalanche current, repetitive or not-repetitive (pulse width limited by T <sub>J</sub> Max)	5.8	A
E <sub>AS</sub>	Single pulse avalanche energy (starting T <sub>J</sub> = 25 °C, I <sub>D</sub> = I <sub>AR</sub> , V <sub>DD</sub> = 50 V)	300	mJ

## 2 Electrical characteristics

( $T_{CASE} = 25\text{ °C}$  unless otherwise specified)

**Table 4. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source	$I_D = 1\text{ mA}, V_{GS} = 0\text{ V}$	900			V
	Breakdown voltage					
$I_{DSS}$	Zero gate voltage drain current	$V_{GS} = 0\text{ V}, V_{DS} = 900\text{ V}$			1	$\mu\text{A}$
		$V_{GS} = 0\text{ V}, V_{DS} = 900\text{ V}, T_C = 125\text{ °C}^{(1)}$			50	$\mu\text{A}$
$I_{GSS}$	Gate body leakage current	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			$\pm 10$	$\mu\text{A}$
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 100\text{ }\mu\text{A}$	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{ V}, I_D = 2.9\text{ A}$		1.56	2	$\Omega$

1. Defined by design, not subject to production test.

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 25\text{ V}, f = 1\text{ MHz}, V_{GS} = 0\text{ V}$		1350		$\mu\text{F}$
$C_{oss}$	Output capacitance			130		
$C_{rss}$	Reverse transfer capacitance			26		
$C_{oss\text{ eq.}}^{(1)}$	Equivalent output capacitance	$V_{GS} = 0\text{ V}, V_{DS} = 0\text{ V to } 720\text{ V}$		70		$\mu\text{F}$
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 450\text{ V}, I_D = 3\text{ A}, R_G = 4.7\text{ }\Omega,$ $V_{GS} = 10\text{ V}$ (see Figure 17. Test circuit for resistive load switching times and Figure 22. Switching time waveform)		17		ns
$t_r$	Rise time			20		
$t_{r(off)}$	Turn-off delay time			45		
$t_f$	Fall time			20		
$Q_g$	Total gate charge	$V_{DD} = 720\text{ V}, I_D = 5.8\text{ A}, V_{GS} = 0\text{ to } 10\text{ V}$ (see Figure 18. Test circuit for gate charge behavior)		46.5	60.5	nC
$Q_{gs}$	Gate-source charge			8.5		
$Q_{gd}$	Gate-drain charge			25		
$t_{r(voff)}$	Off-voltage rise time	$V_{DD} = 720\text{ V}, I_D = 5.8\text{ A}, R_G = 4.7\text{ }\Omega,$ $V_{GS} = 10\text{ V}$ (see Figure 19. Test circuit for inductive load switching and diode recovery times)		11		ns
$t_f$	Fall time			12		
$t_c$	Cross-over time			20		

1.  $C_{oss\text{ eq.}}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$ .

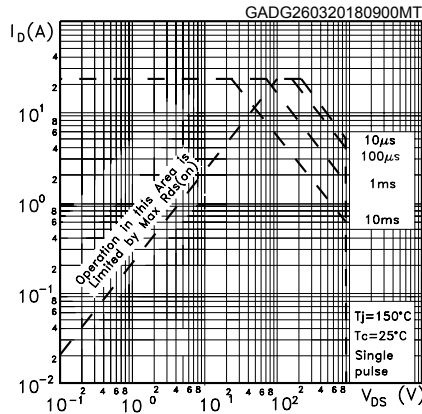
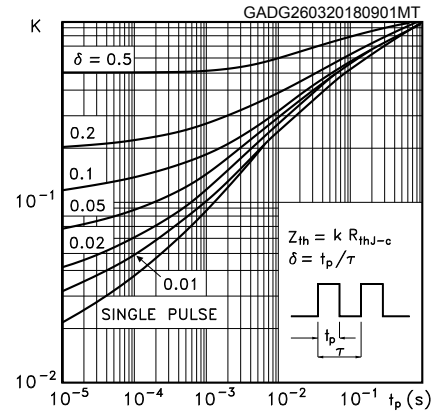
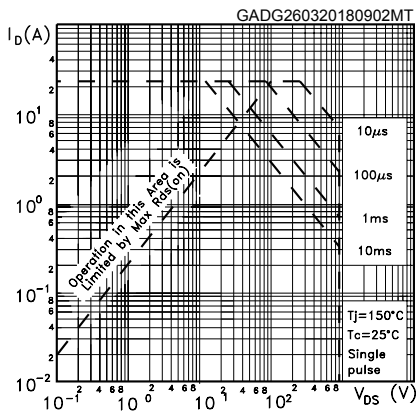
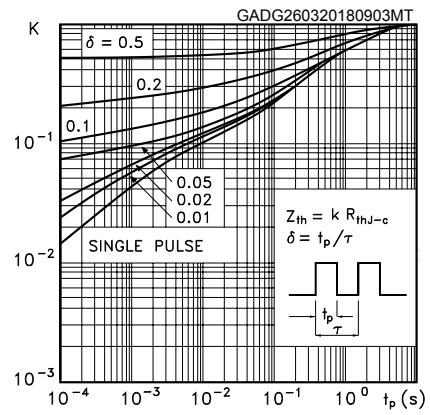
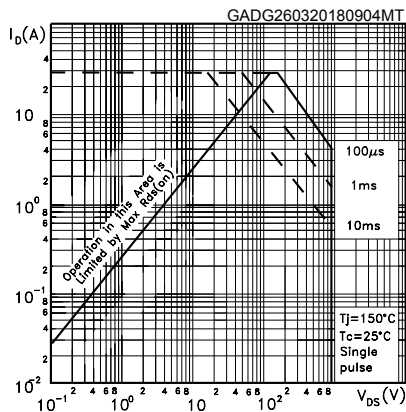
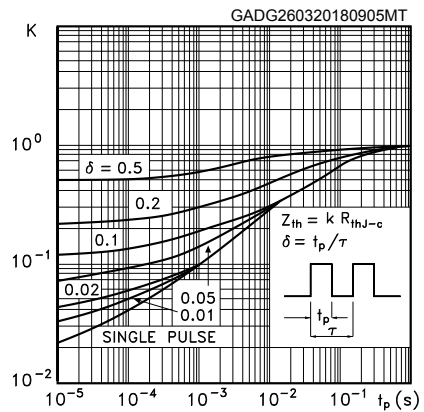
**Table 6. Source drain diode**

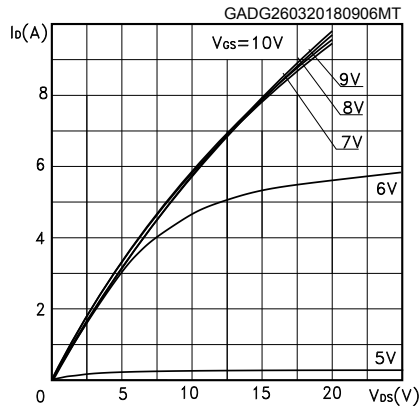
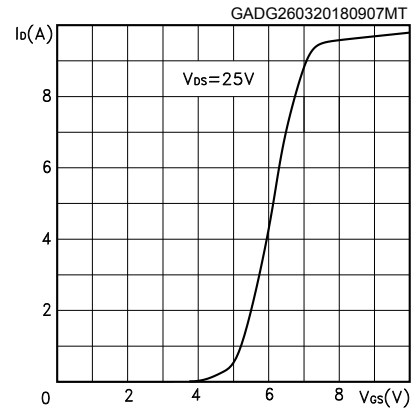
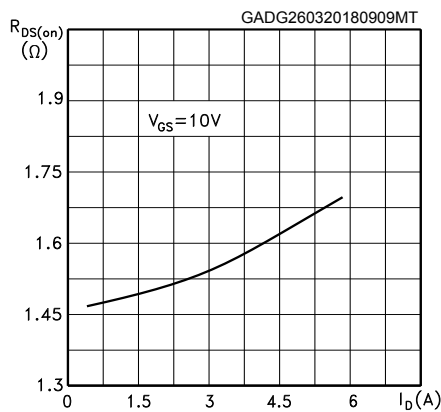
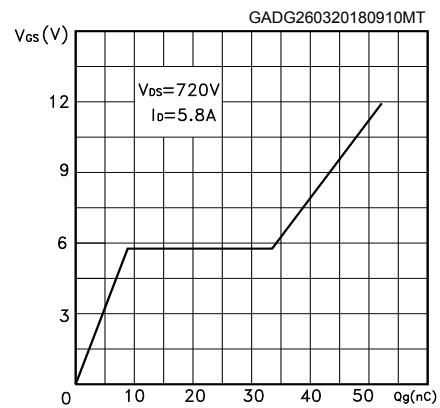
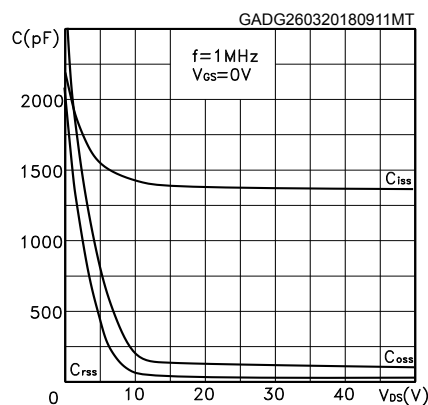
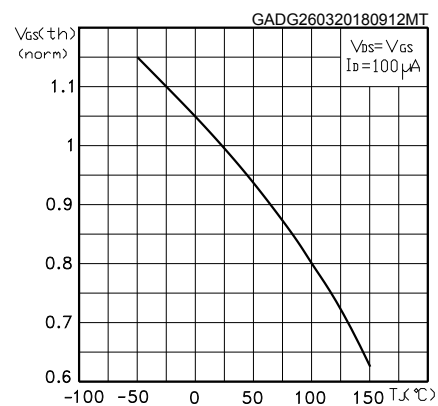
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current				5.8	A
$I_{SDM}$	Source-drain current (pulsed)				23.2	
$V_{SD}$	Forward on voltage	$I_{SD} = 5.8 \text{ A}, V_{GS} = 0 \text{ V}$			1.6	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 5.8 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s}$		840		ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 36 \text{ V}, T_j = 150 \text{ }^\circ\text{C}$ (see <a href="#">Figure 19. Test circuit for inductive load switching and diode recovery times</a> )		5880		nC
$I_{RRM}$	Reverse recovery current			14		A

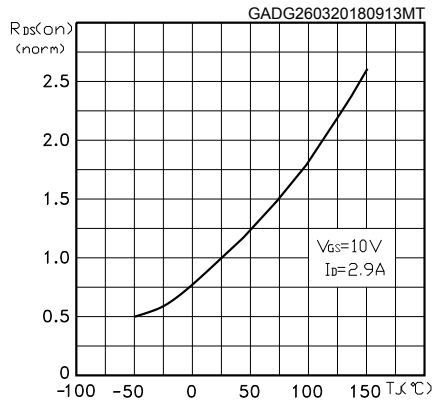
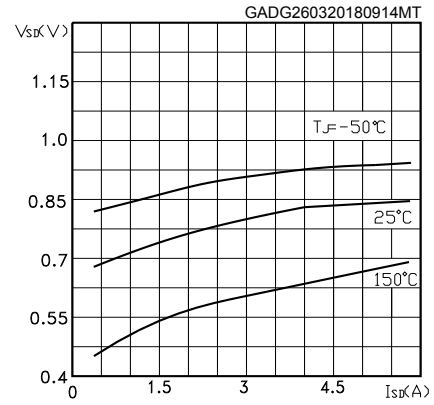
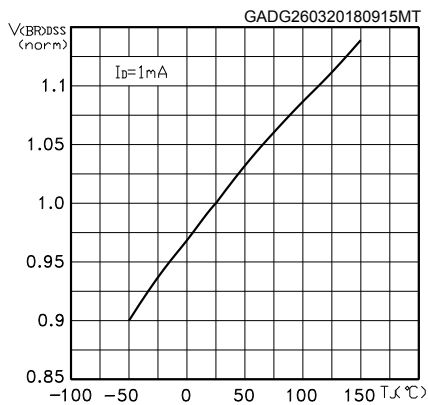
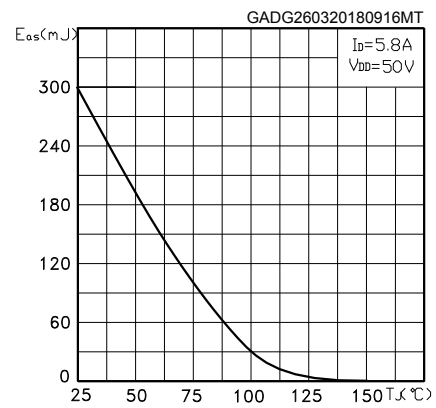
**Table 7. Gate-source zener diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	$I_{GS} = \pm 1 \text{ mA}, I_D = 0 \text{ A}$	$\pm 30$			V

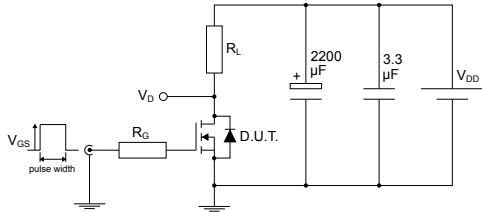
The built-in back-to-back Zener diodes are specifically designed to enhance the ESD performance of the device. The Zener voltage facilitates efficient and cost-effective device integrity protection, thus eliminating the need for additional external componentry.

**2.1 Electrical characteristics curves**
**Figure 1. Safe operating area for TO-220/D<sup>2</sup>PAK**

**Figure 2. Thermal impedance for TO-220/D<sup>2</sup>PAK**

**Figure 3. Safe operating area for TO-220FP**

**Figure 4. Thermal impedance for TO-220FP**

**Figure 5. Safe operating area for TO-247**

**Figure 6. Thermal impedance for TO-247**


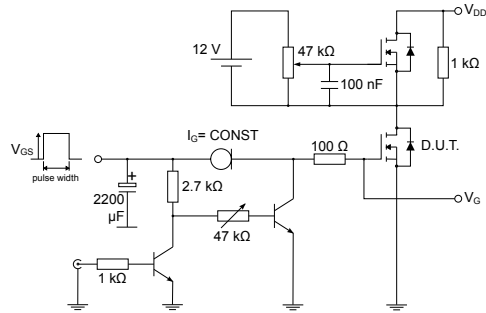
**Figure 7. Output characteristics**

**Figure 8. Transfer characteristics**

**Figure 9. Static drain-source on resistance**

**Figure 10. Gate charge vs gate-source voltage**

**Figure 11. Capacitance variations**

**Figure 12. Normalized gate threshold voltage vs temperature**


**Figure 13. Normalized on resistance vs temperature**

**Figure 14. Source-drain diode forward characteristic**

**Figure 15. Normalized  $V_{(BR)DSS}$  vs temperature**

**Figure 16. Maximum avalanche energy vs temperature**


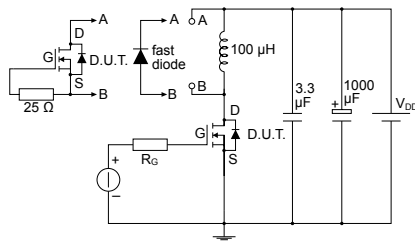
### 3 Test circuits

**Figure 17. Test circuit for resistive load switching times**


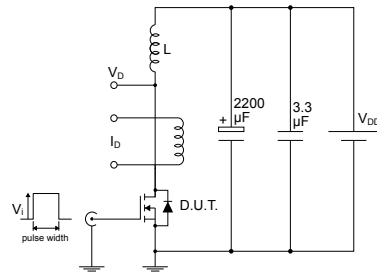
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**Figure 18. Test circuit for gate charge behavior**


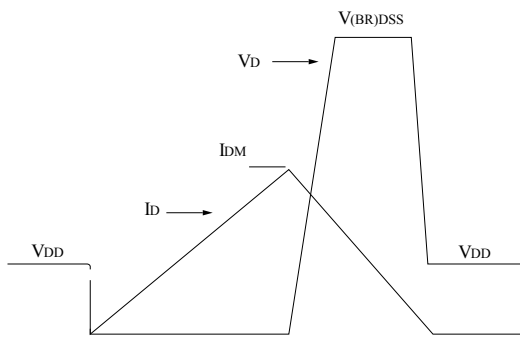
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**Figure 19. Test circuit for inductive load switching and diode recovery times**


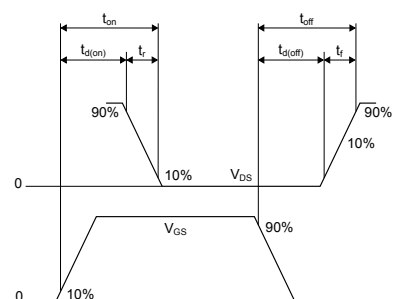
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**Figure 20. Unclamped inductive load test circuit**


AM01471v1

**Figure 21. Unclamped inductive waveform**


AM01472v1

**Figure 22. Switching time waveform**


AM01473v1



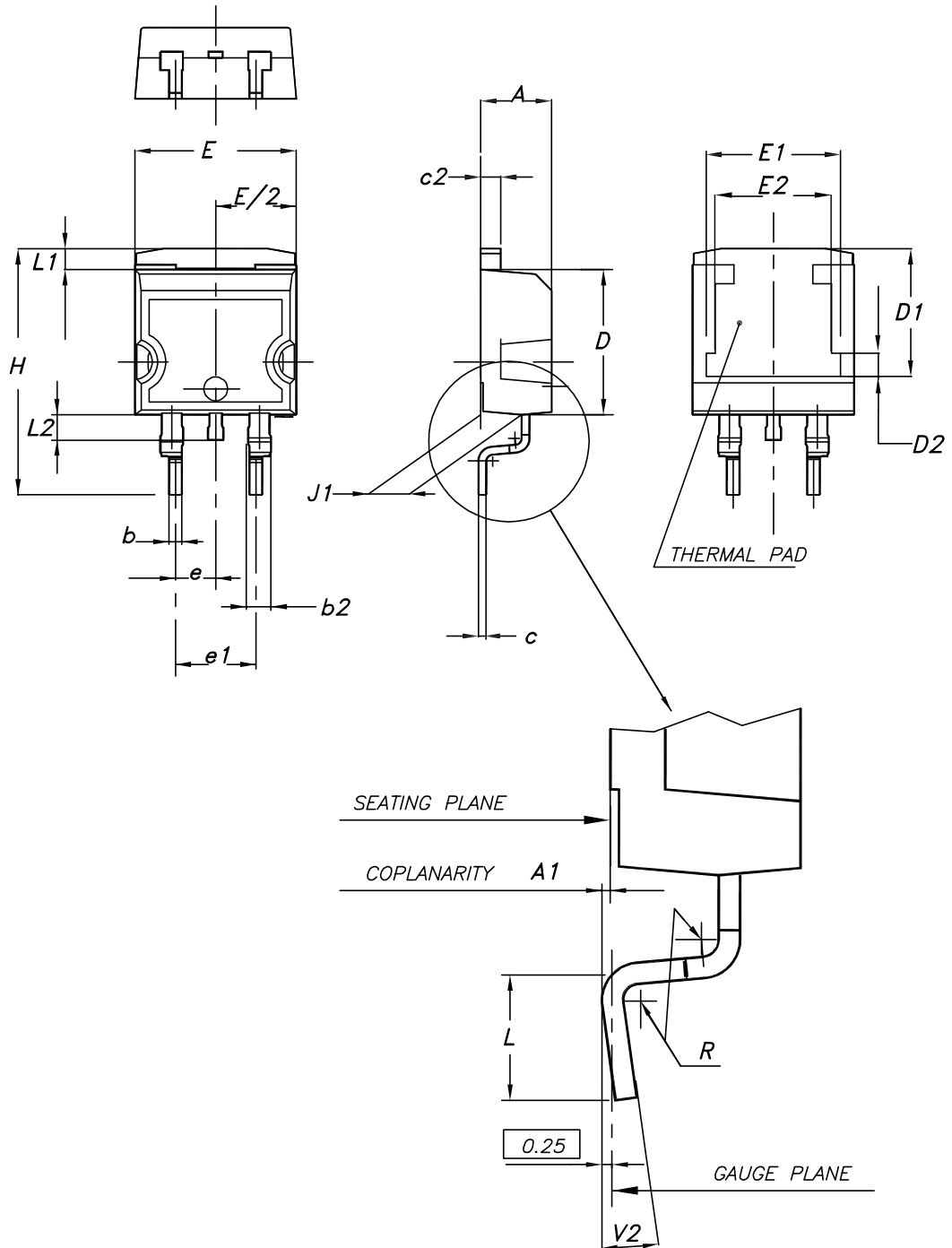
## 4 Package information

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In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

### 4.1 D<sup>2</sup>PAK (TO-263) package information

Figure 23. D<sup>2</sup>PAK (TO-263) type A package outline

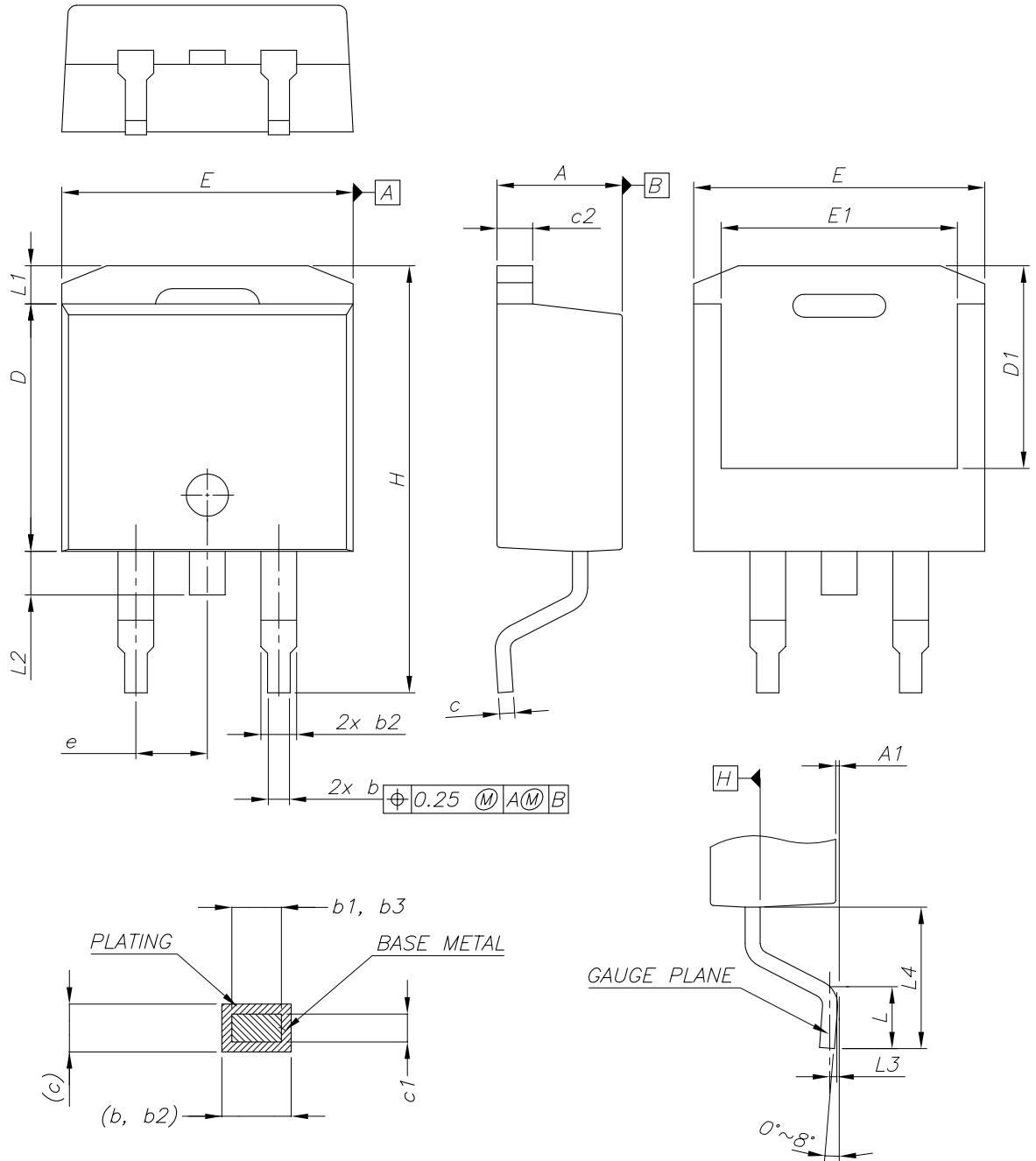


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**Table 8. D<sup>2</sup>PAK (TO-263) type A package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50	7.75	8.00
D2	1.10	1.30	1.50
E	10.00		10.40
E1	8.50	8.70	8.90
E2	6.85	7.05	7.25
e		2.54	
e1	4.88		5.28
H	15.00		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.40	
V2	0°		8°

Figure 24. D<sup>2</sup>PAK (TO-263) type B package outline

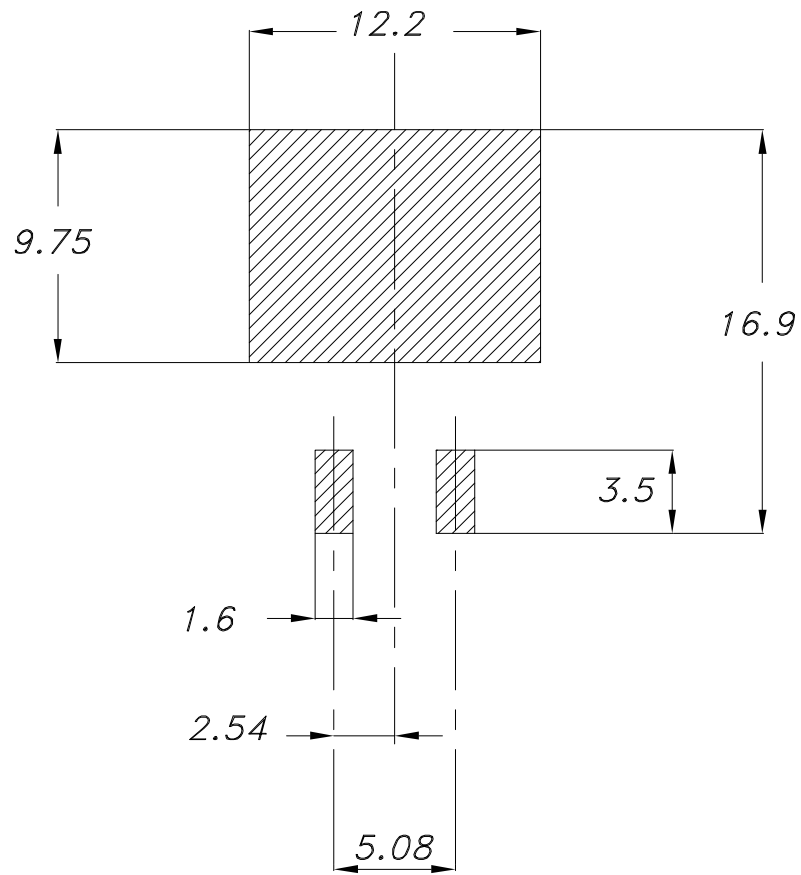


0079457\_24\_B

**Table 9. D<sup>2</sup>PAK (TO-263) type B mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.36		4.56
A1	0		0.25
b	0.70		0.90
b1	0.51		0.89
b2	1.17		1.37
b3	1.36		1.46
c	0.38		0.694
c1	0.38		0.534
c2	1.19		1.34
D	8.60		9.00
D1	6.90		7.50
E	10.15		10.55
E1	8.10		8.70
e	2.54 BSC		
H	15.00		15.60
L	1.90		2.50
L1			1.65
L2			1.78
L3		0.25	
L4	4.78		5.28

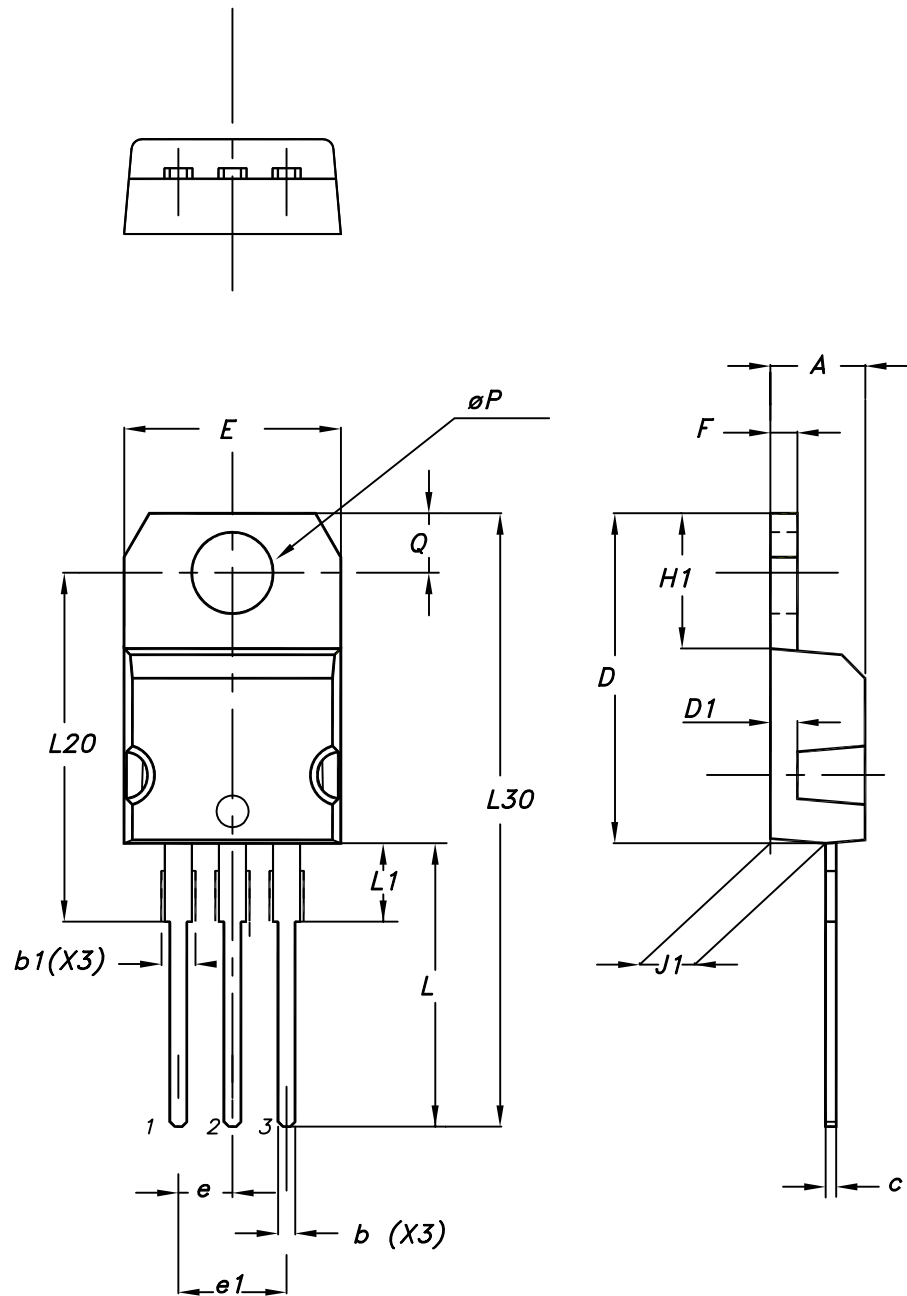
Figure 25. D<sup>2</sup>PAK (TO-263) recommended footprint (dimensions are in mm)



Footprint

## 4.2 TO-220 type A package information

Figure 26. TO-220 type A package outline



0015988\_typeA\_Rev\_21

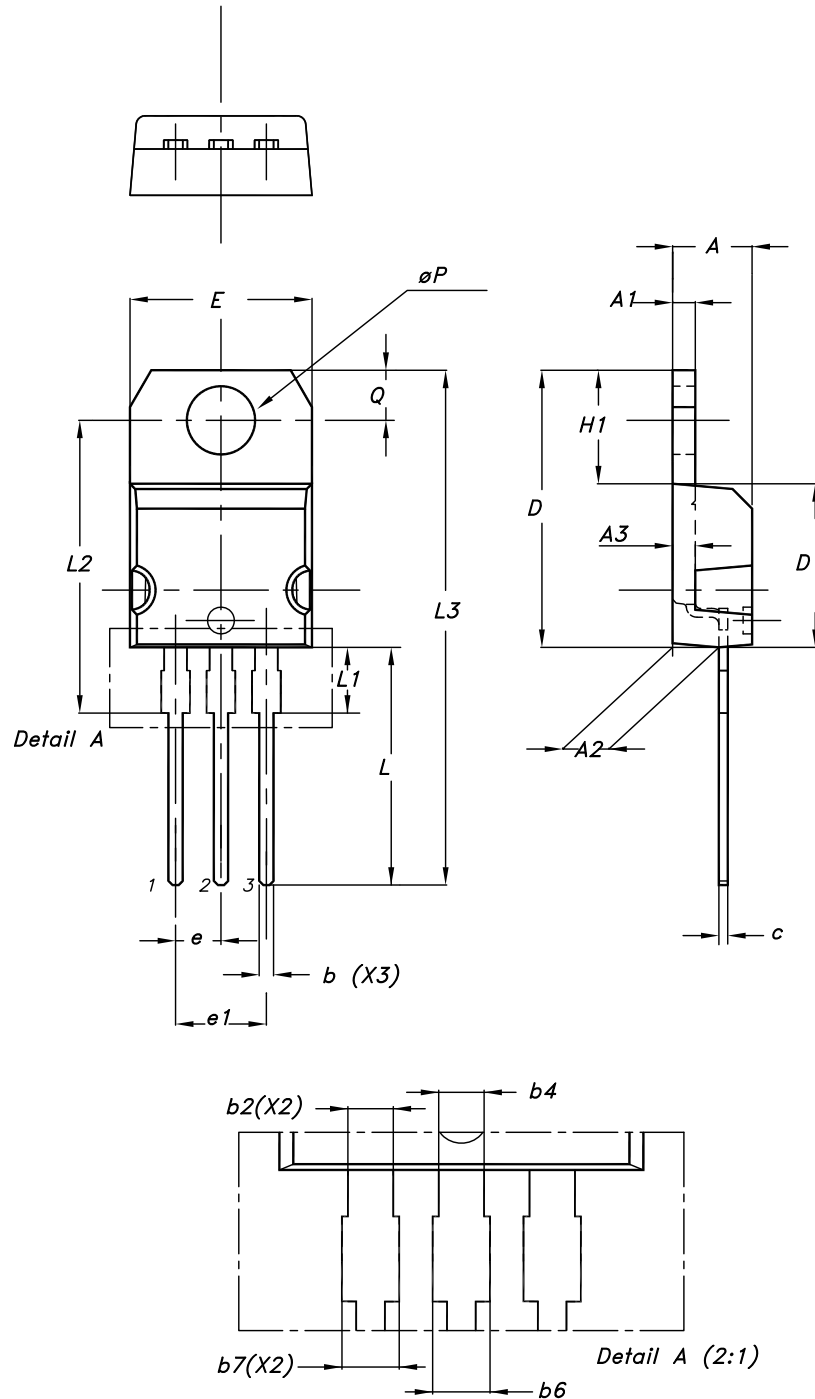
**Table 10. TO-220 type A package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.55
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10.00		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13.00		14.00
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95



### 4.3 TO-220 type H package information

Figure 27. TO-220 type H package outline



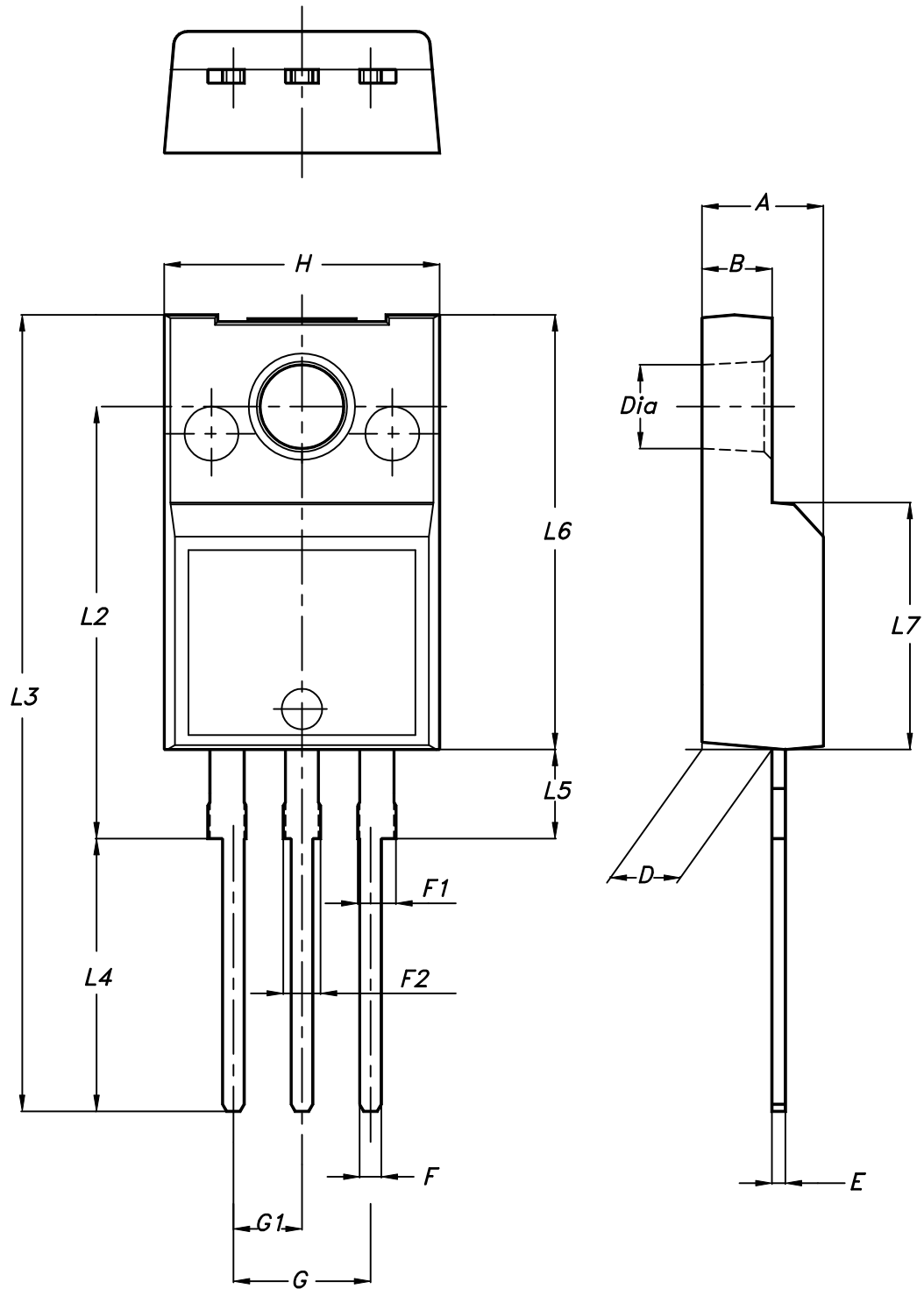
0015988\_H\_21

**Table 11. TO-220 type H package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.40	4.45	4.50
A1	1.22		1.32
A2	2.49	2.59	2.69
A3	1.17	1.27	1.37
b	0.78		0.87
b2	1.25		1.34
b4	1.20		1.29
b6			1.50
b7			1.45
c	0.49		0.56
D	15.40	15.50	15.60
D1	9.05	9.15	9.25
E	10.08	10.18	10.28
e	2.44	2.54	2.64
e1	4.98	5.08	5.18
H1	6.25	6.35	6.45
L	13.20	13.40	13.60
L1	3.50	3.70	3.90
L2	16.30	16.40	16.50
L3	28.70	28.90	29.10
ØP	3.75	3.80	3.85
Q	2.70	2.80	2.90

#### 4.4 TO-220FP package information

Figure 28. TO-220FP package outline



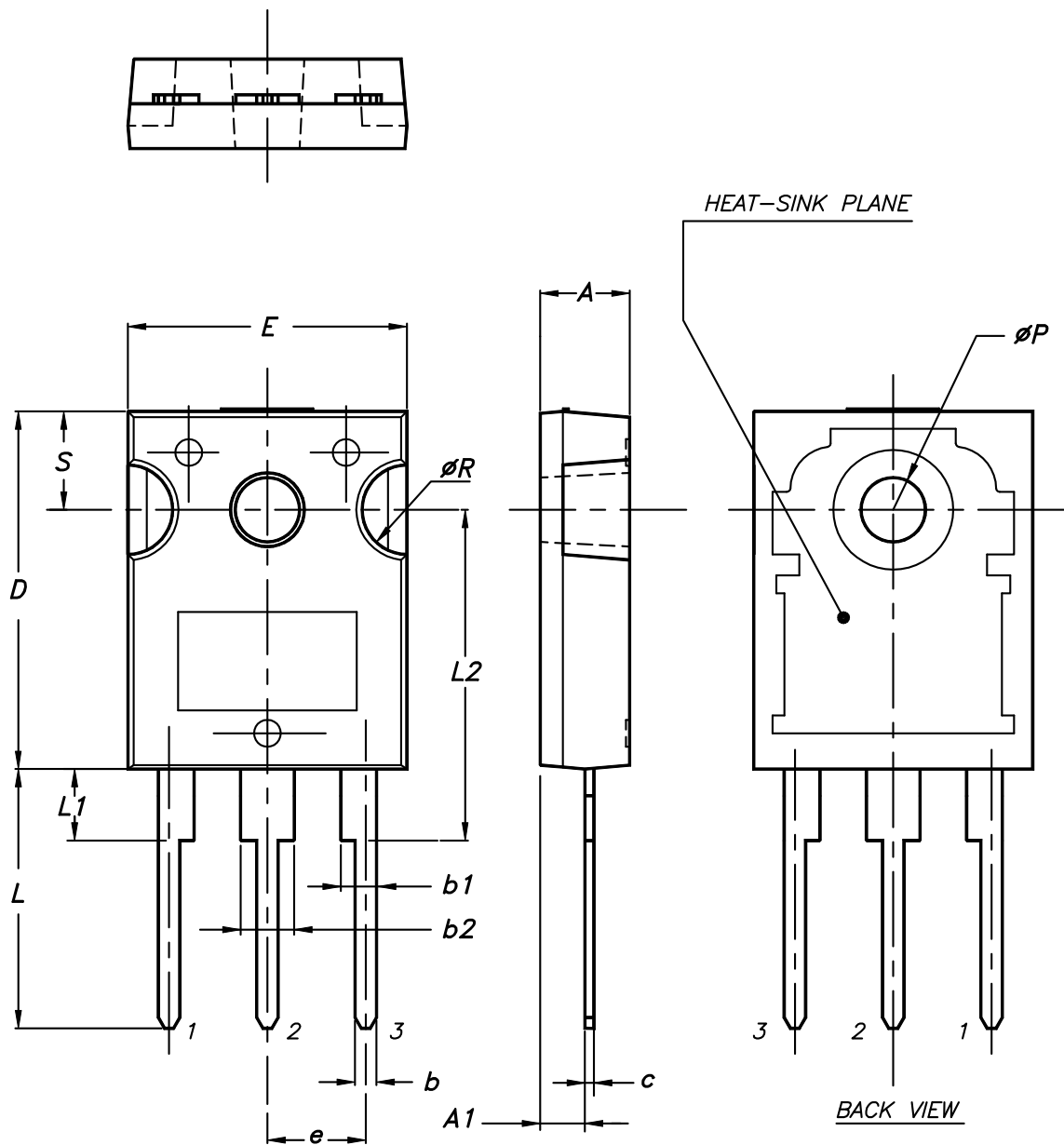
7012510\_Rev\_12\_B

**Table 12. TO-220FP package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

### 4.5 TO-247 package information

Figure 29. TO-247 package outline



0075325\_9

**Table 13. TO-247 package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e	5.30	5.45	5.60
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
ØP	3.55		3.65
ØR	4.50		5.50
S	5.30	5.50	5.70

## 5 Ordering information

Table 14. Order codes

Order code	Marking	Package	Packing
STB6NK90ZT4	B6NK90Z	D <sup>2</sup> PAK	Tape e reel
STP6NK90Z	P6NK90Z	TO-220	Tube
STP6NK90ZFP	P6NK90ZFP	TO-220FP	Tube
STW7NK90Z	W7NK90Z	TO-247	Tube

## Revision history

**Table 15. Document revision history**

Date	Version	Changes
29-Nov-2005	3	Complete version
16-Aug-2006	4	New template, no content change
10-Apr-2007	5	Typo mistake on Table 2
04-Apr-2018	6	Removed maturity status indication from cover page. The document status is production data. Updated <a href="#">Table 5. Dynamic</a> and <a href="#">Table 6. Source drain diode</a> . Minor text changes.



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<b>4.2</b>	<b>TO-220 type A package information</b> .....	<b>14</b>
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<b>5</b>	<b>Ordering information</b> .....	<b>23</b>
	<b>Revision history</b> .....	<b>24</b>



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